MATERIALS FOR HIGH RELIABILITY DEVICES



## Reliability of Cu Nanoparticles/Bi-Sn Solder Hybrid Bonding Under Cyclic Thermal Stresses

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The influence of thermal cycle stress loading on hybrid bonding, which was formed by sintering a mixture of Cu nanoparticles and a eutectic Bi-Sn solder powder, has been investigated. A Si chip and a directly bonded aluminum (DBA) substrate were bonded using the hybrid bonding layer. The bonded sample was evaluated using a thermal cycle test ( $-40^{\circ}$ C and 250°C). The degradation process of the sample during the test was observed nondestructively using synchrotron radiation x-ray computed laminography. The thermal cycle stress loading had a minimal effect on the microstructure of the bonding layer, which has a high bonding strength owing to the liquid phase sintering and high decomposition melting temperature of the Cu-Sn compound formation. This property reduced the Al deformation of the DBA substrate caused by the thermal cycle loading, resulting in the suppression of the bonding layer degradation. Therefore, hybrid bonding can be instrumental in achieving the reliable operation of power modules at high temperatures.

## **INTRODUCTION**

The realization of a sustainable society with a low-carbon footprint requires the popularization of electrified vehicles (i.e., hybrid electric vehicles, fuel cell vehicles, and electric vehicles), which have recently received growing interest.  $^{1\!-\!3}$  These vehicles have batteries, motors, and power control units (PCUs). Power devices that are mounted on power modules in PCUs operate at a high frequency to convert DC to AC power. High-power density PCUs are required to reduce their size and weight. SiC devices are instrumental in achieving high-power density PCUs because they have the potential to operate at higher temperatures than conventional Si devices. Heat-resistant bonding materials are needed to ensure the reliable operation of power modules at high temperatures. $^{4-6}$  Several heatresistant bonding methods have been reported. These include Bi- or Zn-based soldering,<sup>7,8</sup> transient liquid phase bonding,<sup>9–11</sup> and pure metallic nanoparticle sintering. Nanoparticle sintering methods provide bonding layers with a high melting

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point despite the low temperatures used in the sintering process. Among them, Ag nanoparticle sintering has received extensive attention because of its high thermal and electrical conductivity.<sup>12–16</sup> Several studies have been conducted on Cu nanoparticle sintering,<sup>17-24</sup> which is less expensive and has a higher electromigration tolerance than Ag nanoparticle sintering. A previous study<sup>24</sup> has suggested that high-reliability Cu nanoparticle bonding layers require micropore suppression and interfacial adhesion improvement. To overcome these issues, we proposed a bonding layer sintered by mixing Cu nanoparticles and Bi-Sn particles; this bonding technique was called "hybrid bonding".<sup>25,26</sup> This bonding layer formed using low additional pressure (3 kPa) showed а high bonding strength (> 30 MPa). To verify the reliable operation of power modules under high temperatures, several reliability tests, such as high-temperature storage, thermal cycles and power cycle tests, are generally required. A previous study<sup>27</sup> confirmed that the proposed bonding layer maintained its initial bonding strength after a high-temperature storage test (>  $200^{\circ}$ C). Although the thermal cycle test is crucial for ensuring the high-temperature operation of the power modules, few studies have

undertaken thermal cycle tests for hybrid bonding. This study conducts a nondestructive observation of the degradation process of hybrid bonding under a cyclic thermal stress test using high spatial resolution synchrotron radiation x-ray computed laminography (SRCL) measurements.<sup>28–35</sup>

### **EXPERIMENTAL PROCEDURE**

#### **Sample Preparation**

As shown in Fig. 1, a Si chip  $(5 \times 5 \text{ mm}^2)$  and a bonded (DBA) direct aluminum substrate  $(20 \times 20 \text{ mm}^2)$  were bonded together by hybrid bonding. The DBA substrate consisted of an AlN plate and a high-purity Al metal film (99.99%). Cu nanoparticles with a diameter of 230 nm were obtained by decanoic acid (C<sub>9</sub>H<sub>19</sub>COOH) and decylamine (C<sub>10</sub>H<sub>21</sub>NH<sub>2</sub>) modification<sup>17</sup> Commercial Bi-47 wt.% Sn particles (eutectic temperature of 137°C diameter  $< 36 \ \mu m$ ) were and obtained from Kojundo Chemical Laboratory. The Cu nanoparticles and Bi-Sn powder were mixed at a ratio of 7:3, and  $\alpha$ -terpineol was added to the mixture to turn it into a paste using a planetary centrifugal mixer. A Ti (100 nm)/Ni (200 nm)/Ag (100 nm) film was formed as an adhesive layer on the joint surface of the SiC chip and the DBA substrate by magnetron sputtering. The Si chip was mounted on the DBA substrate after applying a  $100-\mu$ m-thick layer of the paste using a metal mask. Two-step firing (first firing step: heating to 200°C and holding for 10 min; second firing step: heating to 350°C and holding for 5 min) was carried out in an H<sub>2</sub> atmosphere while applying a pressure of 0.5 MPa. The sintered sample was subjected to the thermal cycle test in atmospheric air (1 atm). The thermal cycle test was conducted under two testing conditions: (1) minimum and maximum temperatures were -40and 150°C, respectively, and the exposure time at each temperature was equal to 30 min; (2) minimum and maximum temperatures were -40 and 250°C, respectively, and the exposure time at each temperature was 60 min. During the thermal cycle testing, 200 cycles of the thermal cycle stress were applied to the sample.

## Characterization

SRCL measurements were performed from the initial state to 200 cycles at the same location of the joint sample. These measurements were conducted at the BL33XU Toyota beamline  $^{36,37}$  located at the synchrotron radiation x-ray facility SPring-8, which is characterized by a high flux density, small angular divergence, and a quasi-monochromatic energy spectrum. $^{38-43}$  The incident beam to the sample is inclined at an angle of 30° with respect to the sample surface. The SR energy (29 keV) was large enough to penetrate the sample along the direction of the incident beam. The exposure step of the sample rotation was  $0.1^{\circ}$ . The transmitted SR beam was converted to visible light by a scintillator, which was directed through a lens to a complementary-metal-oxide-semiconductor camera. The voxel size in this setup was 0.33 or 1.3  $\mu$ m. The measured projection images were reconstructed using the filtered back-projection method, considering the tilt angle of the rotational axis.<sup>28,32</sup> As shown in Fig. 1, we focused on the slices of three positions in the thickness direction. After the SRCL measurements, the samples were mechanically polished and etched by Ar ion sputtering for cross-sectional observations. The cross-sectional images and elemental maps were obtained by scanning electron microscopy (SEM) and energy dispersive x-ray spectrometry (EDS).

## RESULTS

## Thermal Cycle test at Temperatures Between – $40^{\circ}$ C and $150^{\circ}$ C

The reconstructed cross-sectional images of the hybrid bonding layer parallel to the joint surface by the SRCL measurements under the thermal cycle test ( $-40/150^{\circ}$ C) are shown in Fig. 2. The brightness of a reconstructed image reflects the weight of an element or the density of the material structure. For instance, the presence of a heavy element or a high-density structure is shown as a bright area in a reconstructed image. According to the reconstructed images before the thermal cycle test, two types of morphologies in the bonding layer were observed:



Fig. 1. Schematic diagram of the test sample layered structure.



Fig. 2. Reconstructed cross-sectional images of the hybrid bonding layer parallel to the joint surface by SRCL measurement under thermal cycle test (- 40/150°C).

(1) voids with diameters  $< 100 \ \mu m$  at both bonding interfaces, and (2) voids with diameters  $< 40 \ \mu m$  in the parent phase. Although there were some voids at the bonding interfaces ((i)-a, (i)-b, and (i)-c in Fig. 2), the interfaces appear to be almost uniform. A comparison between the reconstructed images before and after the thermal cycle loading indicates that the effect of thermal cycle stresses  $(-40/150^{\circ}C)$ on the microstructure of reconstructed cross-sectional images parallel to the joint surface was insignificant. A-A cross-sectional images of the hybrid bonding layer vertical to the joint surface under the thermal cycle test  $(-40/150^{\circ}C)$  are shown in Fig. 3. The reconstructed image by the SRCL measurements before and after 200 thermal cycles are shown in Fig. 3a and b. There were only small differences between the reconstructed cross-sectional images vertical to the joint surface before and after the thermal cycle test (Fig. 3a and b). The A-A cross-sectional SEM images vertical to the joint surface shown in Fig. 3c indicate the presence of the interfacial voids on the Si chip side ((I)-a, (I)-b) in addition to the voids in the parent phase ((II)-a). Figure 3c shows that the interfacial voids ((I)-a and (I)-b) are flat in shape, whereas the void in the parent phase ((II)-a) is spherical. Because these voids correspond to the those that were present before the thermal cycle test ((i)-a, (i)-b, and (ii-a) in Fig. 2), it is confirmed that they were not caused by the thermal cycle loading.

The cross-sectional SEM-EDS mapping of the hybrid bonding layer after the thermal cycle test  $(-40/150^{\circ}C)$  is shown in Fig. 4. Three phases (A, B, C) were observed in these images. Phases A and B are sintered Cu and Cu-Sn compounds, respectively, in the parent phase. Phase C is a Bi-related material (Bi or Bi-Ni) at the joint interface.<sup>24</sup> Because the reaction of Sn in the Bi-Sn powder with Cu nanoparticles outside the powder resulted in the spherical voids ((II)-a), those voids are presumed to be the traces of the Bi-Sn powder.<sup>25</sup> It is observed that Sn migrated widely across the parent phase, while the majority of Bi was segregated at both interfaces. The Ni layer on the Si chip and the DBA substrate remained at their interface in the bonding layer. Figure 4 shows that the initial dense layer was retained during the thermal cycle test. As a result, it was confirmed that the effect of thermal cycle loading  $(-40/150^{\circ}C, 200 \text{ cycles})$  on the degradation of the bonding layer microstructure was insignificant.

Our previous work<sup>24</sup> revealed that thermal cycle stresses  $(-40/150^{\circ}C)$  cause the propagation of cracks over a wide extent of the conventional Cu nanoparticle bonding layer due to its low sintering density. In contrast, the Cu nanoparticle sintering with the liquid phase Bi-Sn enables the densification of the sintering layer due to the liquid phase sintering and the formation of a Cu-Sn compound with a high decomposition melting temperature.<sup>25</sup>



20 µm

Fig. 3. A–A cross-sectional images of the hybrid bonding layer vertical to the joint surface under thermal cycle test (- 40/150°C): (a) reconstructed image by SRCL measurement before thermal cycle test; (b) reconstructed 2D image by SRCL measurement after 200 cycles; (c) corresponding SEM image after 200 cycles.



Fig. 4. Cross-sectional images of hybrid bonding layer after thermal cycle test (- 40/150°C, 200 cycles): SEM image (a); SEM–EDS map for Ni (b), Cu (c), Bi (d), and Sn (e).

Moreover, the initial sintered structure was unaltered even after the thermal cycle loading (as shown in Fig. 2). Therefore, this study confirms that the addition of the Bi-Sn powder to the Cu nanoparticles improves the thermal cycle reliability of the bonding layer.

## Thermal Cycle Test at Temperatures Between – $40^{\circ}C$ and $250^{\circ}C$

The reconstructed cross-sectional images of the hybrid bonding layer parallel to the joint surface by the SRCL measurements under the thermal cycle



Fig. 5. Reconstructed cross-sectional images of the hybrid bonding layer parallel to the joint surface by SRCL measurement under thermal cycle test (- 40/250°C).

test ( $-40/250^{\circ}$ C) are shown in Fig. 5. The reconstructed images before the thermal cycle test show the crack of the bonding layer (iii), traces of Bi-Sn powder (ii), and interfacial voids (i) formed by the insufficient Bi wetting.<sup>25</sup> The changes observed in the interfacial voids ((i)-d, (i)-e, and (i)-f), the Bi-Sn traces ((ii)-b), and the crack ((iii)-a) in the bonding

layer caused by the thermal cycle loading were insignificant. Therefore, these morphologies did not become weak spots of reliability. Conversely, the thermal cycle stress loading changed the almost uniform interfacial joint at the Si chip side to a nonuniform interface at the periphery of the Si chip. Moreover, we observed remarkable segregation,



Fig. 6. A–A cross-sectional images of the hybrid bonding layer vertical to the joint surface under thermal cycle test (- 40/250°C): (a) reconstructed image by SRCL measurement before thermal cycle test; (b) reconstructed 2D image by SRCL measurement after 200 cycles; (c) corresponding SEM image after 200 cycles.

assumed to be related to the Bi material designated as (iv)-a in Fig. 5. This interfacial change was remarkable up to 10 cycles, whereas the changes were insignificant after 100 cycles.

The cross-sectional images of the hybrid bonding layer vertical to the joint surface under the thermal cycle test  $(-40/250^{\circ}C)$  are shown in Fig. 6. The reconstructed images by the SRCL measurements before and after 200 thermal cycles are shown in Fig. 6a and b. The SEM image after 200 thermal cycles is shown in Fig. 6c. The interface voids ((I)-d, (I)-e, and (I)-f) were observed in the cross-sectional SEM images vertical to the joint surface shown in Fig. 6c. These voids correspond to those present before the thermal cycle test ((i)-d, (i)-e, and (i)-f in Fig. 5); therefore, they were not caused by the thermal cycle loading. This Bi segregation ((IV)-a in Fig. 6c) corresponds to the morphology ((iv)-a in Fig. 5). Figure 6c reveals the non-uniformity of the interfacial Bi-related material in the peripheral region 300  $\mu$ m inward from the chip edge, designated as region (X) in Fig. 6c. Accordingly, the thermal cycle stresses generated remarkable Bi segregation and non-uniformity of the interfacial product (region (X)).

Figure 7 shows low-magnification images of the hybrid bonding layer parallel to the joint surface on

the Si chip side obtained by SRCL measurements after the thermal cycle test ( $-40/250^{\circ}$ C, 200 cycles). The morphology ((v)-a) in Fig. 7) shows a networklike macro-void of ~ 50- $\mu$ m width in the region (Y), which originates from the gas molecules caused by the solvent in the paste and the capping layer of Cu nanoparticles.<sup>27</sup> A comparison between Fig. 7a and b indicates that the effect of thermal cycle stress loading ( $-40/250^{\circ}$ C, 200 cycles) on region (Y) was lower than that on region (X).

Figure 8 shows the cross-sectional SEM-EDS mapping of the hybrid bonding layer after the thermal cycle test  $(-40/250^{\circ}C)$ . As depicted in Fig. 4, phases A (Cu sintered part) and B (Cu-Sn compound) in the parent phase and a phase C (Birelated material) are also observed. The binary phase diagram indicates that phase B is either Cu6Sn5, Cu3Sn, or Cu41Sn11, and indicates that phase C is Bi3Ni at 350°C (second firing). In our previous study, phase B and phase C were estimated to be Cu3Sn and Bi3Ni based on the SEM-EDS results.<sup>25</sup> Although small voids and cracks caused by thermal stresses were found in the parent phase, several interfacial cracks on the Si chip side were generated between the Birelated material and the Ni adhesive layer. These results indicate that



Fig. 7. Low magnification reconstructed cross-sectional images of the hybrid bonding layer parallel to the joint surface at Si chip side by SRCL measurement after thermal cycle test (- 40/250°C): (a) before thermal cycle test; (b) after 200 cycles.



Fig. 8. Cross-sectional images of hybrid bonding layer after thermal cycle test (- 40/250°C, 200 cycles): SEM image (a); SEM–EDS map for Ni (b), Cu (c), Bi (d), Sn (e).

the thermal cycle stress only affected the interface on the Si chip side.

## DISCUSSION

# Segregation of the Bi-Related Material During the Sintering Process

The heating process for sintering causes the shrinkage of the Cu/Bi-Sn paste, while causing the expansion of the Si chip and the DBA substrate. This results in the tensile strain of the bonding layer, especially at the bonding interfaces. In the second firing process at 350°C, melted Bi migrates towards the bonding interface, where the thermal strain is large, without reacting with the sintered Cu portion. This leads to the brittle Bi segregation, which may reduce the interfacial strength at both the Si chip interface and the DBA substrate interface, as shown in Fig. 5. A similar phenomenon was reported by Satoh et al.<sup>44</sup> on Zn-mixed Cu nanoparticles/Bi-Sn solder bonding.

# Segregation of the Bi-Related Material During the Thermal Cycle Test

The thermal strain is induced by the mismatch of the coefficient of thermal expansion ( $\Delta CTE$ ) between the elements of the sample during the thermal cycle loading. The thermal strain  $\varepsilon$  applied to the bonding layer under linear approximation is given by Eq. 1: Reliability of Cu Nanoparticles/Bi-Sn Solder Hybrid Bonding Under Cyclic Thermal Stresses

$$\varepsilon = \Delta \text{CTE} \cdot \Delta T \cdot L \tag{1}$$

where  $\Delta T$  is the temperature difference during the thermal cycle test, and L is the length from the center of the joint surface. The CTE of the joint parts are as follows: Si, Al, Cu, and Cu-Sn (Cu3Sn) are 3 ppm/K, 23 ppm/K, 17 ppm/K, and 19 ppm/K, respectively. Equation (1) indicates that the thermal strain at the peripheral interfacial layer of the Si chip side increases during the thermal cycle test. It can be assumed that the large tensile thermal strain during the low-temperature period (around - 40°C) caused micro-voids in the interfacial product formed by the brittle Bi-related material. When the sample temperature was  $\sim 250^{\circ}$ C, which is close to the Bi melting point, the low-strength Bi segregated at the peripheral interfacial layer of the Si chip side. As a result, the repetition of the microvoid formation and the Bi segregation led to a nonuniform peripheral interfacial layer (X), as shown in Fig. 6c. Conversely, the uniformity in region (Y) at the interface was maintained during the thermal cycle loading because the thermal strain in region (Y) was smaller than that in region (X). Degradation at the central region of a bonding layer between a semiconductor chip and a substrate decreases its thermal and electrical conduction characteristics, resulting in a remarkable increase in the thermal resistance of a power module. In contrast, the effects of the degradation of the bonding layer in the outer peripheral region observed in this study on the conduction characteristics are assumed to be insignificant. Furthermore, because the degradation in the region (X) led to the relaxation of the thermal strain due to the thermal cycle stress loading, it is assumed that the bonding layer did not change significantly after 100 cycles.

### Degradation Mode of the Thermal Cycle Stresses with a Large Temperature Difference

DBA substrates with AlN plates of high thermal conductivity have been used for a semiconductor power module that is required to have low thermal resistance.<sup>47</sup> The Al film, which has a small Young's modulus, small yield strength, and small work-hardening rate, is often used as a metal layer for a DBA substrate because the AlN plate has low flexural strength.<sup>48</sup> Previous studies have reported the results of the thermal cycle stress test (over 200°C) on a joint sample that was composed of the semiconductor chip, the DBA substrate, and the heat-resistant bonding materials (Ag nanoparticles or Zn-related material).<sup>7,49,50</sup> Because the recrystallization temperature is regarded as half of the absolute temperature of the melting point of the metal, the rotation and coarsening of the Al grains due to the thermal cycle stress leads to Al deformation.<sup>51</sup> For this reason, the application of the thermal stresses caused the Al of the DBA substrate to deform

greatly, resulting in the formation of cracks or voids in the Ag nanoparticles or Zn-based bonding layer. In contrast, our previous study<sup>27</sup> revealed that high-temperature storage led to little oxidation of the bonding layer, suppressing the decrease in the mechanical strength. Accordingly, the high bonding strength reduced the Al deformation, resulting in the suppression of the hybrid bonding degradation.

#### CONCLUSION

The reliability of a hybrid bonding layer sintered between a Si chip and a DBA substrate under thermal stresses was evaluated by a thermal cycle test at temperatures of -40/250 °C. High spatial resolution SRCL measurements were performed to observe the degradation process of the microstructure within the hybrid bonding layer. While the impact of thermal cycle stress loading on the parent phase in the bonding layer was minimal, thermal cycle stress caused remarkable Bi segregation and a product with a non-uniform interface at the outer peripheral region on the Si chip side. It is assumed that the thermal and electrical conduction characteristics of a power module are not significantly affected by this degradation distribution. Additionally, the changes in the bonding interface result in the relaxation of the thermal strain due to the thermal cycle stress loading. Furthermore, the bonding layer has a high bonding strength, which decreases the Al deformation of the DBA substrate due to the thermal cycle loading and suppresses the degradation process of the bonding layer. Therefore, we believe that hybrid bonding can be a promising technique for achieving the reliable operation and high-power density of power modules at high temperatures.

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#### **CONFLICT OF INTEREST**

The authors claim no conflict of interest.

#### REFERENCES

- H. Ohashi, I. Omura, S. Matsumoto, Y. Sato, H. Tadano, and I. Ishii, *IEICE Trans. Commun.* E87-B, 3422 (2004).
- O. Kitazawa, T. Kikuchi, M. Nakashima, Y. Tomita, H. Kosugi, T. Kaneko, and S.A.E. Int, J. Alt. Power. 5, 278 (2016).
- T. Hasegawa, H. Imanishi, M. Nada and Y. Ikogi, SAE Tech. Paper 2016-01-1185 (2016).
- K. Hamada, M. Nagao, M. Ajioka, and F. Kawai, *IEEE Trans. Electron. Dev.* 62, 278 (2015).

- 6. T. Ogawa, A. Tanida, T. Yamakawa and M. Okamura, SAE Tech. Paper 2016-01-1230 (2016).
- Y. Yamada, Y. Takaku, Y. Yagi, I. Nakagawa, T. Atsumi, M. Shirai, I. Ohmura, and K. Ishida, *Trans. Jpn. Inst. Electron. Packag.* 79, 2 (2009).
- H. Zhang, C. Chen, J. Jiu, S. Nagao, and K. Suganuma, J. Mater. Sci. Mater. Electro. Mater. Electron. 29, 8854 (2018).
- 9. H.A. Mustain, W.D. Brown, and S.S. Ang, *IEEE Trans. Compon. Packag. Technol.* 33, 563 (2010).
- H. Ito, M. Kuwahara, H. Kadoura, and M. Usui, *IET Power Electron.* 12, 492 (2019).
- Y. Liu, S.N. Joshi, and E.M. Dede, J. Electron. Packag. 142, 011003 (2020).
- 12. K.S. Siow and S.T. Chua, JOM 71, 3066 (2019).
- W.S. Hong, M.S. Kim, C. Oh, Y. Joo, Y. Kim, and K.-K. Hong, JOM 72, 889 (2020).
- R. Khazaka, L. Mendizabal, and D. Henry, J. Electron. Mater. 48, 2459 (2014).
- M.-S. Kim and H. Nishikawa, Mater. Sci. Eng. A 645, 264 (2015).
- S.A. Paknejad and S.H. Mannan, *Microelectron. Reliab.* 70, 1 (2017).
- T. Ishizaki and R. Watanabe, J. Mater. Chem. 22, 25198 (2012).
- O. Mokhtari and H. Nishikawa, J. Mater. Sci. Mater. Electron. 27, 4232 (2016).
- Y. Liu, B. Ren, M. Zhou, X. Zeng, and F. Sun, J. Mater. Sci. Mater. Electron. 31, 8258 (2020).
- T. Ishizaki, D. Miura, A. Kuno, R. Nagao, S. Aoki, Y. Ohshima, T. Kino, M. Usui, and Y. Yamada, *Microelectron. Reliab.* 64, 287 (2016).
- T. Satoh, T. Ishizaki, and K. Akedo, J. Alloy. Comput. 691, 524 (2017).
- Y. Mou, Y. Peng, Y. Zhang, H. Cheng, and M. Chen, *Mater. Lett.* 227, 179 (2018).
- J. Xie, J. Shen, J. Deng, and X. Chen, J. Electron. Mater. 49, 2669 (2020).
- M. Usui, H. Kimura, T. Satoh, T. Asada, S. Yamaguchi, and M. Kato, *Microelectron. Reliab.* 63, 152 (2016).
- T. Satoh, T. Ishizaki, and M. Usui, *Mater. Des.* 124, 203 (2017).
- T. Satoh, T. Ishizaki, and M. Usui, J. Mater. Sci. Mater. Electron. 29, 7161 (2018).
- M. Usui, T. Satoh, H. Kimura, S. Tajima, Y. Hayashi, D. Setoyama, and M. Kato, *Microelectron. Reliab.* 78, 93 (2017).
- L. Helfen, F. Xu, H. Suhonen, P. Cloetens, and T. Baumbach, J. Phys. Conf. Ser. 425, 192025 (2013).
- 29. J.O. Suh, K.N. Tu, and N. Tamura, JOM 58, 63 (2006).
- X. Milhet, A. Nait-Ali, D. Tandiang, Y.-J. Liu, D. Van Campen, V. Caccuri, and M. Legros, *Acta Mater.* 156, 310 (2018).

- D.T. Chu, Y.-C. Chu, J.-A. Lin, Y.-T. Chen, C.-C. Wang, Y.-F. Song, C.-C. Chiang, C. Chen, and K.N. Tu, *Microelectron. Reliab.* 79, 32 (2017).
- H. Tsuritani, T. Sayama, Y. Okamoto, T. Takayanagi, M. Hoshino, K. Uesugi, J. Ooi and T. Mori, *Proc. ASME 2017 IPACK* 2017-74177 (2017) V001T01A015.
- M. Hoshino, K. Uesugi, A. Takeuchi, Y. Suzuki, and N. Yagi, *Rev. Sci. Instrum.* 82, 073706 (2011).
- T. Asada, H. Kimura, S. Yamaguchi, S. Hayashi and Y. Uyama, Proc. Int. Conf. Adv. Technol. Exp. Mech. 48 (2015).
- H. Kimura, M. Usui, M. Kamiyama, T. Asada, S. Yamaguchi, D. Setoyama, and T. Satoh, *R&D Rev. Toyota CRDL* 50-1, 39 (2019).
- T. Nonaka, K. Dohmae, Y. Hayashi, T. Araki, S. Yamaguchi, Y. Nagai, Y. Hirose, T. Tanaka, H. Kitamura, T. Uruga, H. Yamazaki, H. Yumoto, H. Ohashi, S. Goto, and A.I.P. Conf, *Proc.* 1741, 030043 (2016).
- 37. Y. Hirose, SPring-8 Research Frontiers 2009, 170 (2009).
- L. Wang, M. Li, J. Almer, T. Bieler, and R. Barabash, *Front. Mater. Sci.* 7, 156 (2013).
- J.J. Williams, Z. Flom, A.A. Amell, N. Chawla, X. Xiao, and F. De Carlo, Acta Mater. 102, 220 (2016).
- Y. Hayashi, Y. Hirose, and Y. Seno, J. Appl. Crystallogr. 48, 1094 (2015).
- D. Setoyama, Y. Hayashi, and N. Iwata, *Mater. Sci. Forum* 777, 142 (2014).
- Y. Hayashi, D. Setoyama, Y. Hirose, T. Yoshida, and H. Kimura, Science 366, 1492 (2020).
- 43. K. Tanaka, Y. Akiniwa, JSME Int. J., 47-3, 252 (2004).
- T. Satoh and M. Usui, J. Mater. Sci. Mater. Electron. 31, 6547 (2020).
- Y. Yanaka, Y. Kariya, H. Watanabe, and H. Hokazono, Mater. Trans. 57, 819 (2016).
- W.H. Tao, C. Chen, C.E. Ho, W.T. Chen, and C.R. Kao, Chem. Mater. 13, 1051 (2001).
- Y. Nagatomo, T. Kitahara, T. Nagase, Y. Kuromitsu, H. Sosiati, and N. Kuwano, *Mater. Trans.* 49, 2808 (2008).
- T. Gua. Lei, J. N. Calata, K. D. T. Ngo and G.-Q. Lu, *IEEE Trans. Dev. Mater. Reliab.* https://doi.org/10.1109/tdmr.200 9.2033668.
- C. Pei, C. Chen, K. Suganuma, and G. Fu, J. Electron. Mater. 47, 811 (2018).
- S. Nishimoto, S.A. Moeini, T. Ohashi, Y. Nagatomo, and P. McCluskey, *Microelectron. Reliab.* 87, 232 (2018).
- D. Kim, C. Chen, S.-J. Lee, S. Nagao, and K. Suganuma, J. Mater. Sci. Mater. Electron. 31, 3715 (2020).

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