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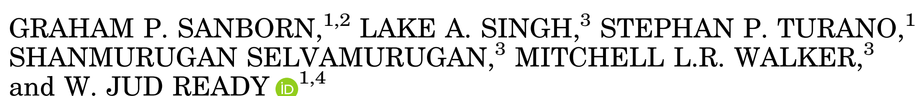
TECHNICAL ARTICLE

Field Emission Damage Modes of Carbon Nanotube Spindt Cathode Arrays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The field electron emission of carbon nanotubes has been heavily studied over the past two decades for various applications, including display technologies and spacecraft propulsion. However, a commercializable, lightweight and internally gated electron source has yet to be realized. Electrical shorting of the gate to the substrate from arcing between electrodes is a common and problematic failure mode for Spindt-type carbon nanotube electron sources, causing catastrophic damage and severely limiting their manufacturability. Other types of damage and degradation include physical damage to the carbon nanotubes and their disconnection from the substrate. This work explores field emission damage and its effects on failure in a uniquely designed Spindt-type carbon nanotube cathode. Eighty samples are fabricated and characterized for field emission performance. Analysis of the tested samples reveals three distinct types of damage to the emission pits.

INTRODUCTION

The current technologic age is embodied by a constant push for increased performance and efficiency of electronic devices. This push is particularly observable for technologies that comprise electron sources, such as spacecraft propulsion, electronic displays and x-ray sources.[1] Efficiency of these systems can be increased by reducing weight and power consumption but is often limited by a bulky electron source with a high energy demand. This work details developments for a low-power, chip-scale electron source that takes advantage of the unique material properties of carbon nanotubes (CNTs).

An alternative to traditional thermionic electron sources is field electron emission (FE), which involves the application of electric fields at room temperature to induce electron emission via tunneling. Normally, large electric fields (100 s of V μm^{-1}) are needed for FE,[2] but this field is highly dependent on the electron source geometry, where sharp tips enhance the macroscopic electric field. These FE sources can be much more efficient and reliable if emission can be achieved at a sufficiently low potential, providing marked improvement over current technologies.[1,3,4] Conductive, high-aspect-ratio nanomaterials, such as CNTs, have this favorable geometry for improving FE performance by field enhancement. CNTs are theoretically ideal for FE, having very high electrical conductivity, low work function, high temperature stability, chemical inertness and a nanoscale high aspect ratio.[5–7]

The first demonstration of the FE properties of CNTs was reported in 1994,[8] and thousands of papers have been published since.[9] Single CNT emitters are able to emit over a very large current range and have a large maximum emission current of about 0.2 mA.[10–12] Some work has explored an internally gated and arrayed CNT field emitter using a Spindt cathode-based design by separating a conductive substrate and gate with a dielectric layer.[6,13–18] This design enables higher field enhancement and reduces electrostatic screening in the arrays of isolated emission pits.

The degradation and failure of CNTs from FE have been well studied, but mostly as individual CNTs or mats of randomly oriented CNTs.[19] FE at

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high currents can quickly damage the structure of a CNT, and gradual degradation is often observed at low currents. In situ observations of CNT emission have shown segment-by-segment shortening of the CNT, structural changes to the CNT tip and loss of entire CNT walls.[12,20,21] Specifically, variations in the emitter tip radius typically result in burnout of individual field emitters from Joule heating at high saturation currents. To address this problem, scientists have incorporated vertical current limiters in series with field emitters, allowing for uniform emission without thermal runaway and overall improved reliability.[22] CNTs can also become disconnected at the substrate during emission, suggesting mechanical failure due to tensile loading and/or resistive heating at the CNT-substrate interface.[5,20] A catastrophic failure mechanism occurs from arcing between electrodes during FE. Dielectric breakdown between electrodes due to high emission currents, anode outgassing and/or local evaporation of the cathode creates a conduction channel between electrodes that generates an arc and can destroy CNTs.[4,5,23]

There are many fewer studies on the damage and failure modes from FE testing in this Spindt-based structure. The failure modes include those for individual CNTs or CNT mats, but the cathode design is especially susceptible to arcing and electrical shorting because of the small electrode separation distance. Electrical shorting of the gate to the substrate is a common and problematic failure mode that prevents the production of commercializable CNT electron sources.[13,24,25] Understanding their failure will help produce more reliable and robust Spindt-based CNT electron sources.

Spindt et al.[26] studied the damage in their metal-based emitters from arcing. In CNT Spindt-based structures, failure and damage have been observed because of disconnection of the CNTs from the substrate and arcing in the emission pits.[6,27] Recent work with Spindt cathodes revealed that the presence of damaging arcs at high voltages is not due to overheating and exploding emitter tips from poor uniformity between these tips. Rather, failure of Spindt-based electron sources can be traced to flashover along the oxide walls spurred by emission from the triple point in the cathode cavities.[28] Considering these few studies, more work is needed to understand and prevent the causes of damage in these Spindt-type emitters so their performance and reliability can be improved.

For this work, 80 Spindt-type CNT emission samples were fabricated and characterized for field emission performance. The chips were analyzed by optical and scanning electron microscopy for any damage or changes to the CNT morphology. Possible causes of the observed damage and specific mechanisms involved in the deformation of the emission pits are discussed.

MATERIALS AND METHODS

The details of the CNT electron source specifically designed to prevent shorting of the gate layer have been reported elsewhere.[16] In this design, etch pits extend into the Si substrate, and isotropic etching is utilized to create a horizontal and lateral buffer zone between the gate and CNTs, respectively. Doped silicon serves as the substrate and cathode contact. Thermally grown SiO_2, about 2 μm thick, is used as the insulator, and 500-nm-thick doped polycrystalline silicon (p-Si) is used as the gate. A schematic of the fabrication process is shown in Fig. 1. Standard ultraviolet lithography is used to pattern the substrate (Fig. 1c). Arrays of 4-μm-diameter circles across an 8.5×8.5-mm square with a 50-μm, 100-μm or 200-μm pitch are patterned on each chip.

A Bosch etch process anisotropically etches the p-Si gate (Fig. 1d), and the SiO_2 is isotropically etched in a buffered oxide etch (BOE) solution (Fig. 1e). A second Bosch etch is used to deepen the etch pits by etching into the Si substrate (Fig. 1f). An SF_6 reactive ion etch (RIE) process simultaneously removes the undercut p-Si and increases the diameter of the Si pit (Fig. 1g). The etch geometry allows for electron beam evaporation of the Fe catalyst directly on the base of the pit (Fig. 1h). A low-pressure chemical vapor deposition (LPCVD) system with precisely controlled process parameters is used to produce uniform and consistent CNT growth (Fig. 1j). The LPCVD synthesis uses C_2H_2 and NH_3 or H_2 at 700°C and 10 mbar for 0.5-5 min. The CNT growth can be precisely controlled, remains aligned past the Si pit and is uniform across many pits.

FE testing is conducted in a vacuum chamber at $<1 \times 10^{-6}$ torr in a triode design with the gate grounded, a negative bias on the cathode and a +50 V bias on an anode. A schematic of the electrical setup is shown in Fig. 2. The voltage bias set on the cathode and anode is carried via the Xantrex XFR 600-2 DC and the Xantrex XPD 60-9 DC programmable power supplies, respectively, both of which are controlled through GPIB by LabView. A PXI-4065 digital multimeter is connected to the setup to measure the emission current generated by the cathode, while a shunt box passes through the gate and anode via resistors to determine the current across the voltage drop. Gate, cathode and anode currents are independently monitored using the LabView program virtual instrument (VI) interface through a GPIB-USB connection with an Agilent 37940a data acquisition unit (DAQ).

For a given FE test, an automated current-controlled process is used. The test starts with a cathode voltage ramp in 5-V steps every 15 s until turn-on or the 200 V maximum is reached. A current density target of 10 μA/cm^2 is used. After turn-on, the voltage is automatically adjusted based on the emitted current density. Emission is sampled and voltage adjusted every 3 s to maintain the

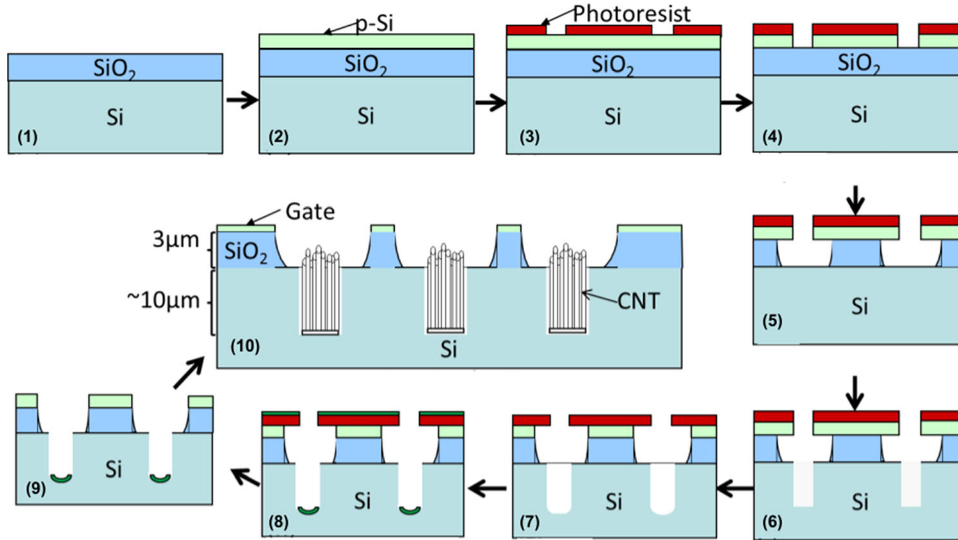

Fig. 1. Fabrication process flow for the internally gated CNT FE design involving (1) SiO_2 deposition, (2) p-Si deposition, (3) photolithography, (4) p-Si Bosch etch, (5) SiO_2 wet etch, (6) Bosch Si etch, (7) isotropic/wet Si etch, (8) Fe-catalyst deposition, (9) strip photoresist and (10) CNT synthesis. Adapted from Refs. 16 and 23.

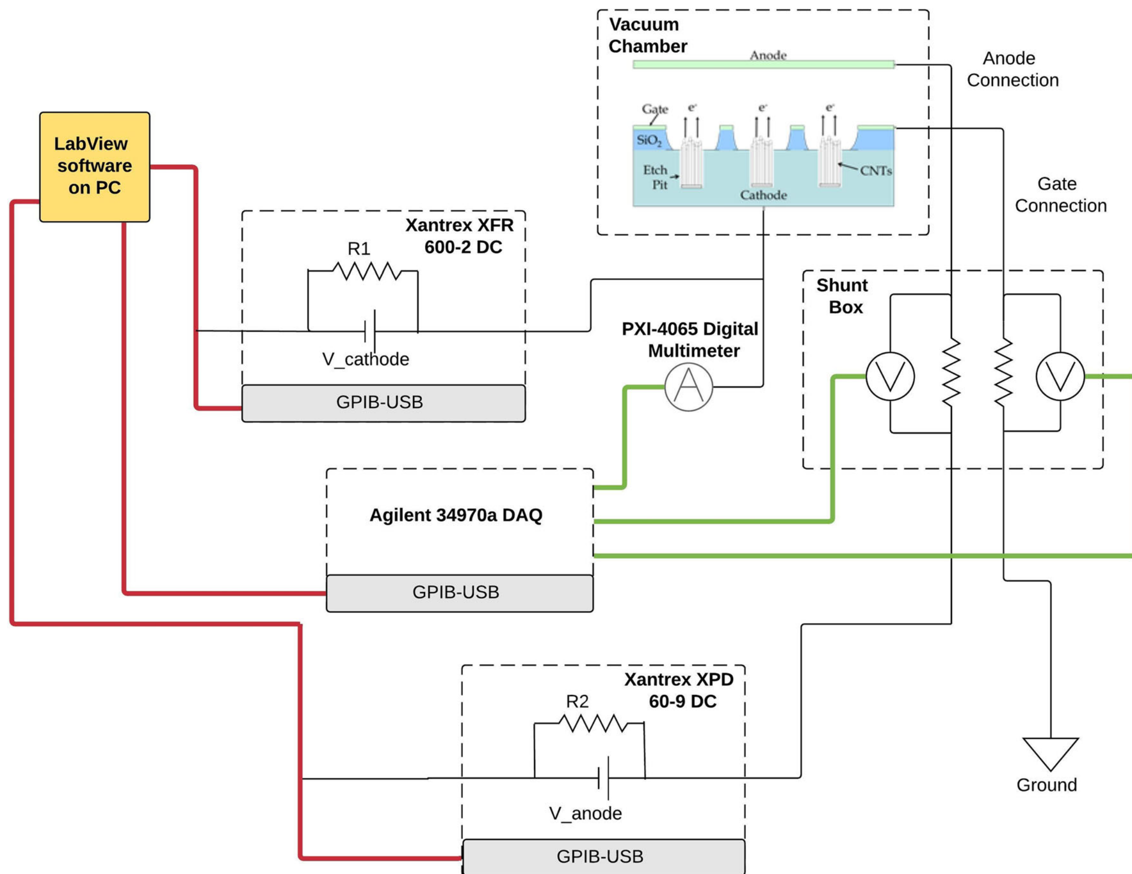

Fig. 2. Schematic of the electrical setup for FE testing.

current target. For an initial characterization test, this emission current is held for 5 min. And for a lifetime test, the current is held for a period of hours or until failure. Failure is recognized by a loss of emission at the maximum 200 V cathode voltage, or a large increase in cathode current at low voltages, indicating a possible short between the gate and cathode. Once failure is detected, the test is automatically terminated. All samples were characterized for field emission, and most were characterized

several times before microscopy analysis. Some high-performing chips were also subjected to a lifetime test before analysis. The typical emission achieved is reported elsewhere.[16]

After FE testing, the chips are analyzed for CNT degradation and damage by optical microscopy (OM) and scanning electron microscopy (SEM). This qualitative analysis is carried out on all tested chips, regardless of their emission performance or failure. OM is used as a quick way to scan over an entire chip and inspect every emission pit to note any damage. Since the SEM is higher magnification, it is impractical to image all pits in a sample. As a result, SEM is used primarily to closely investigate any noted damage from OM and to inspect portions of the chip.

RESULTS AND DISCUSSION

Of the 80 chips tested, 35 or about 43% showed at least one type of observed damage after field emission characterization, regardless of whether the chip electrically shorted or not. In most cases, the number of damaged pits is minimal at < 15 pits per chip of the 1800–30,000 total pits, depending on pitch. However, four chips show > 50 damaged pits, with a maximum amount of damage at about 5% of the pits. In addition, 18 of the damaged chips were not electrically shorted, indicating that the chip design has substantial damage tolerance. Results from the first I-V test on the number of electrically shorted and open chips are provided in Fig. 3. From the optical and electron microscopy investigations of the samples that underwent multiple emission tests, three distinct damage modes were identified.

Damage Mode I: Poly-silicon Melting

One common type of damage is an outward melting of the p-Si gate around an emission pit aperture. Figure 4 is an optical micrograph of an array of undamaged pits, with an arrow indicating one pit with the typical observed damage. Figure 5 shows an SEM image of a normal emission pit and a damaged pit from the same sample. In the normal emission pit, the gate and Si aperture are well defined, and the CNT bundle is unobstructed. With damage mode I, the p-Si area around the feature has quickly melted away from the pit and resolidified, causing the damage seen in Fig. 5b.

It is proposed that damage mode I occurs when a conductive species, such as a CNT, bridges between the silicon pit or CNT in the pit and the p-Si gate surface, creating an electrical short. The resulting high current density of the short locally increases the temperature of the p-Si near the emitter pit opening above its melting temperature (1414°C). This local temperature increase causes the gate material to melt and flow. The p-Si can cool and resolidify because of (1) the melting material removing the short circuit, (2) the high current density burning out the short or (3) the removal of the electrical potential.

It is possible that this type of damage could be a healing mode by removing an electrical short, especially since this damage has been observed on chips that are not shorted. The outward melting of the p-Si suggests this type of damage is a very fast, nearly explosive event, where the damage occurs almost instantly and either removes the short or sustains a short on the entire chip.

Damage Mode II: Melting Within the Etch Pit

The second type of damage commonly observed is melting within the emission pit with limited damage to the p-Si. Figure 6a shows an SEM image of an emission pit with this type of damage. Compared with the undamaged pit in Fig. 5a, the silicon

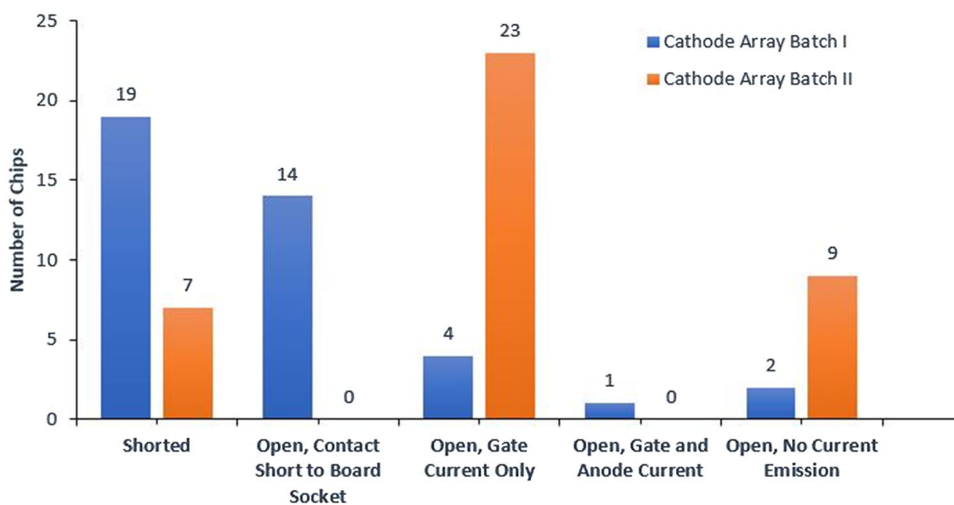

Fig. 3. Number of chips with open and shorted circuits from an initial I–V test identified by measuring the cathode-to-gate resistance with a Keithley 2400 sourcemeter. Samples were divided into two groups, with batch I used for repeated I–V tests and batch II used for exposure to a Hall-effect thruster.

aperture is no longer defined, and the CNTs are obstructed. The SEM analysis suggests that the silicon pit melts and resolidifies around the CNT bundle. Often the CNTs are still visible within the melted material and look undamaged, indicating an electrical short is not directly through the CNT bundle. Figure 6a shows that the insulating layer has not melted, suggesting there is no breakdown of the oxide.

Similar to damage mode I, it is proposed that damage mode II occurs when a conductive species bridges between the silicon or CNT in the pit and the p-Si gate surface, creating an electrical short. The fact that the p-Si gate is not significantly damaged could be explained by having a lower current density around the p-Si, but a higher current density through the silicon pit, which is high enough to cause melting. This situation could be possible, for example, by having a short with a larger contact area on the p-Si.

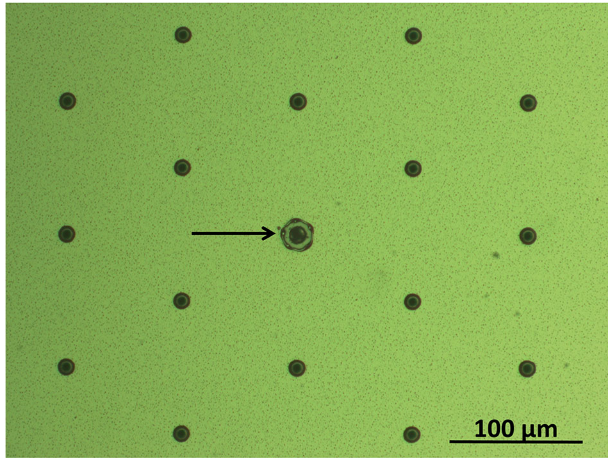

Fig. 4. Optical micrograph of an array of emission pits with arrow indicating a damaged pit with p-Si melting away from the pit.

Combination of Damage Modes I and II

Although damage modes I and II are observed, there is often a combination of these two modes present in a damaged pit, where the amount of each damage mode varies. Figure 6b shows an SEM image of an emission pit where there is both significant melting to the silicon pit and outward melting to the p-Si gate. In this case, there is melted

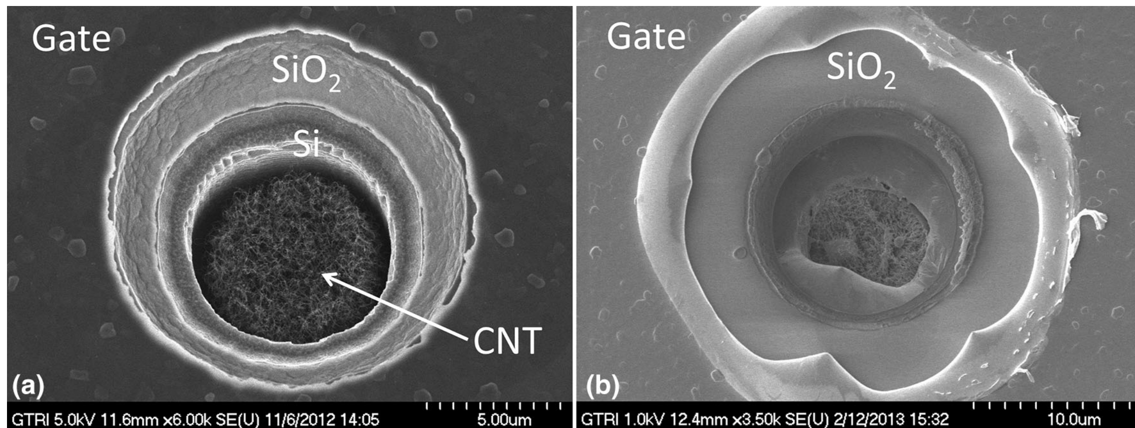

Fig. 5. SEM image of (a) normal and (b) damaged emission pit with outward p-Si melting.

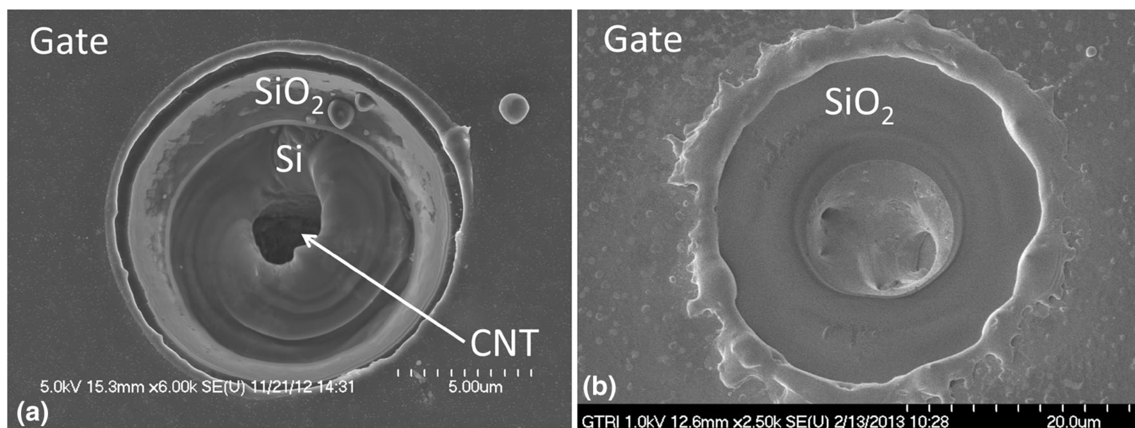

Fig. 6. SEM image of an emission pit with (a) damage mode II and (b) a combination of damage modes I and II.

material covering the pit, so the presence of CNTs cannot be observed. Damage modes I and II are observed around emission pits, as well as around areas with processing defects, i.e., features that are inadvertently transferred to the surface because of lithography defects, particles or damage to the photoresist.

Damage Mode III: Material Ejecta

A third type of damage is frequently observed where, in combination with the other two damage modes, there is a pattern of ejected material around the damaged pit. As seen in the optical and SEM images in Fig. 7, the damage leads to discoloration and ejection of material in a radial pattern far away from the damaged pit. The emission pits around the damaged pit appear to be undamaged and unaffected by the material ejecta. Like the other damage modes, this damage can also occur at the edge of a processing defect.

Comparison of the damage in Fig. 7a and b reveals that the damage does not always look the same in optical and electron microscopy. Figure 7 shows a side-by-side comparison of the same damaged spot using the two techniques. The arrow indicates the same damaged pit, which is at the vertex of a line-processing defect on the p-Si. In the optical image, there is no evidence of the ejecta seen in the SEM image. The presence of this pattern in only the SEM image could be due to a change in the electrical conductivity of the ejected versus p-Si material in this region, which would not be observable using OM.

As with the other damage modes, it is proposed that damage mode III occurs when a conductive species bridges between the silicon or CNT in the pit and the p-Si gate surface, creating an electrical short. In this case, the electrical short is probably a particularly fast and explosive event, such that material around the shorted pit is ejected.

As mentioned earlier, the electrical short that causes the damage could be created between CNTs that become detached or CNTs that are grown near the surface of the pit because of of a processing defect. Figure 8b shows a magnified SEM image of this case, where CNTs are inadvertently grown close to the gate because of a processing defect. The damage mode III ejection pattern seen around the CNT defect in Fig. 8a indicates that the CNT defect could be a cause of the damage. For example, during FE testing, some CNTs in the defect could have come into contact with the gate, causing a temporary short, destruction of the shorting CNT and ejection of material.

Damage Mechanism

SEM analysis, such as the images shown in Figs. 5–8 and in supplementary Fig. S-1 to S-8 (refer to online supplementary material), indicates that damage and melting are focused on the silicon and p-Si materials. When the CNTs are not completely covered by melted material, they are present and look unaffected. This observation suggests that the electrical short is mostly not occurring through the CNTs, except when the CNTs are part of a processing defect (Fig. 8).

Energy-dispersive x-ray spectroscopy (EDS) was performed on each type of damage to determine if there was any foreign material present that could be a cause of the damage. This spectroscopy was used to detect any contamination around the damage, especially heavier atoms, other than the carbon, silicon and oxygen natively present on the samples. EDS analysis as shown in supplementary Fig. S-9 reveals that no unexpected materials were in or around the damaged regions.

Considering that contamination or deposition of material is probably not a cause for the damage, there are two general possible causes of the formation of an electrical short in the CNT emission pit:

1. The formation of a physical electrical connection between the two electrodes.
2. Dielectric breakdown of the vacuum gap between the two electrodes in an emission pit.

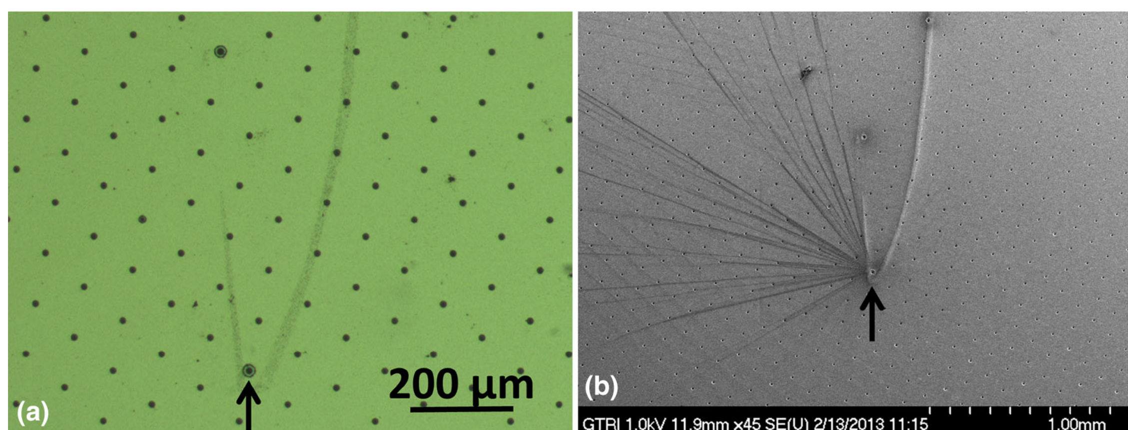

Fig. 7. (a) Optical and (b) SEM images of the same damaged pit showing how damage mode III can look different between the two methods.

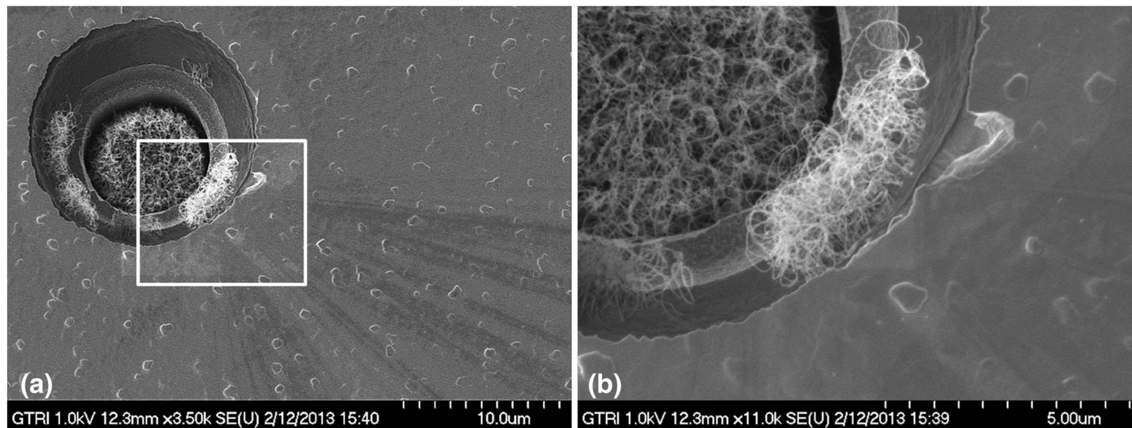

Fig. 8. SEM images of damage mode III caused by a CNT defect by the edge of the p-Si. Box in (a) indicates the magnified region (b).

The first cause could be due to a foreign body, such as a metal catalyst particle or contamination from handling. In this case, implementing a protective shield to serve as a screen for the Spindt-type CNTs may prevent such contamination, especially gas absorption on the cathode base, thereby mitigating damage sustained by the CNTs.[29] However, further analysis suggests that this cause is most likely due to stray CNTs or amorphous carbon from the CVD synthesis. The electrical connection may also be the result of the large electric field between the electrodes during testing, causing the “kinky” CNTs to physically straighten and move toward the gate. This phenomenon is hard to confirm because the CNTs would likely revert to their original coiled shape once the potential is removed. However, CNTs have been shown to move during FE and in the presence of strong electric fields.[5,20] SEM comparison of the CNTs before and after field emission testing shows no significant changes or loss of CNTs, indicating that most CNTs are not being permanently pulled out or changed during testing. To prevent this type of electrical short, the CNTs are intentionally synthesized to a height several micrometers below the gate to provide a larger vertical separation between the two electrodes.

The second potential cause of an electrical short arises from the idea that increased localized pressures around the pits could provide enough gas molecules to form an arc from dielectric breakdown in the large electric field during testing. The small 2–3-μm gate-to-cathode electrode separation results in an electric field strong enough to cause arcing at atmospheric pressure at just 20–30 V.[30] The literature shows that these Spindt-type structures can outgas significantly and often require baking because of the extremely large surface area of the pit/CNT geometry.[5,26,31] Thus, the outgassing could increase the localized pressure enough to allow an arc within the pit. The use of a bake-out or a UV lamp in vacuum could improve FE performance[5,31] and prevent FE damage in these emitters, and this is the subject of ongoing studies. The baking or UV exposure can help drive out moisture on the samples during pump-down and minimize outgassing during testing.

It is important to note that the damage modes observed do not always indicate an electrical short between the gate and cathode layers. About half of the damaged chips tested were not electrically shorted, and chips that were not shorted were observed with all three types of damage. In addition, the four chips that were observed with many damaged pits are all electrically open. This result indicates that the chips can survive for an extended period with significant damage. An oxygen plasma etch treatment may also be applied on the CNTs to reverse shorting without subjecting the Spindt-based cathodes to physical deterioration.[32] However, the chips by themselves are inherently designed to induce a self-restoration mechanism that eliminates temporary individual shorts by accumulating damage over time.

These observations indicate that there is robustness in this electron source design that allows damage to reverse electrical shorting and for the accumulation of significant damage before failure from shorting. It is proposed that the horizontal and lateral separation of the CNTs from the gate in this particular chip design allows for this robustness, permitting damage and melting without causing an electrical short. In addition, this evidence substantiates the perceived enhanced reliability of CNT Spindt-based cathodes from the reduced possibility of single point failures in the arrayed pit design, a common failure mode in traditional electron sources.

Distinct damage types are observed in these structures, which are indicative of the possibility of various mechanisms for damaging the pits. These different damage types need to be further studied to learn about how and why they occur. With a good understanding of the damage mechanisms, informed designs and engineering can be made to prevent damage and further enhance the performance of these CNT Spindt-type emitters.

CONCLUSION

This work explores field emission damage in a uniquely designed Spindt-type carbon nanotube electron source. Eighty different samples were fabricated and characterized for field emission performance. The chips were analyzed by optical and scanning electron microscopy for any damage or changes to the CNT morphology. The chip analysis reveals three distinct types of damage that are repeatedly observed: melting of the p-Si gate, melting within the silicon emission pit and material ejection around the pit aperture. About 43% (35 of the 80 chips) show at least one type of damage. Two possible damage mechanisms are proposed, caused by either a conductive species or dielectric breakdown in the emission pit. The testing revealed that about half of the damaged chips are not electrically shorted, and all the heavily damaged pits are not shorted. These observations reveal that the chip design is robust and can contribute to a reliable FE source. An understanding of these types of damage and their effect on failure will help improve the reliability and performance of Spindt-type electron sources.

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ELECTRONIC SUPPLEMENTARY MATERIAL

The online version of this article (https://doi.org/10.1007/s11837-019-03921-x) contains supplementary material, which is available to authorized users.

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