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A Review of Interface Microstructures in Electronic Packaging Applications: Soldering Technology

PAUL T. VIANCO[1,2]

1.—Sandia National Laboratories, Albuquerque, NM, USA. 2.—e-mail: ptvianc@sandia.gov

This report examines the role of interfaces in electronic packaging applications with the focus placed on soldering technology. Materials and processes are described with respect to their roles on the performance and reliability of associated interfaces. The discussion will also include interface microstructures created by coatings and finishes that are frequently used in packaging applications. Numerous examples are cited to illustrate the importance of interfaces in physical and mechanical metallurgy as well as the engineering function of interconnections. Regardless of the specific application, *interfaces are non-equilibrium structures*, which has important ramifications for the long-term reliability of electronic packaging.

INTRODUCTION

Interfaces have a significant role in a wide range of engineering structures from the nanometer-sized conductors used in microprocessor chips to the solder joints that attach advanced packages to the printed circuit board. Numerous studies have addressed the fundamental structures and properties of interfaces; references[1–5] comprise a sample of several such resources.

Regardless of the specific application, the following premise underscores both the scientific and engineering aspects of interfaces: *interfaces are non-equilibrium structures*. The non-equilibrium condition has two ramifications. The first consequence is that the physical metallurgy cannot always be readily predicted by equilibrium data and principles. For example, binary and ternary phase diagrams can only provide a first-order determination of *likely* phase structures that form at an interface.[6,7] The non-equilibrium stipulation results in unexpected microstructures having, at times, unpredictable mechanical properties. Anticipating the microstructure of an interface relies heavily upon empirical observations, which are then often correlated to equilibrium test data (e.g., phase diagrams) as a first-order predictive methodology.

The second consequence of the non-equilibrium nature of interfaces is that their microstructures can continually change with time. In some cases, those changes take place over several seconds while in other instances the time period may extend up to, or beyond, the service lifetime of the structure. The latter situation is often referred to as *pseudo-equilibrium* or *quasi-equilibrium*. Therefore, understanding the rate kinetics is an important facet in predicting the long-term microstructure, performance, and reliability of changing interfaces.

The objective of this report is to review the critical interfaces that are found in electronic packaging with a focus on *soldering technology*. A later report will address the two other joining technologies used in packaging applications: *brazing* and *welding*. The section: "Soldering Technology and Interfaces" begins by examining the interfaces that develop between a molten solder alloy, the base material, and the flux during the soldering process. Next, a detailed discussion highlights changes to the interface microstructure after solidification when solid-state interface reactions are active in the joint. Those processes are correlated to the reliability that can be expected of the solder joint in service. The next section is entitled: "Coatings and Finishes" and considers interfaces that are created by deposited coatings and surface finishes, which are now so critical to advanced packaging technologies. A short primer describes physical vapor deposition (PVD), electro- and electroless plating, as well as thick-film technologies. That information is correlated with actual applications to illustrate the importance of understanding the effects of coatings and finishes and, specifically, their associated interfaces on

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solder interconnection properties. Computation modeling is examined as a tool for predicting the development of interface reaction layers. However, the final section, “Future Trends,” affirms the need to understand the materials science and engineering of interfaces to predict the reliability of solder interconnections with increasingly smaller dimensions.

Many of the examples presented in this report were based upon the use of the eutectic or off-eutectic tin-lead (Sn-Pb) solder. In fact, the Sn-Pb alloys are still used extensively in the assembly of high-reliability electronics—although Pb-free solders are making inroads into this community as well. Nevertheless, many of the underlying precepts and behaviors described below are applicable across the variety of solder alloys used in both consumer and high-reliability electronics. An understanding of the materials science and engineering principles is essential to address the finer details of interface reactions that are a function of not only the particular solder composition, but also the base material, surface finish, and process parameters.

A sufficient, but certainly not fully complete, reference section is provided at the end of the text. The reader is encouraged to explore additional print and electronic resources to gain a further understanding of interfacial phenomena and their effects on the performance and reliability of interconnections that are critical to electronic packaging technologies.

SOLDERING TECHNOLOGY AND INTERFACES

Materials and Processes: Molten Solder Interface

The predominant joining technology in electronic packaging is *soldering*. Soldering is defined as a joining process that uses a *filler metal* (“solder” or “solder alloy”) having a liquidus temperature < 450°C.[8] Solder alloys can have a range of compositions based upon elements that include gallium (Ga), indium (In), bismuth (Bi), tin (Sn), lead (Pb), and silver (Ag) as well as gold (Au). Gold-based alloys are used as the high-melting temperature, die-attach solders. Besides establishing the melting properties of the solder, these elements, either by themselves or in alloy combinations, affect the soldering process by the interfaces formed between them (as liquids) and the base material as well as flux.

Figure 1 shows the schematic diagrams of a horizontally oriented, base material, and *sessile drop geometry*. The sessile drop profile is controlled by gravity as well as the *interfacial tensions*, γ_{SF}, γ_{SL}, and γ_{LF}. The interfacial tensions are defined below:

- γ_{SF}, base material (S)/flux (F) interface
- γ_{LF}, liquid solder (L)/flux (F) interface, and
- γ_{SL}, base material (S)/liquid solder (L) interface.

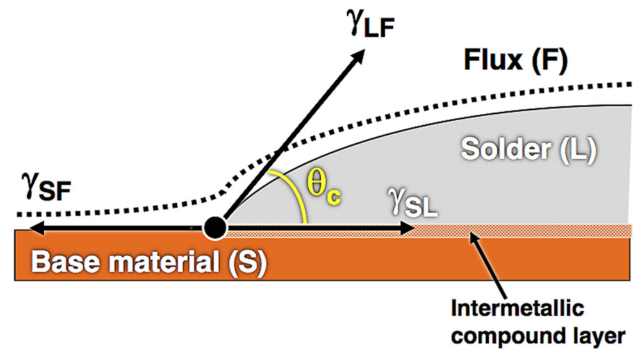


Fig. 1. Schematic diagram shows the horizontal or “sessile drop” geometry to describe the wetting and spreading activity of molten solders. The interfacial tensions, γ_{ij} (ij = SF, SL, and LF), and contact angle, θ_c, are indicated in each diagram.

These interfacial tensions each have a role in the soldering process. The value of γ_{SF} is determined by the interface between the flux coating and base material. The purpose of the flux is to *maximize the value of* γ_{SF} by removing oxides and other inorganic contaminants (e.g., corrosion layers) from the base material surface. An oxide-free surface provides an increased driving force for wetting and spreading by the molten solder. The flux must also protect the now-pristine base material surface from re-oxidation by the elevated temperatures present during the soldering process.

The cleaning function of the flux is a chemical reaction and thus is a function of formulation and temperature. The rate kinetics generally increases with temperature. However, a prolonged exposure to excessively high temperatures degrades the ability of the flux to reduce surface oxides. In fact, if the flux is very badly degraded, it becomes an organic contaminant that, by itself, impedes wetting and spreading by the solder on the base material surface. Therefore, thermal stability of the flux must be considered when defining the details of a soldering process such as ramp rates, preheat hold times, peak temperature, and time above liquidus.

The second interfacial tension, γ_{LF}, is determined by the compositions of the molten solder and flux material. Wetting and spreading are improved when the flux *minimizes the value of* γ_{LF}. This objective is realized by removing the oxide layer (or “skin”) from the molten solder surface and protecting that surface from re-oxidation during the soldering process. The flux chemistry has a significant effect on this role. Temperature has a lesser effect on γ_{LF} compared with its role in the cleaning function (γ_{SF}) or the solder/base material interface reaction (γ_{SL}).

The molten solder surface tension, as it affects γ_{LF}, is also dependent upon the alloy composition. Elements such as Pb and Bi reduce the molten alloy surface energy, while Au and Ag tend to increase it. As expected, both trends are dependent upon the

concentration of the elements. However, typical soldering process temperatures do not significantly change the intrinsic surface tension of solder alloys. These points are illustrated in Table I.[9] The value of γ_{LF} is shown as a function of three solder compositions: 96.5Sn-3.0Ag-0.5Cu (wt.%) solder, abbreviated Sn-Ag-Cu; 60Sn-40Pb (Sn-Pb), and 58Bi-42Sn (Bi-Sn). The same flux and copper (Cu) base materials were used in all cases. The Pb- and Bi-containing alloys have considerably lower values of γ_{LF} compared with those of the Sn-based alloy having Ag and Cu. Lead (Pb) and Bi lower the molten solder surface tensions. The limited effect of temperature on γ_{LF} is shown by the Sn-Ag-Cu and Sn-Pb data. In fact, a non-monotonic trend is observed with the Sn-Ag-Cu surface tension, which further illustrates the variable behaviors exhibited by the flux/molten solder interface.

The third interfacial tension is γ_{SL}. The value of γ_{SL} is determined by the reaction between the molten solder and base material. The most-often observed interfacial reaction product is an *intermetallic compound (IMC)* layer. This scenario is illustrated by the scanning electron microscope (SEM) photographs in Fig. 2.[10] The image in Fig. 2a shows the IMC reaction layer that formed along the interface between the 95.5Sn-3.9Ag-0.6Cu (Sn-Ag-Cu) solder and Pd base material. The layer composition was (Pd, Cu)Sn_4 with a Cu concentration in the range of $0 < Cu < 2$ at.% as determined by electron probe microanalysis (EPMA). The IMC layer developed with a columnar microstructure and exhibited a relatively uniform thickness along the Sn-Ag-Cu/Pd interface.

A different interface reaction developed when the solder was changed to the 63Sn-37Pb (Sn-Pb) alloy as shown in Fig. 2b. The process temperature and time remained the same. The IMC layer was a combination of $PdSn_3$ and $PdSn_4$ phases. Although Sn was the primary reactant, the presence of Pb versus Ag and Cu in the filler metal caused an entirely different microstructure and phase compositions to form at the interface.

A second feature observed in Fig. 2a is the presence of $PdSn_4$ (IMC) needles in the Sn-Ag-Cu microstructure. It is instructive to note that the needle shape is a two-dimensional rendering of the phase; they can actually be plates in three dimensions, depending upon their level of development. These needles resulted from the dissolution of Pd into the molten Sn-Ag-Cu alloy and their formation upon solidification. Base material dissolution is an ancillary process that occurs at the solder/base material interface. Generally, base material dissolution does not directly affect γ_{SL} unless there is a change of composition with depth into the base material. However, the elemental additions made to the molten filler metal by base material dissolution can alter γ_{LF} because the latter is sensitive to the molten solder composition (e.g., Table I). The Pd-Sn phase particles were not detected in the Sn-Pb solder field as shown in Fig. 2b, further accentuating the effect of the solder composition on base material dissolution behaviors.

The combination of the interfacial tensions controls the overall solderability of the solder/flux/base material system by minimizing the latter's overall free energy. The free energy is minimized under an *equilibrium condition*. At equilibrium, the effects of the interfacial tensions are combined together quantitatively through Young's equation:[11]

$$\gamma_{SF} - \gamma_{SL} = \gamma_{LF} \cos \theta_c \tag{1}$$

The parameter θ_c is referred to as the *contact angle*. Solderability is optimized by minimizing the value of θ_c. The value of θ_c is reduced by maximizing the difference $\gamma_{SF} - \gamma_{SL}$. This difference is increased by raising the value of γ_{SF}, which is precisely the role of the flux when eliminating an oxide layer from the base material surface. The difference is also maximized by reducing the value of γ_{SL}. The value of γ_{SL} is less sensitive to the process parameters because it is controlled by the reaction layer that forms at the solder/base material interface. As noted above, the reaction layer composition is determined primarily by the solder and base materials. Soldering time and temperature affect γ_{SL} only when they alter the reaction layer composition.

The value of θ_c can also be reduced by minimizing the solder-flux interfacial tension, γ_{LF}. The flux has a critical, albeit often unrecognized, role in solder

Table I. Effect of solder composition and process temperature on the solder/flux interfacial tension, γ_{LF}, and contact angle, θ_c

Solder (wt.%)	Temp. (°C)	γ_{LF} (dyne/cm)	θ_c (°)
95.5Sn-3.9Ag-0.6Cu	260	497 ± 16	40.0 ± 1.0
	245	444 ± 17	39.0 ± 1.0
	230	485 ± 17	42.0 ± 1.4
60Sn-40Pb	260	380 ± 10	29 ± 2
	245	390 ± 20	32 ± 1
	230	390 ± 10	28 ± 1
	215	380 ± 20	31 ± 2
58Bi-42Sn	215	310 ± 50	37 ± 7

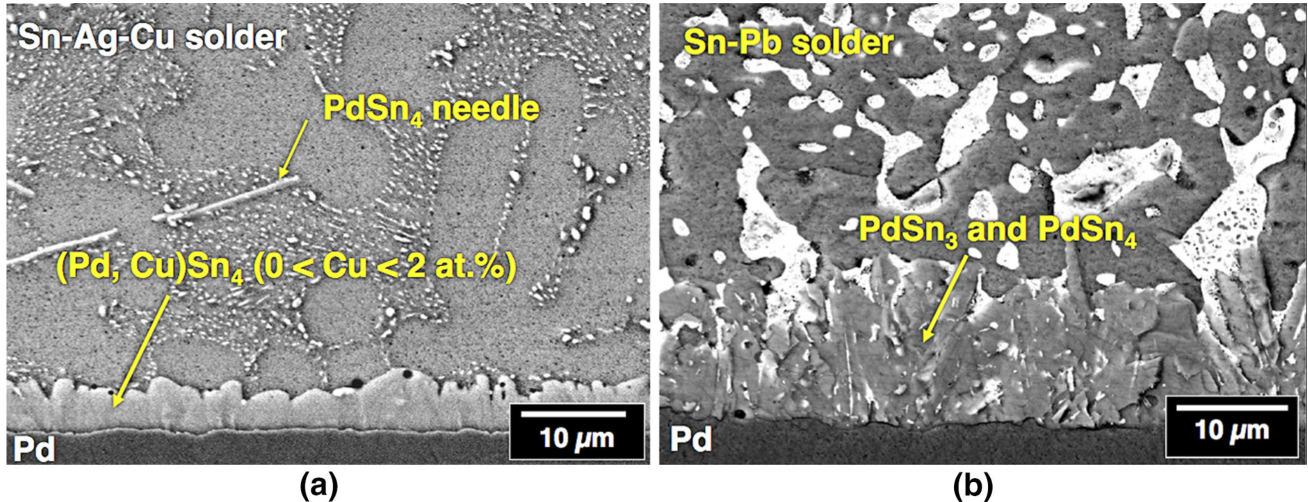


Fig. 2. SEM image shows the interface and solder microstructures that formed between the Pd base material and molten (a) 96.5Sn-3.9Ag-0.6Cu (Sn-Ag-Cu) solder and (b) 63Sn-37Pb (Sn-Pb) solder. The process conditions were 290°C and 5 s. The IMC layer and phase compositions are identified in the images.

Table II. Interfacial tensions and contact angle as function of base material and surface finish

Solder (wt.%)	Base material	γ_{LF} (dyne/cm)	$\gamma_{SF} - \gamma_{SL}$ (dyne/cm)	θ_c (°)
60Sn-40Pb	Copper	380	370	17
	Au/Ni (Kovar™)[a]	330	325	11
96.5Sn-3.5Ag	Copper	460	380	36
	Au/Ni (Kovar™)	370	310	34
100Sn	Copper	470	360	40
	Au/Ni (Kovar™)	390	280	44

Solder temperatures: 60Sn-40Pb, 260°C; 96.5Sn-3.5Ag, 260°C; and 100Sn, 270°C; Flux: rosin-based, mildly activated (RMA), diluted 1:1 with isopropyl alcohol. [a]Kovar™ is a registered trademark of Carpenter Technologies, Reading, PA.

wetting and spreading by reducing the surface tension of the molten solder (γ_{LF}). Table I showed values of γ_{LF} of 380–390 dyne/cm when the molten Sn-Pb solder is coated with a rosin-based, mildly activated (RMA) flux. In the absence of a flux, Muir reported a surface tension of 492 dyne/cm for the molten 63Sn-37Pb alloy.[12]

The dissolution of base materials or surface finishes changes the composition of the molten solder and thus can also affect γ_{LF}. Mention was already been made of this scenario in the discussion around Fig. 2. A similar effect is had from surface finishes. Gold is a common protective surface finish used to maintain the solderability of the Ni-solderable layers placed on base materials. (Surface finishes are discussed in detail in a later section.) During the soldering process, Au is dissolved into the molten solder. The total free energy of the system is reduced when the Au atoms diffuse to the molten solder *surface* because the Au reduces the latter's surface tension and consequently the value of γ_{LF}. This scenario is illustrated quantitatively by the solderability data in Table II.[13,14] The value of γ_{LF} decreased for all three solders when the base material was changed from Cu to the Au/Ni-plated Kovar™ owing to the presence of Au on the molten solder surface. The other parameters, $\gamma_{SF} - \gamma_{SL}$ and θ_c, were also included in Table II to illustrate the point that overall solderability of the base material/solder/flux system, as reflected by θ_c, is still dependent upon all three interface tensions.

Different flux chemistries give rise to different values of γ_{LF} when using the same solder alloy. This behavior is illustrated by the data in Table III.[13] Flux "A" is a rosin-based, mildly activated product, while the other four fluxes are water-soluble, halide-containing materials. The flux lowers γ_{LF} through its intrinsic interaction with the molten solder surface along their mutual interface. Unfortunately, the details of this interaction are not well understood at the atomic/molecular level.

The above discussion illustrated the effect of interfaces on the soldering process by considering the various interfacial tensions under the assumed

Table III. Interfacial tensions and contact angle as function of flux material

Flux[a]	γ_{LF} (dyne/cm)	$\gamma_{SF} - \gamma_{SL}$ (dyne/cm)	θ_c (°)
A	400 ± 20	340 ± 10	31 ± 2
B	640 ± 70	370 ± 15	55 ± 3
C	510 ± 90	370 ± 15	37 ± 2
D	420 ± 30	364 ± 7	30 ± 5
E	740 ± 90	450 ± 20	53 ± 3

[a]The base material is electropolished Kovar™; the solder is 60Sn-40Pb, 260°C.

equilibrium condition represented by Young's equation. However, the formation of a solder joint is also dependent upon the *dynamics* of the wetting and spreading activity by the molten solder. The speed with which wetting and spreading occurs is a function of the chemical reactions that take place at each of the three interfaces: (1) flux/base material; (2) flux/molten solder; (3) molten solder/base material. The rate kinetics of those reactions are a function of temperature (T) and time (t) so that the non-equilibrium condition is more aptly described by γ_{SF} (T, t), γ_{SL} (T, t), γ_{LF} (T, t) and consequently, θ_c (T, t).

Several phemenologic approaches have been developed to predict wetting and spreading rate kinetics.[15–17] *Non-reactive models* consider only the fluid properties of the molten solder while reactive models consider the formation of the solder/base material (IMC) reaction layer. The geometry must also be considered of the molten solder/base material system, such as the sessile drop configuration in Fig. 1, or the meniscus rise up a vertical plate. Gravity has a significant role in defining the shape of the molten solder surface.

Despite the numerous investigations cited above, by and large, rate kinetics studies are rather limited with respect to interface development in soldering technology. High-fidelity data that are reproducible are difficult to obtain, even in laboratory experiments. In addition, empirical studies are sensitive to the particular solder alloys, base materials, flux chemistries, and test specimen geometries, causing difficulties with generalizing one set of findings to other solder/base material/flux systems by similarity. Generally speaking, reaction rates increase with temperature. It is important to remember that, in the case of γ_{SF} (T, t) and γ_{LF} (T, t), time progression leads to an exhaustion of flux reactants that are available to support the interface reactions. Therefore, the reaction rate will decrease with time.

The solder/base material interfacial reaction [γ_{SL} (T, t)] poses a slightly different circumstance with respect to wetting and spreading rate kinetics. Once development of the interface reaction product, which is typically an IMC layer, has initiated, the value of γ_{SL} (T, t) becomes insensitive to time and temperature unless there is a change in the composition of the IMC layer at the molten solder/IMC interface. Otherwise, further thickening of the IMC layer does not affect γ_{SL} (T, t).

Probably no other phenomenon reflects the complex time-dependent interactions among the interfacial tensions γ_{SF}, γ_{LF}, and γ_{SL} more than *dewetting*. This behavior is illustrated in Fig. 3.[13,18] Figure 3a shows the schematic diagram and photograph representing the case of satisfactory wetting and spreading performance. The solder exhibits a uniform layer over the base material. Dewetting is illustrated in Fig. 3b. Wetting and spreading initially take place on the base material (1). In this example, the relatively thick solder film masked a less-than-optimal solderability condition of the base material surface (γ_{SL}) due to isolated non-wettable areas. As the molten solder continues to spread out, the layer becomes thinner (2). The non-wetted areas have an increased effect on γ_{SL}, resulting in an instability in the thin solder coating that causes it to retract into isolated mounds (3). A thin solder film may still cover, although not necessarily wet to, the non-solderable areas, depending upon the dynamics of the dewetting step. The photograph at the bottom of Fig. 3b shows dewetting by 60Sn-40Pb solder on an Fe-Ni-Co base material. Dewetting can also occur when time-dependent changes take place in the flux that lead to an increase in the value of γ_{LF}. The subsequent increase of θ_c (T, t) causes the molten solder to retract in a manner similar to Fig. 3b (iii).

Reliability: Solid-State Interface Reactions

The function of the solder joint is to provide mechanical strength, electrical conductivity, hermeticity, or, as is typically the case, a combination of these properties, toward the function of the printed wiring assembly. The performance and reliability of the solder joint depend on the bulk properties of the structures—the solder, base materials, and coatings and surface finishes—and the interfaces between them. This interdependency is illustrated by the schematic diagram of the solder joint in Fig. 4a. A Cu pin was soldered to a Ti-W/Cu/Pt/Au thin film layer on low-temperature co-fired ceramic (LTCC) base material using the 63Sn-37Pb (Sn-Pb) solder.[19] The black arrows indicate all of the interfaces present within this simple joint geometry. Under the application of a tensile load, the weaker of the bulk materials or interfaces controls the tensile strength of the interconnection. A similar premise holds true when the joint is subjected to a shear load; however, the contributions made by the individual bulk structures and interfaces become less distinguishable when the materials slide past one another—the Mode II fracture—rather than separating in the Mode I fracture geometry of a tensile test.

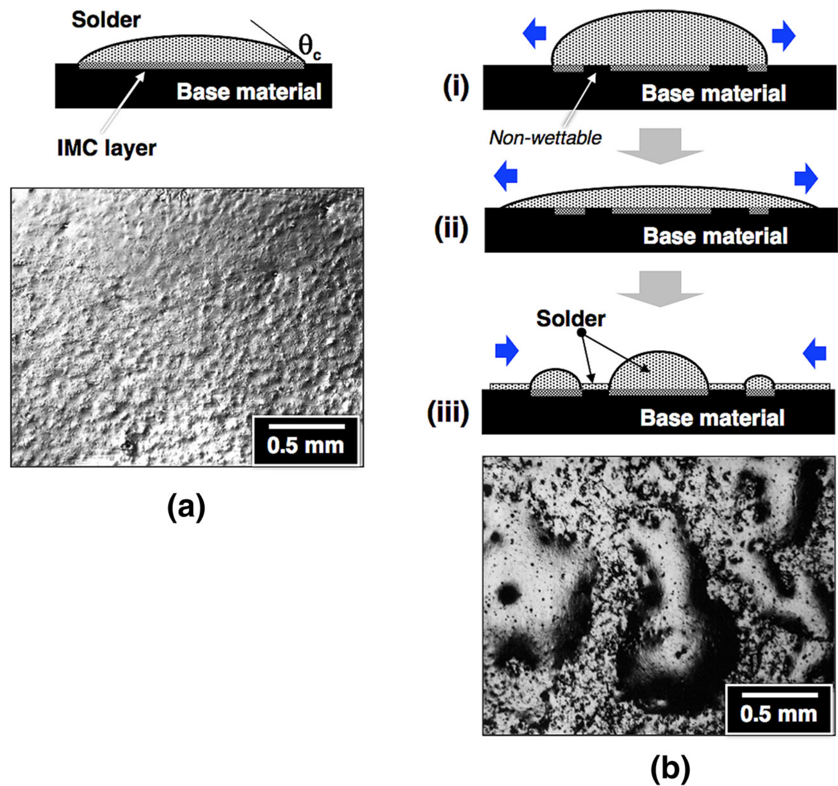


Fig. 3. Schematic diagrams and photographs illustrate the phenomenon of dewetting. (a) Photograph shows the uniform solder film that is representative of good wetting and spreading by the molten solder. (b) The schematic diagram and photographs show the sequence of steps responsible for dewetting as the molten solder film thins out over a less-than-optimally solderable base material surface. This example is based upon 60Sn-40Pb solder (260°C) that dewetted on an Fe-Ni-Co alloy surface *(portions reprinted in part with permission of the American Welding Society, Miami, FL)*.

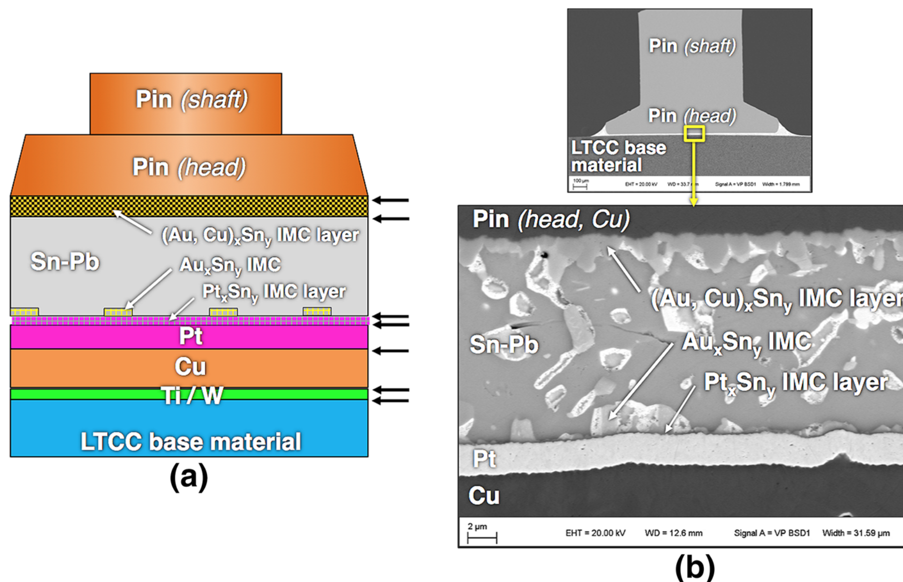


Fig. 4. (a) Schematic diagram shows a solder joint made between a Cu pin and Ti/W-Cu-Pt-Au thin layer on LTCC base material using the Sn-Pb eutectic solder. Three reaction product phases developed at the interfaces with the solder. The black arrows indicate all of the interfaces present in the joint. (b) SEM image shows the corresponding microstructure in the actual joint. The soldering parameters were 215°C for 60 s.

The physical metallurgy of one interface can affect that of the other and thus the overall reliability of the solder joint. An actual solder joint having the configuration in Fig. 4a is shown by the SEM image in Fig. 4b (not to scale). Specifically, this application illustrates the phenomenon

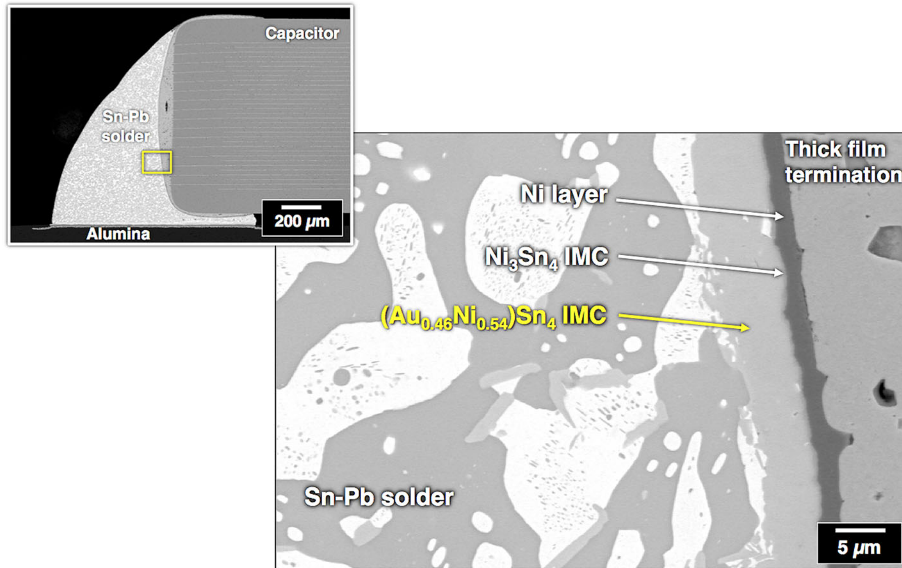


Fig. 5. SEM images show the solder joint made to the termination of a chip capacitor (inset). The high magnification image shows development of the $(Au_{0.46}Ni_{0.54})Sn_4$ IMC layer resulting from Au initially dissolved into the Sn-Pb solder that underwent solid-state diffusion back to the Ni layer.

whereby those elemental metals dissolved into the molten solder at one interface can diffuse to, and react with, the base material at the second interface and thus alter the latter's mechanical properties. The Cu pin-to-Ti-W/Cu/Pt/Au (LTCC) solder joint was made using these parameters: 215°C and 60 s. A portion of the Au layer reacted with the Sn component of the solder and formed islands of Au_xSn_y IMC along the solder/Pt interface. The rest of the latter interface was the thin Pt_xSn_y IMC layer. The remainder of the Au dissolved into the molten solder and diffused to the Cu pin where it formed an $(Au, Cu)_xSn_y$ IMC layer. The presence of the $(Au, Cu)_xSn_y$ IMC layer (thickness and coverage) increased with longer soldering times and/or higher process temperatures. Subsequent pull test data showed a *decrease of pull strength* that correlated with the increased development of the $(Au, Cu)_xSn_y$ IMC layer where the fracture occurred.

The influence of the metallurgy of one interface on that of another interface can also be observed after solidification of the solder joint. Solid-state diffusion can readily occur because, even at room temperature, the Sn-based solders are at a high homologous temperature, T_h, where $T_h = T/T_s$ (K).*

An important engineering example is based upon solid-state Au diffusion in Sn-based solders. Mei et al. and Evans et al. studied this phenomenon.[20,21] The Au protective finish, which belonged to a Ni/Au metallization, was dissolved into molten Sn-Pb solder during the assembly process. The Sn-Pb solder subsequently wets and spreads over the underlying Ni solderable layer. After solidification, Au diffused back to the Ni surface under the chemical potential to grow an $(Au_x, Ni_y)Sn_z$ IMC layer. The SEM images, which illustrate this phenomenon, are shown in Fig. 5. A 63Sn-37Pb solder joint was made between a chip capacitor and thick-film pad over alumina. The chip capacitor had an Sn-Pb protective finish over a Ni solderable layer. The thick film pad used a Ni solderable layer followed by an Au protective finish. The Au layers were dissolved into the solder. After "aging" at room temperature for several months, solid-state diffusion allowed the Au to diffuse back to both Ni solderable layers; the case of the capacitor interface is shown in Fig. 8. Electron probe microanalysis (EPMA) determined the stoichiometry of the IMC layer to be $(Au_{0.46}, Ni_{0.54})Sn_4$.[22]

A similar solid-state diffusion mechanism causes Au to return to a Cu base material after having been dissolved in molten Sn-Pb solder. In a study performed by Susan et al., Cu-to-Cu solder joints were fabricated with Sn-Pb and Sn-Ag-Cu solders having Au concentrations of 0 wt.%, 2 wt.%, 4 wt.%, and 8 wt.%.[23] Two IMC layers were formed at the interface. The layer adjacent to the solder had the $(Cu, Au)_6Sn_5$ stoichiometry, and the second layer, which formed between the first layer and the Cu base material, had the Cu_3Sn concentration. The Au concentration increased from 0 at.% to 14 at.% in the $(Cu, Au)_6Sn_5$ layer with increased Au content of the solder; however, Au was not observed in the Cu_3Sn layer. The effect of Au on the growth rate kinetics also differed between the layers; it enhanced growth of the $(Cu, Au)_6Sn_5$ layer and

*For example, 63Sn-37Pb solder has a solidus of 183°C (456 K). At room temperature, 23°C, (298 K), T_h = 298/456 = 0.65. By comparison, at the same T_h of 0.65, a Ni-based superalloy having a T_s = 1400°C (1673 K) is being exposed to a service temperature of 0.65 (1673 K) = 1087 K, or 814°C, which is equivalent to the hot section temperatures of an operating jet engine.

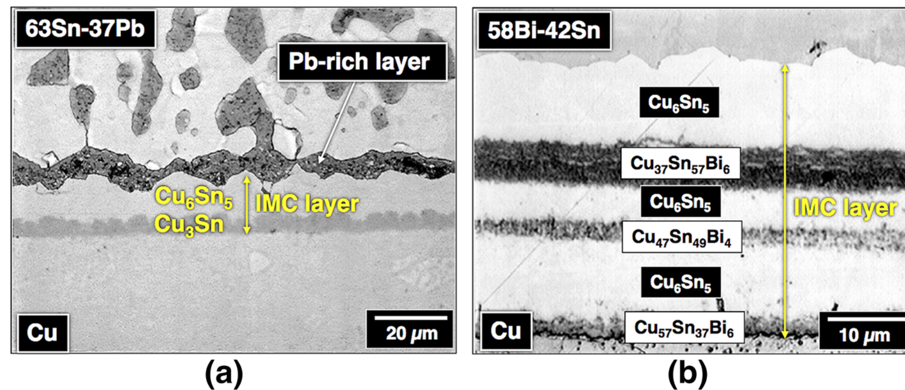


Fig. 6. (a) Optical micrograph shows formation of the IMC layer between 63Sn-37Pb solder and Cu base material after solid-state aging at 135°C for 40 days. Lead (Pb) accumulated at the solder/IMC interface. (b) Optical micrograph shows the IMC layer that developed between 58Bi-42Sn solder and a Cu base material following solid-state aging at 120°C for 40 days. The rejected Bi formed Cu-Sn-Bi layers between the Cu_6Sn_5 layers.

suppressed that of the Cu_3Sn layer compared with joints having zero Au content in them.

Solid-state diffusion processes control the development of the interfacial IMC layer and, as such, the long-term reliability of the solder interconnection. Often, the interface reactions do not include all of the solder or base material constituents in the reaction. Figure 6a shows the interface microstructure that developed following aging of the common 63Sn-37Pb/Cu couple at 135°C for 40 days.[24] The Pb component of the solder does not participate in the reactions that form the Cu_3Sn and Cu_6Sn_5 IMC layers; therefore, it accumulates as a Pb-rich layer along the solder/IMC interface. The Pb-rich layer is a mechanically weaker structure and can become the preferred path of crack propagation in the solder joint.

The formation of more complex IMC layers is exemplified by the interface microstructure that forms between the 58Bi-42Sn solder and Cu base material.[25] Figure 6b shows the interface microstructure that formed after solid-state aging at 120°C for 40 days. The IMC reaction occurred specifically between the Sn component of the solder and Cu base material. The Bi constituent was rejected from the reaction; it accumulated into Cu-Sn-Bi layers that formed between layers of the traditional Cu_6Sn_5 phase. The Cu-Sn-Bi layers, whose compositions were determined by EPMA, were relatively brittle and readily susceptible to crack propagation.

The solid-state reaction rates can also have a profound effect on the interface microstructures. As the reaction rate increased, minor differences in diffusion rates of the various constituents can become amplified to the extent that Kirkendall voids develop as a result of the mass flow imbalance across the interface. This point is exemplified by the solid-state IMC development in couples between the 95.5Sn-3.9Ag-0.6Cu solder and Cu base material.[26] Figure 7a shows the IMC layer that formed after aging at 135°C for 300 days. Both Cu_6Sn_5 and Cu_3Sn stoichiometries were created along the interface. However, when the aging temperature was increased to 205°C, the faster diffusion rate of Cu versus Sn became accentuated at the Cu_3Sn/Cu interface. As shown in Fig. 7b, Kirkendall voids formed along the Cu_3Sn/Cu interface that collected together to create the observed porosity. Such extensive pore development would compromise the functional integrity of the interface. At locations along the interface where porosity did not develop, the Cu_3Sn continued its growth into the Cu base material, having a “plume” geometry. Figure 7b schematically illustrates both pore and plume development mechanisms.

The purity of the base material can have a significant effect on the propensity for Kirkendall voids to develop at the IMC/base material interface. Electroplated Au provided the means to illustrate this behavior.[27] An application resulted in an interface microstructure between the 50In-50Pb (wt.%) solder and pure Au (100Au) electroplated layer (over a Cr adhesion layer and evaporated Au seed layer). This electroplated Au layer had a very low contaminant level. The joint was aged at 100°C for 288 h, resulting in formation of the Au_9In_4 layer adjacent to the remaining Au layer and (Au, Cu)In_2 + Pb IMC layer next to the solder field. Kirkendall voids were *not* observed along the interfaces. However, when the solder joint was made to an electroplated Au layer having a high contaminant level, the Au_9In_4 IMC layer was not observed in the joints. More so, significant void development took place along the interface between the Au (base material) and (Au, Cu)In_2 + Pb IMC layer. This microstructure is shown in Fig. 8. The hypothesis was made that the reduced purity of the electroplated layer hindered the driving force and thus the diffusion rate of In toward the Au layer. A relatively high diffusion rate of Au toward the 50In-50Pb solder was retained, resulting in Kirkendall void

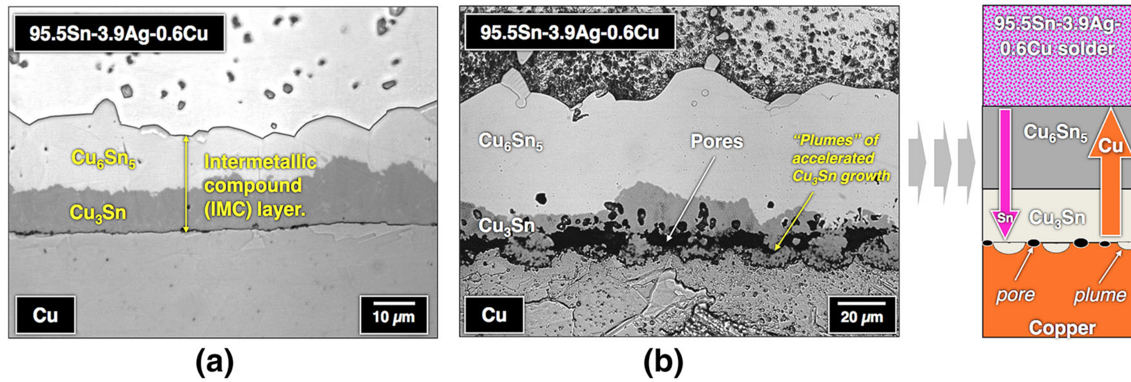


Fig. 7. (a) SEM photograph shows development of the Cu_6Sn_5 and Cu_3Sn IMC layers at the interface between the 95.5Sn-3.9Ag-0.6 solder and Cu base material after solid-state aging at 135°C for 300 days. (b) SEM photograph documents the Kirkendall porosity and growth "plumes" that formed along the Cu_3Sn/Cu interface after very accelerated aging at 205°C for 300 days. The diagram at right schematically illustrates the latter phenomena.

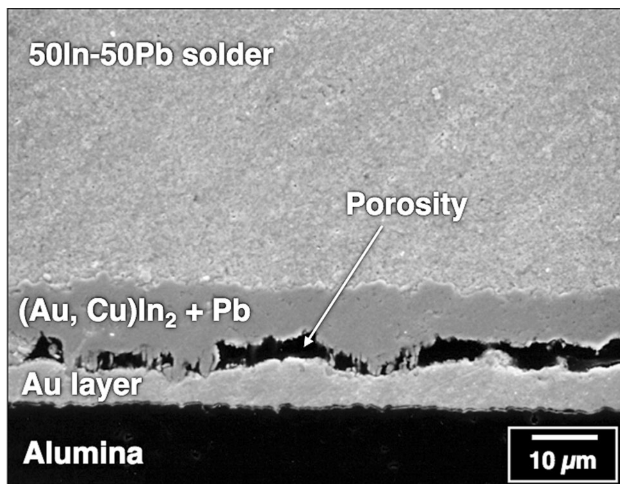


Fig. 8. SEM image shows the development of the interface IMC layer between 50In-50Pb solder and an electroplated 100Au layer after aging at 100°C for 288 h. The Au layer was heavily contaminated with organic compounds, which altered the relative diffusion rates between Au and In.

formation that led to the extensive porosity in Fig. 8. The porosity was the root cause of the poor mechanical strength observed in these joints.

Solder interconnections are mechanically tested in the *tension, compression,* or *shear mode*. The *peel test* is a variant of the tension test whereby the load is applied over a linear dimension rather than over an area. Interfaces are particularly sensitive to tensile loads whether the latter is applied by the pull test or the peel test. In case of complex structures such as solder joints, the tension test provides the means to more accurately assess the mechanical performance of the joint because the load is applied equally across *all* materials and interfaces. Also, fracture surface analysis is simplified because there is not the damage caused by surfaces sliding past one another as is the case of the shear test.

Whether the methodology is a tensile test or a shear test, the *plane strain* effect must be considered with respect to the solder joint geometry.[28] The predominance of the plane strain condition or its counterpart, the *plane stress* condition, is a critical factor with respect to the role played by interfaces on the mechanical properties of the solder joint. When the solder joint gap is thick relative to the solder joint area, the plane stress condition dominates, and deformation readily occurs in the (bulk) solder under either a tensile or shear load. The fracture strength can be estimated by the strength of the bulk solder divided by the load bearing area. However, as the gap is reduced, increasing constraint is placed on deformation in the solder. The solder appears to be *stronger* than would be predicted from its bulk strength properties. This circumstance reflects the plane strain condition.

The degree to which plane strain, plane stress, or a mixture of the two conditions prevails in a solder joint is a function of these variables:

a. the gap thickness;
b. the joint area (footprint);
c. mechanical properties (yield stress, strain hardening/softening exponent, etc.) of the solder;
d. the deformation rate.

The plane strain condition is favored by the following circumstances: (1) *small* gap thickness; (2) *large* joint area (footprint); (3) *high yield stress* and/or *rapid strain hardening*; (4) *fast* deformation rate. The opposite trends favor the plane stress condition. The plane strain/plane stress effect has less significance under the slow strain rates of time-dependent deformation (creep) that dominates *low-cycle fatigue (LCF)*, including *thermal mechanical fatigue (TMF)*. Under TMF conditions, deformation occurs preferentially in the solder but near the interface because of a stress-concentration effect created there by the material change between the solder and base material.

The plane strain condition dominates high strain rate events such as (1) stress-strain tests, (2) high-cycle fatigue (HCF), which includes vibration

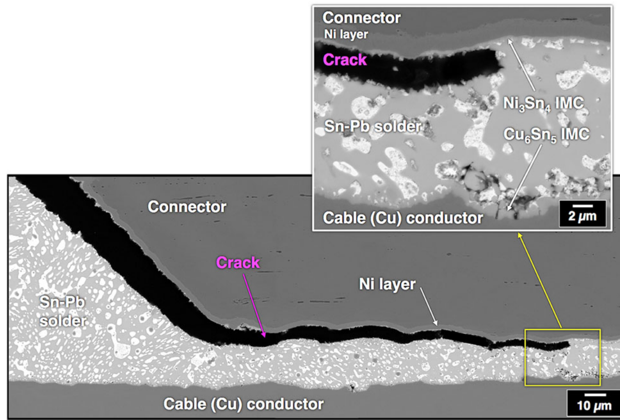


Fig. 9. SEM images show crack propagation in a connector solder joint caused by excessive bending of the cable (outer) conductor. The high-magnification inset image shows failure in the Ni_3Sn_4 IMC layer.

conditions, or (3) mechanical shock loads. The seemingly stronger solder forces deformation and cracking to develop at the solder/base material interface, often in the IMC reaction layer. This case is exemplified in Fig. 9. The SEM photographs show the failure of the Sn-Pb solder joint made between a connector and cable conductor. The overload event was caused by subjecting the two structures to an excessive bending moment. The fracture path occurred in the Ni_3Sn_4 IMC layer. The IMC layer is also the fracture path under the high-cycle fatigue (HCF) conditions that characterize shock and vibration environments. The higher strain rates, coupled with the rapid strain hardening of Sn-based solders, force the failure to occur in the IMC layer at the interface.

The SEM images in Fig. 9 also illustrate the important point that the mechanical performance of the interface is also dependent upon the mechanical properties of the IMC phase(s). The fracture path occurred preferentially in the Ni_3Sn_4 IMC layer of the connector rather than in the Cu_6Sn_5 IMC layer of the cable conductor. The Ni_3Sn_4 IMC is more brittle than the Cu_6Sn_5 IMC and, as such, is more susceptible to failure under a relatively high strain rate deformation.[29]

The following application illustrates the point that an interface failure can be affected by multiple materials processes. In this instance, the IMC layer controlled the interface failure despite the relatively slow strain rate of TMF.[30] The inset micrograph of Fig. 10a shows a PBGA solder joint. The interconnection had undergone 750 thermal cycles (– 55°C/125°C; 10-min hold times; and 10°C/min ramp rates). The high-magnification image highlights the interface between the Sn-Pb solder and Ni layer on the Cu pad belonging to the interposer of the PBGA. The interface microstructure was comprised of the Ni_3Sn_4 IMC layer, $(AuNi)Sn_4$ IMC layer, and Pb-rich layer.** The $(AuNi)Sn_4$ IMC layer resulted from Au returning to the Ni layer by solid-state diffusion. The Pb-rich layer resulted from Pb rejected by growth of the $(AuNi)Sn_4$ IMC layer. The slow strain rate, coupled with the relatively large solder joint “gap” of 1.0 mm, would certainly predict a plane stress condition. However, fracture occurred catastrophically along the Ni/Ni_3Sn_4 IMC interface under these test conditions. The root-cause analysis determined that failure was caused by a change in the local stress concentration condition that resulted from the development of the additional $(AuNi)Sn_4$ IMC layer.

A second pre-mature failure mode resulted from formation of the $(AuNi)Sn_4$ IMC layer. The details of the phenomenon are different, although the consequence was the same: shortening the lifetime of the interconnection. See Fig. 10b. On the same package, a majority of the solder joints failed early because of an acceleration of crack growth in the Pb-rich layer that formed as a result of the development of the $(AuNi)Sn_4$ IMC layer.

Clearly, as solder joint size continues to decrease, the properties and thickness of the IMC layer will have a greater role in the overall performance and reliability of the interconnections. It is possible that the IMC layer will control both the TMF and the shock and vibration performance of miniaturized solder joints; the bulk solder properties will become a lesser contributor to solder joint properties.

COATINGS AND FINISHES

Coatings and finishes are being used to a greater extent as the means to improve the solderability of new base materials used in electronic packaging applications. As such, consideration must be given to the performance and long-term reliability of the additional interfaces that coatings and finishes introduce into the interconnections. This report cannot provide a detailed treatise of all coating and surface finish technologies. Therefore, a brief “primer” is provided, which describes those technologies having the broadest range of applications in electronic packaging. Those technologies are: (1) physical vapor deposition, (2) plating processes, and (3) thick film layers. The discussion will focus on the resulting interfaces and their effect on solder joint processibility and reliability.

The important aspect of these technologies, or any coating or surface finish methodology, is that each layer introduces into the interconnection not only its properties, *but also those of the two additional interfaces. Both structures will affect the processability as well as long-term reliability of the interconnections.*

Physical Vapor Deposition

The two most commonly used physical vapor deposition (PVD) methods are *evaporation* and *sputtering*. Evaporation is largely an intrinsic property of the metal based upon the latter’s heat of

**The EPMA technique was used for the $(AuNi)Sn_4$ stoichiometry.

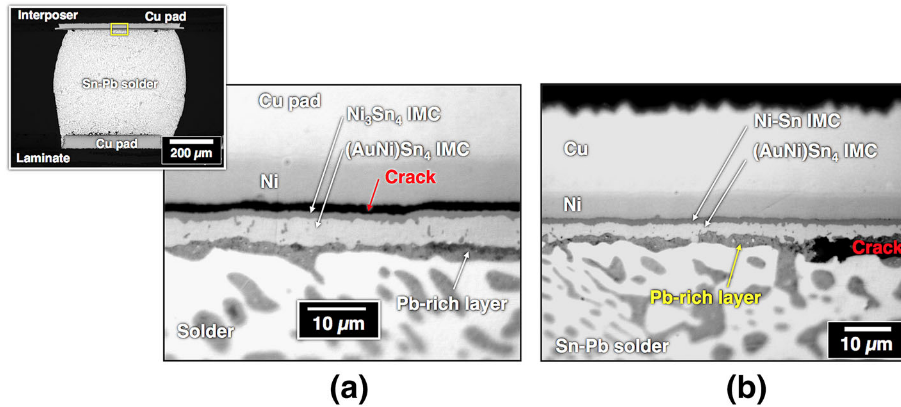


Fig. 10. (a) Inset optical micrograph shows a PBGA solder joint after completing 750 cycles of TMF deformation (− 55°C/125°C; 10 min hold times; 10°C/min ramp rates.) The high magnification image shows the interface microstructure, which included the Ni_3Sn_4 IMC layer; the (AuNi)Sn_4 IMC layer after Au diffused back to the Ni layer; the Pb-rich layer. Crack formation was observed along the Ni_3Sn_4/Ni interface. (b) Optical micrograph shows a second joint in which the TMF crack propagated in the Pb-rich layer that formed as a consequence of the formation of the (AuNi)Sn_4 IMC layer.

vaporization and melting temperature. Therefore, the deposition rate is controlled by (1) the source temperature (above melting) and (2) proximity of the target surface to the source. The evaporation of multi-component sources is difficult to control because the vaporization of each constituent is determined primarily by its individual heat of vaporization and melting temperature. However, associated residual stresses in the film are not readily controlled by process parameters. If the residual stresses become excessive with increased thickness, spalling or delamination can occur, leading to a failed interconnection.

The thickness of the coating is theoretically unlimited under evaporation. However, evaporated layer thicknesses are generally limited to less than a few microns and are most typically in the range of 10–100 nm to avoid high residual stresses and excessive material waste. The adhesion of evaporated films is sensitive to contamination of the base material surface. The photograph in Fig. 11 shows an instance of the delamination (red arrows) by an evaporated Ti-Cu-Pt-Au thin film from the surface of a low-temperature, co-fired ceramic (LTCC) base material caused by excessive surface contamination.

Sputtering offers a wider process window than does evaporation by providing the means to adjust deposition rates to control residual stresses in the coatings and optimize interface adhesion. Because the sputtering process is largely based upon the mechanical dislodgement of atoms from the source, multi-component (alloy) film compositions can be deposited on the targeted base material surface that closely replicate the source (alloy) composition.

Sputtered coatings are generally less than several microns thick for most packaging applications. However, thicker layers can be readily deposited without a risk of overheating the base material. Sputtered atoms impact the base material surface with a greater degree of kinetic energy. That energy

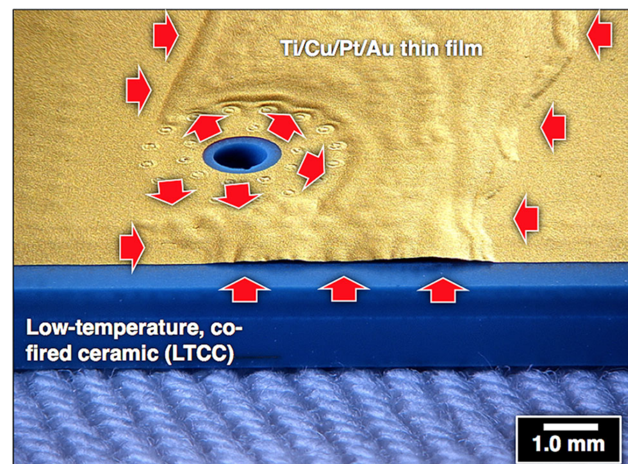


Fig. 11. Photograph shows the delamination (red arrows) of a Ti/Cu/Pt/Au thin film from the surface of a low temperature co-fired ceramic (LTCC) base material caused by excessive surface contamination.

produces an etching effect that removes surface contaminants during the deposition process as well as promotes adhesion.

Metallographic cross sections are used to provide images of thin films and associated interfaces. Sample SEM photographs are shown in Fig. 12. The inset image is an SEM photograph taken in the secondary emission (SE) mode that shows the Sn-Pb solder joint made to a Ti/W-Cu-Pt-Au thin film evaporated on the low-temperature, co-fired ceramic (LTCC) base material. The soldering process dissolved away the Au layer. The high-magnification, SEM-backscattered electron (BSE) image nearly provides the optimum resolution that can be obtained from a metallographic cross section and an SEM operating at its highest magnification. Although those pictures provide important information about the interfaces, they illustrate the need for

higher resolution to examine the finer details of interface structures.

Higher fidelity can be realized by using the focused ion-beam (FIB) cross sectioning process. The Ti/W-Cu-Pt-Au thin film, but without the solder joint, is shown in Fig. 13. The FIB process highlights the mutual interface (blue arrows) between the Cu and Pt layers as well as their individual layer microstructures. The high magnification image confirmed excellent adhesion at the interfaces between the Ti/W and Cu layers as well as the Ti/W/LTCC interface (magenta arrows). Atomic-level details of the interface would require the use of transmission electron microscopy (TEM).

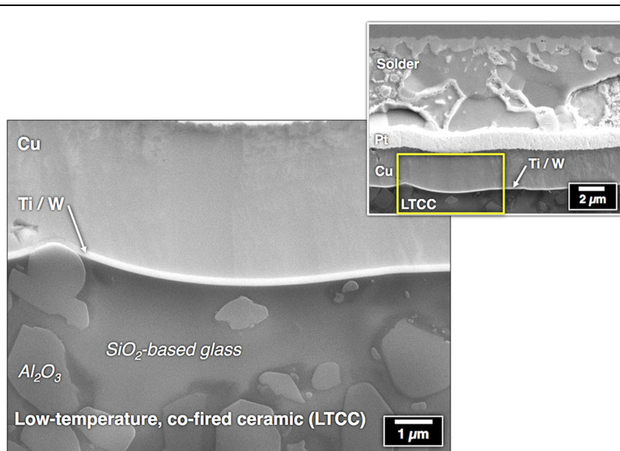


Fig. 12. Photographs illustrate the upper resolution limits provided by metallographic cross sections and SEM imaging when examining thin film layers and associated interfaces. Interest was given to the integrity of the interface between the Ti/W adhesion layer and the LTCC base material, specifically at the SiO_2 glass phase.

Plating Processes

Plating (or "wet deposition") processes used in electronic packaging applications can be placed into three categories: (1) electro- (galvanic) plating, (2) electroless (autocatalytic) plating, and (3) conversion ("immersion") plating. As noted previously, many excellent review papers have been written on each of these three topics. Electroplating is used on both structural parts—e.g., lead frames, pins, and so on—as well as printed circuit board features. In the case of lead frames, a Ni solderable layer is plated on iron-alloy frame materials to improve solderability. Typical Ni thicknesses are 1.3–3.8 μm. Nickel layers are also placed over Cu frame surfaces, not only to assure consistent solderability performance, but to also serve as a diffusion barrier between Cu and the most-often used protective finish, Au. The Au protective finish is deposited on the Ni layer to prevent the latter's loss of solderability due to oxidation. The typical Au thickness is 1.3–2.5 μm. All surfaces must be electrically connected to form the continuous anode needed to receive the metal cations.

Electroless and conversion ("immersion") processes do not require an interconnection between to-be-plated surfaces because the anode is created by the bath chemistry at each site of the base material. Temperature, pH, and the optimization of buffers allow the electroless process to achieve thicknesses of several microns, which are similar to electroplating methods. However, layer thicknesses are somewhat more limited because of

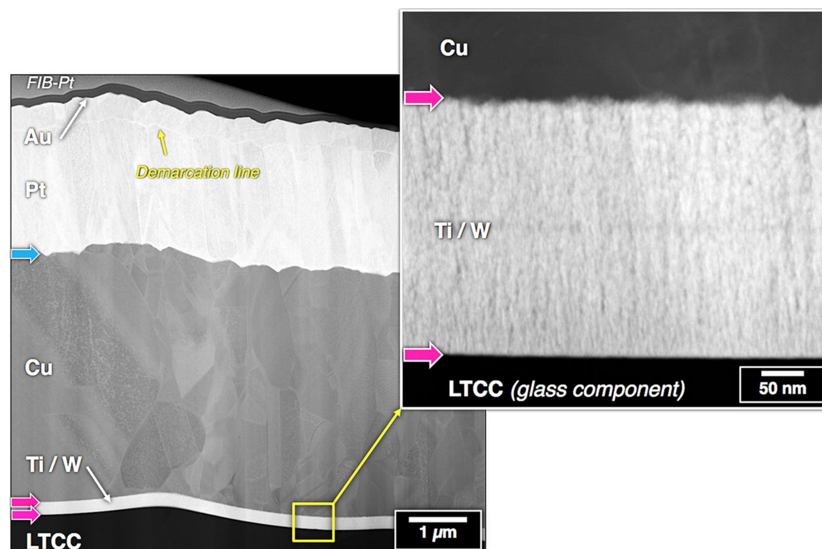


Fig. 13. High-resolution SEM images were obtained at nearly an order-of-magnitude higher magnification using the focused ion-beam (FIB) cutting technique versus standard metallographic cross-section techniques. Critical interfaces included those between: the Ti/W layer and LTCC, the Ti/W and Cu layers (magenta arrows), and Cu/Pt interface (blue arrows).

charge build-up and the change to the base material surface (atoms) with coating development that alters the local chemistry. The critical facet of electroless plating is surface activation of the base material needed to catalyze the electroless reaction. Poor surface activation will result in inconsistent layer thicknesses and poor adhesion properties at the interface.

The immersion plating process is used primarily in electronic packaging. There is the immersion Sn protective layer that is placed on Cu conductor features. The second application is the deposition of an immersion Au protective layer on an electroless Ni solderable layer that is over the Cu conductors of the printed circuit board—this configuration forms the *ENIG* surface finish. The third application has an immersion Au protective finish deposited on an electroless Pd layer (also a protective finish), which covers the electroless Ni solderable layer over the Cu, printed circuit board features. This geometry is referred to as the *ENEPIG* finish.

Immersion coatings are especially thin because the layers are deposited by a replacement process. That is, the base material surface atoms are replaced with the immersion coating atoms. Once all of the base material surface atoms have been replaced with coating atoms (e.g., Au), the reaction comes to a halt. Typical immersion layer thicknesses are several tens of nanometers. The FIB ion milling process is required to make cross sections that can be viewed by SEM. The SEM image in Fig. 14 shows an ENEPIG finish that was deposited on a Cu pad (not shown). The electroless Pd and Ni layers as well as the immersion Au layer are identified in the photograph. Also, the interfaces, which provide robustness to the finish, are indicated in the image: the Au/Pd interface (blue arrow) and the Pd/Ni interface (magenta arrow). Although not shown in this image, an excellent interface was formed between the electroless Ni layer and Cu pad to assure good adhesion of the overall ENEPIG finish.

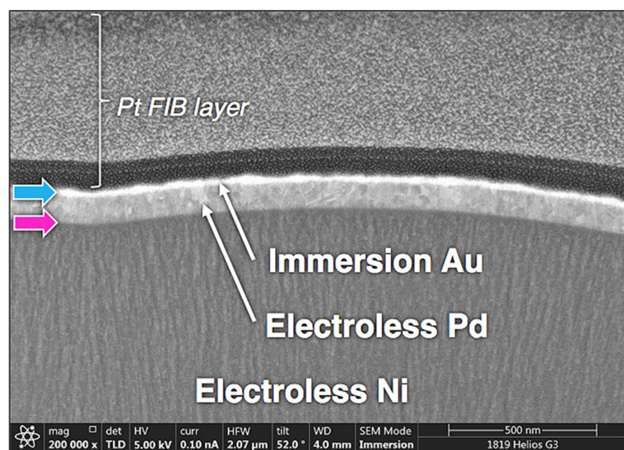


Fig. 14. The SEM image shows a FIB cross section made to an ENEPIG finish on the Cu pad (not shown) of a printed circuit board. The microstructure can be discerned of the 100-nm Pd layer in this SEM photograph. Also, the Au/Pd interface (blue arrow) and Pd/Ni interface (magenta arrow) were shown to have excellent integrity in these images.

Thick Film Layers

Thick films are used in soldering technologies, including the lid sealing of hermetic packages and defining the conductor pattern (traces and pads) of hybrid microcircuits (HMCs). An HMC is a printed circuit made on ceramic base materials rather than on laminate printed circuit boards. Ceramic base materials include alumina, aluminum nitride, and both low- and high-temperature co-fired ceramics (LTCC and HTCC, respectively). Thick films are constructed from a number of elemental metals and alloy combinations. Precious metals as well as noble metals and alloys, including Ag, Ag-Pd, Au, and Au-Pt-Pd, are used most frequently in electronic packaging applications. The advent of base metal electrode (BME) capacitors is increasing the demand for the Cu and Ni thick-film materials used in their construction. Refractory metal thick films such as Mo, W, and Mo-Mn are also used in electronic packaging; however, they are unsolderable and, as such, require the addition of solderable and protective layers on top of them to support a soldering process.

References 31 and 32 provide details on the fundamental aspects of thick film technology. The current discussion examines the interfaces of interconnections made to thick film layers on ceramic base materials. The 76Au-21Pt-3Pd (wt.%) thick film (abbreviated Au-Pt-Pd) will be exemplified here; it is shown in Fig. 15a, where it had been fired to an alumina substrate. The glass phase layer, which is very thin, bonds the porous metal layer to the ceramic along their mutual interface. A portion of the glass phase also diffuses into the ceramic below the interface.

The incomplete sintering of the metal particles, combined with the movement of the glass phase to the metal/ceramic interface, creates the porosity within the thick film layer. The degree of porosity is a function of the metal composition as well as the firing conditions. Molten solder penetrates the thick film through the highly interconnected pores as shown in Fig. 15b.

The porosity of thick films presents an interesting problem with respect to the role of interfaces on the processing and long-term reliability of accompanying solder interconnections. The porosity significantly increases the interface area over which the solder reacts with the thick film. The consequence is an acceleration of the reactions between them by three to four fold compared with an interface generated by a similar solder and a *sheet* base material having the same Au-Pt-Pd composition.[33]

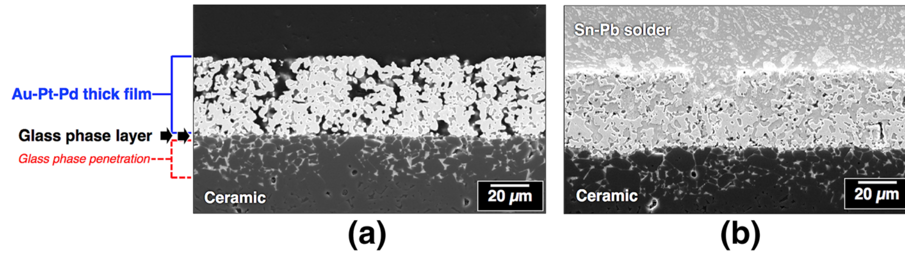


Fig. 15. SEM photograph shows the microstructure of the Au-Pt-Pd thick film layer on an alumna ceramic base material: (a) the as-deposited condition and (b) after soldering with the eutectic Sn-Pb alloy.

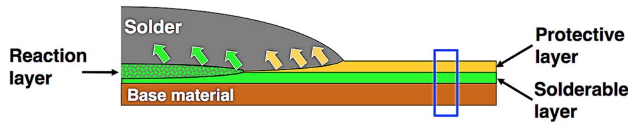


Fig. 16. Schematic diagram illustrates the configuration of the protective and solderable layers atop the base material. The as-deposited configuration occurs at the blue rectangle. The fate of the two layers is shown for the wetting and spreading of the molten solder. The final joint is made to the solderable layer.

Soldering Applications Using Coatings and Finishes

Several applications are exemplified in which coatings and finishes are the used soldering technology. The discussion will emphasize the accompanying interfaces and their role in both processes as well as the long-term reliability of the interconnections.

Coatings and finishes enhance the wetting and spreading of difficult-to-solder base materials (e.g., Al, Fe-Ni-Co alloys, ceramics, etc.) or improve the solderability of nominally solderable base materials to increase production throughput. Referring to Fig. 1 and Eq. 1, coatings improve solderability by increasing the difference, $\gamma_{SF}-\gamma_{SL}$, by increasing γ_{SF}, decreasing γ_{SL}, or both. Coatings and finishes are most successful by increasing γ_{SF}, particularly when the base material is difficult to solder because of a tenacious oxide layer.

The surface finish approach used most frequently in electronic packaging is the combination of a *solderable layer* and a *protective layer*. The schematic diagram in Fig. 16 illustrates this configuration. Referring to the blue box that indicates the as-deposited configuration, the solderable layer is deposited on the base material. *The interconnection will ultimately be made between this layer and the solder.* The protective finish is placed over the solderable layer to “protect” the latter’s solderability by preventing surface oxidation. Clearly, the solderable layer must be adherent to the base material at their mutual interface *at all times*. The protective layer must adhere to the solderable layer until it is fully dissolved into the molten solder.

Some applications do not require the solderable layer. Rather, they need only the protective finish to preserve the solderability of the base material surface.

The schematic diagram in Fig. 16 describes the fates of the protective and solderable layers during the soldering process. Initially, the protective finish must also be solderable to allow for wetting and spreading by the molten filler metal—a flux will assist with this step by eliminating any oxide on the protective finish surface and by lowering the solder-flux interfacial tension. The protective layer is fully dissolved into the molten solder after which the solder wets the solderable layer with a reduced degree of dissolution. The joint is completed by the formation of a reaction layer along the solder/solderable layer interface. The flux does *not* assist directly with the solderability of the solderable layer—so, the latter surface *must be solderable* by being free of oxidation or other contamination.

The thickness of the protective layer determines the extent to which the solder composition is altered during the process. An excessive “contamination” of the molten filler metal by the dissolved protective finish can potentially lead to constitutional solidification that prevents a full completion of the joint configuration.

The most commonly used solderable layer/protective layer methodology is the nickel (Ni)/gold (Au) system. Nickel serves as the solderable layer; Au is the protective layer (Fig. 16). Although critical to the success of many electronic packaging applications, the Ni/Au layer also poses an increased risk to reliability based on the Au dissolution process—the defect mechanism is *Au embrittlement*. There are two embrittlement scenarios. The usual concern is that of *bulk embrittlement* caused by the presence of $AuSn_4$ particles in the solder. As the concentration of $AuSn_4$ phase increases, it imparts its brittle mechanical properties to the solder joint, resulting in an increased susceptibility to crack development. An example of this scenario is shown in Fig. 17a.

However, the greater risk of solder joint failure does not necessarily arise from bulk embrittlement. Instead, catastrophic interface failures have been observed when the Au protective layer is *not* completely dissolved away during the soldering process. This phenomenon is illustrated by the optical micrograph in Fig. 17b. An Sn-Pb solder joint was made to two base materials in a connector

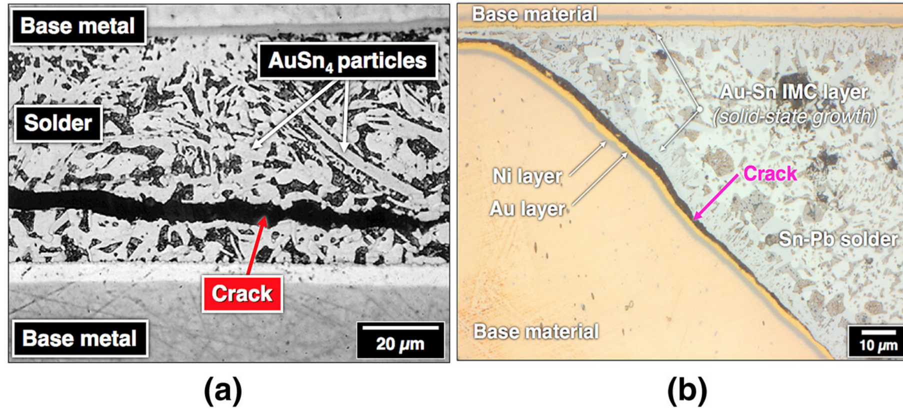


Fig. 17. (a) Optical micrograph shows crack propagation in a Sn-Pb solder joint that was embrittled by the dissolution of Au and formation of the $AuSn_4$ particles. (b) Crack formation occurs along the Au/$AuSn_4$ interface created by *solid-state* reaction when the Sn-Pb soldering process failed to dissolve away all of the Au protective layers from the base materials.

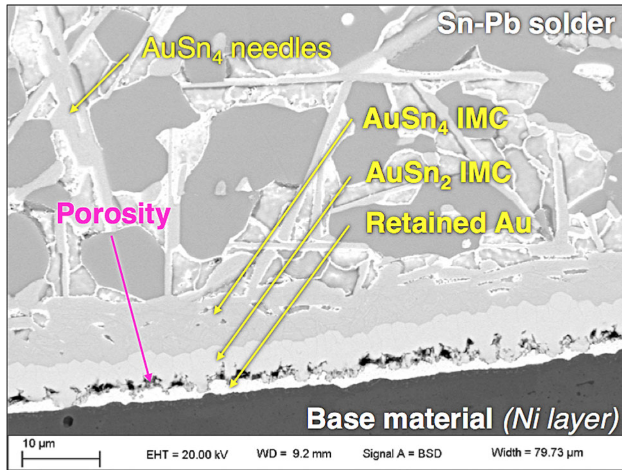


Fig. 18. SEM photograph shows Kirkendall voids caused by solid-state growth between the retained Au layer and Sn-Pb solder. Void development occurred specifically between the $AuSn_2$ layer and remaining Au layer.

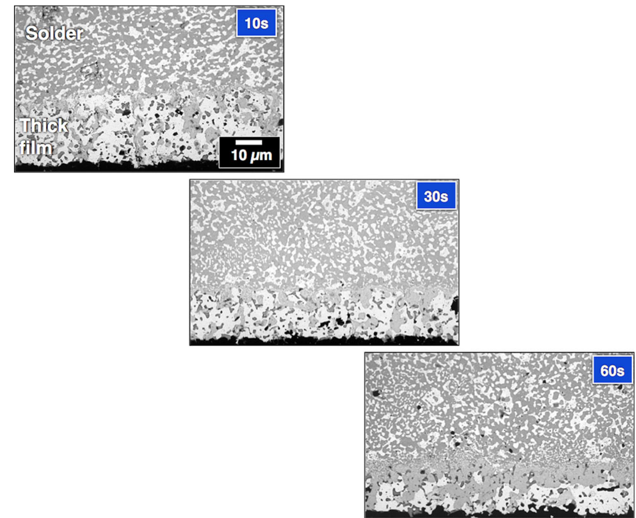


Fig. 19. Series of SEM images illustrate dissolution of the Au-Pt-Pd thick-film layer by 63Sn-37Pb solder at 240°C and time durations of 10 s, 30 s, and 60 s. The IMC stoichiometry was (Au, Pt, Pd)Sn_4, with the Au, Pt, and Pd having the same relative concentrations as in the original thick film composition.

structure having the Ni/Au surface finish. The Au protective layer was not completely dissolved during the soldering process. The cause for this defect can be either too thick an Au layer or too short a soldering process that did not fully dissolve the Au layer. After solidification, the Au-Sn IMC layer developed further, but this time, by *solid-state diffusion and reaction processes* at room temperature. A weak interface forms between the remaining Au layer and the newly developed solid-state Au-Sn IMC layer. A nominal bending load resulted in the formation of a crack that led to a catastrophic fracture of the solder joint.

The root cause for the weakened Au/$AuSn_4$ (solid-state) interface was determined in a second application having an Sn-Pb lap shear joint that was made between two Ni/Au plated leads. A high-magnification SEM image is provided in Fig. 18 that shows the details of the interface microstructure that resulted from the incomplete dissolution of the Au protective layer. The $AuSn_4$ and $AuSn_2$ layers formed between the solder and the retained Au layer under solid-state diffusion processes. Vacancies developed at the $AuSn_2$/Au interface because of the mass transport imbalance between Au and Sn. Gold diffuses faster toward the solder than Sn can diffuse to the $AuSn_2$/Au interface. The vacancies collect at the interface, creating Kirkendall voids that grow into the porosity that subsequently weakens the interface. This case is illustrative of the coupling of the soldering process and the subsequent joint reliability through a changing interface microstructure.

Thick film layers present interesting interface phenomena due to their porosity and infiltration by the (molten) solder (Fig. 15). Interface reactions are

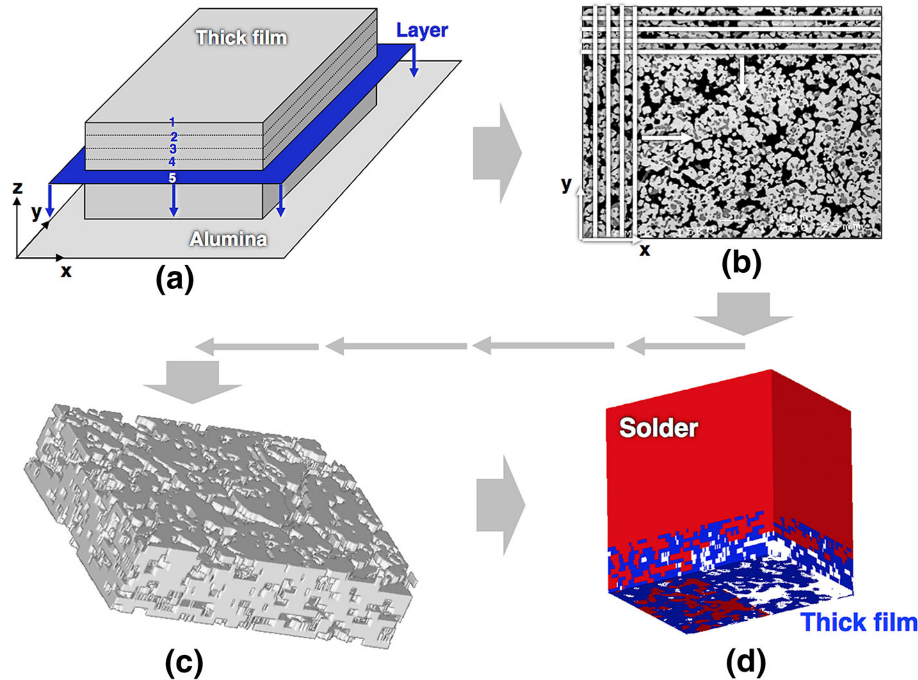


Fig. 20. Images show development of the three-dimensional (3D) model for the Au-Pt-Pd thick-film layer: (a) serial cross sections performed on an actual thick film layer; (b) the mapping of the serial sections (white, metal and black, voids); (c) creating the 3D computer simulation from stacking the 2D layers; (d) allowing solder to fill the porosity as the initial condition (solder, red; thick film, blue; unfilled voids, white).

accelerated between the solder and thick film material during the soldering process as is solid-state IMC growth when the joint is in service. It is clear that pore size distribution and interconnectedness are geometric variables that affect those reactions and, as such, the resulting interface microstructure.

First, the discussion will address the effect of the molten solder. This behavior is illustrated in Fig. 19, which shows Au-Pt-Pd thick-film dissolution by molten Sn-Pb solder (240°C) as a function of exposure time.[34] The IMC stoichiometry was (Au, Pt, Pd)Sn_4. The Au, Pt, and Pd retained the same relative concentrations in the IMC as they were in the original thick-film composition. The geometric effect posed by porosity must be addressed to accurately predict the interface microstructure between the solder and thick film layer. Computational modeling provides the means to do so.

The construction of such a computational model is shown in Fig. 20. The model was applied to eutectic Sn-Pb solder and the Au-Pt-Pd thick film, although it can be applied to any solder/thick film system. Serial cross sections were performed through a thick film layer (a). At each level, a 2D computer mapping was created of the thick film-plus-pore structures (b). The 2D maps were stacked upon one another and stitched together to create the 3D structure (c). The solder was allowed to infiltrate the thick film through surface and interconnected pores to generate the initial soldered condition (d). The solder is red; the unreacted thick film is blue; the unfilled pores are white.

A description of the model for liquid solder reaction begins by referring briefly to the simpler 2D geometry shown on the left-hand side of Fig. 21. The initial condition is at the top whereby the Sn-Pb solder (light blue) was allowed to infiltrate the Au-Pt-Pd thick film (green), but not yet react with it. The white blocks represent unfilled pore space. The bottom image shows the progression of the molten eutectic Sn-Pb solder reaction at 240°C after 15 s. The IMC is in the red color. *The color gradient represents the interface between the molten solder (blue) and IMC (red)—the numerical routine required it to be a gradient to avoid singularity faults.* The color of the unreacted thick film color was changed to blue when the model began its execution—also an artifact of the numerical code. The interface reaction and diffusion equations were constructed from empirical data collected by experiments performed on Sn-Pb solder/Au-Pt-Pd wrought sheet test couples. A significant area of IMC has formed at the expense of a small amount of the Au-Pt-Pd thick film because if the difference between their respective specific volumes. Also, less reaction took place on the lower half of the thick film because the latter is denser—that is, it has less porosity—so that there is a reduced interconnectedness between pores than in the top half portion of the thick film layer. The model predictions were validated by empirical data similar to those shown in Fig. 19.

The 3D dissolution behavior is shown on the right-hand side of Fig. 21. The structure is magnified to more clearly show the reaction. The initial

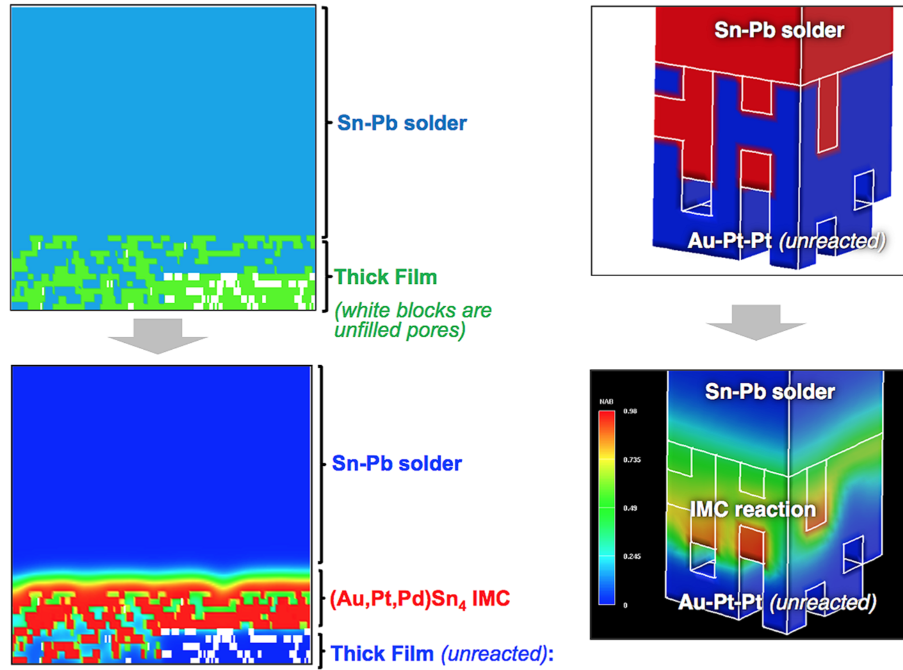
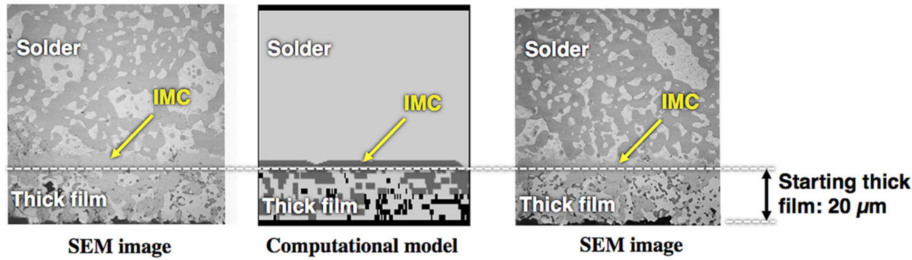


Fig. 21. Two-dimensional (left-hand side) and 3D (right-hand side) computational simulations that describe the reaction between molten Sn-Pb solder on Au-Pt-Pd thick film. The top images show the initial conditions for both cases. In the 2D model, the solder is light blue; the thick film is green; unfilled pores are white. The 3D model shows the solder in red; the thick film is blue; the unfilled pores are white. The bottom images show the reaction between the molten solder and the thick film (240°C, 15 s). In the latter cases, the solder and unreacted thick film are both blue and the IMC is red. The computer-simulated "interface" is represented by the color gradient between red and blue.



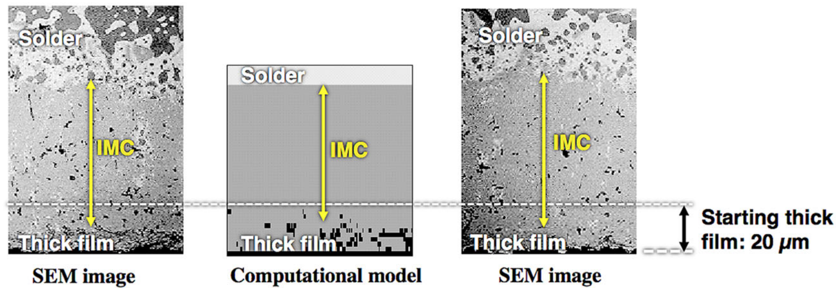


Fig. 22. Combination of SEM images and 2D computer simulations showing solid-state IMC growth between Sn-Pb solder and the Au-Pt-Pd thick film under two conditions: 135°C, 61 h and 170°C, 50 h. The IMC stoichiometry was (Au, Pt, Pd)Sn_4. The duplicate SEM photographs per condition validate the model predictions of IMC growth in the center positions.

condition is at the top, with the solder in red; the unreacted thick film is blue and unfilled pores white. The reaction is shown by the solid model at the bottom of Fig. 21. Both unreacted solder and thick film are blue; the IMC is red. The color gradient represented the interface between the IMC reaction product and unreacted solder and thick film. The attribute of this 3D model, as well as the

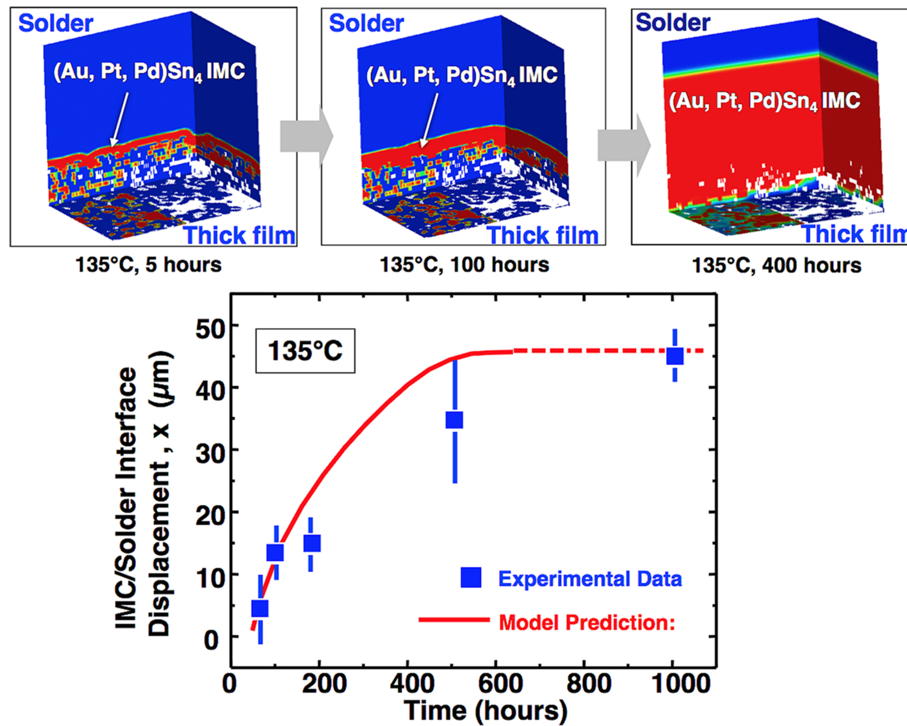


Fig. 23. Three-dimensional model shows solid-state IMC development predicted for Sn-Pb solder and Au-Pt-Pd thick film at 135°C and time periods of 5 h, 100 h, and 400 h. The solder and unreacted thick film are blue; the IMC is red; the interface is the color gradient; unfilled pores are white. The plot, which is at the bottom of the figure, shows a very good correlation between the model prediction (red graph) of the interface displacement and that calculated from the empirical data (square blue symbols).

simpler 2D routine, is that they can easily predict the effects of different porosity microstructures that are often created by small changes to the printing, drying, and firing steps used to create the thick film layer.

The extent of porosity in the thick film layer will also control *solid-state IMC growth*. This effect was first studied experimentally for the same system of Sn-Pb solder and Au-Pt-Pd thick film.[33] The duplicated SEM images in Fig. 22 show the progression of IMC development between the Sn-Pb solder and Au-Pt-Pd thick film following aging at 135°C for 61 h and 170°C for 50 h.[35,36] The IMC stoichiometry was (Au, Pt, Pd)Sn_4, having the same relative Au, Pt, and Pd concentrations as in the original thick film composition. The IMC formation begins at the solder/thick film interface and within the pores infiltrated by the Sn-Pb alloy during the soldering process. The 170°C, 50 h aging time resulted in the complete conversion of the thick film into an IMC layer.[†] The extent of the solid-state reaction was predicted by the 2D computational model. The model predictions are also shown in Fig. 22 between the duplicated SEM images for the two aging conditions. Those predictions show the excellent correlation with the empirical data.

[†]Note the formation of the Pb-rich layer between the IMC layer and solder field. Lead does not participate in the IMC reaction and is rejected ahead of the latter layer. Unfortunately, the materials model cannot capture this phenomenon.

The solid-state IMC growth computational model was extended to the 3D configuration. The predictions are shown at the top of Fig. 23 for IMC development following solid-state aging at 135°C for time periods of 5 h, 100 h, and 400 h. The color scheme is that same as previously discussed: the unreacted solder and thick film are blue; the IMC is red; the interface is the color gradient; the unfilled pores are white. The IMC composition was unchanged at (Au, Pt, Pd)Sn_4. The model prediction of IMC interface displacement is plotted in the graph below the images along with the empirical data. A very respectable correlation was observed between the two results given the complexity of the solder/thick film geometry.

The computational modeling tools cannot replace the need to understand the fundamental materials science that underscores interface reactions and their associated microstructures. For example, an important precaution is to minimize direct contact between the Sn-based solder and the glass phase at the interface between the thick film and the ceramic base material. This point is illustrated by an application that required the use of the Au-Pt-Pd thick-film layer technology for a flip-chip multi-chip module (MCM) application.[37] The requirement of fine-pitch lines and spaces necessitated the use of only a single-print thick film to minimize the layer thickness on the LTCC base material. A low magnification image is shown of the interconnection in Fig. 24a. The high magnification photograph in

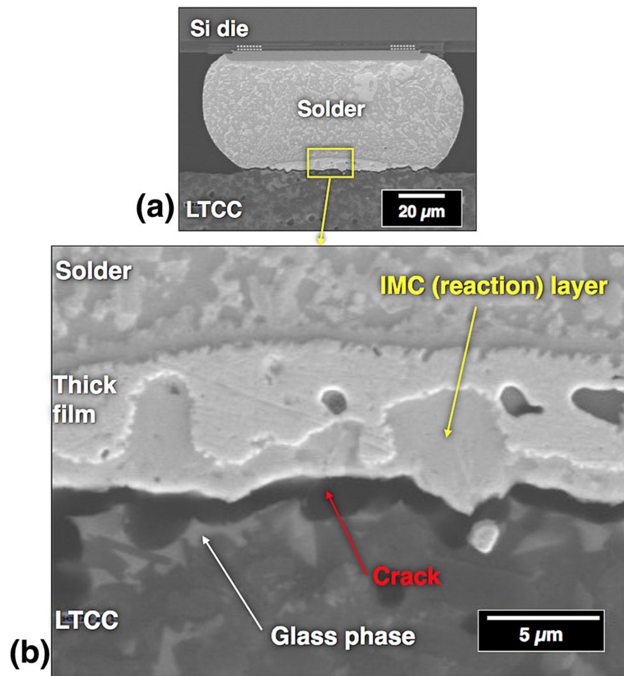


Fig. 24. SEM photographs demonstrate the failure of the Sn-Pb solder/Au-Pt-Pd thick film solder joint. (a) The low-magnification image shows the interconnection between the MCM and the LTCC base material using Sn-Pb solder. (b) High magnification photograph shows separation at the thick film/LTCC interface resulting from the attack of the glass phase by the Sn component of the solder.

Fig. 24b indicates that the solder readily flowed through the interconnected pores as confirmed by IMC formation. Therefore, the Sn component of the solder reached and then attacked the glass phase layer at the thick film/LTCC interface. The result was separation along the interface that compromised both the electrical and mechanical functions of the interconnection.

The above example underscores the role of solder joint volume on interface performance and reliability. To date, the input data for the models were obtained from experiments based upon semi-infinite fields of both the solder and base material (here, the thick film). However, smaller solder joints have lesser quantities of solder. Several authors have shown that the solder quantity affects both the reaction rate kinetics and the phase development of the interface microstructure.[38–40] Therefore, solder joint size will have to be considered with respect to the constitutive behavior(s) that govern computational predictive models.

SUMMARY

1. Electronic packaging technology takes advantage of a variety of materials to optimize performance and long-term reliability. A consequence of utilizing multiple materials is the unavoidable presence of interfaces.
2. This report examined several engineering applications having interface structures that are created by soldering technology. An important point, which was illustrated by those examples, was that interfaces represent non-equilibrium structures. Their physical metallurgy can change at room temperature because of solid-state diffusion processes. Therefore, their microstructures and, consequently, their mechanical properties are not always predictable by equilibrium principles.
3. A successful soldering process requires that an interface support wetting and spreading activity by the molten alloy. Whether interface reactions occur in the presence of molten filler metal or after solidification by solid-state diffusion mechanisms, the processes at one filler metal/base material interface can affect the microstructure and, as such, the performance and reliability of the other interface. Those same interface reactions can also generate solute atoms that alter the properties of the filler metal, itself.
4. Changes can continue to occur at the solder/base material interface after solidification, by means of solid-state diffusion and reaction mechanisms. Such changes have been demonstrated to significantly impact the long-term reliability of the interconnections.
5. Coatings and finishes are critical to the construction of electronic packages. However, it is recognized that regardless of their method of deposition—PVD, wet plating, or thick film—these layers introduce additional interfaces that must also meet assembly process, performance, and reliability requirements for the device or component. Moreover, sacrificial coatings (e.g., protective layers) that dissolve into the filler metal affect the latter's physical and mechanical metallurgy as well as that of the interfaces. The driving forces for these solid-state diffusion processes result directly from their non-equilibrium nature.
6. Computational materials models are being developed that predict both liquid-state and solid-state interface reactions between solder alloys and base materials. The particular attribute of these models is that they can take into account geometric complexities such as the porous nature of thick film layers. However, constitutive equations will have to account for reduced quantities of solder resulting from smaller interconnections.

FUTURE TRENDS

Interface reactions and microstructures will have an increasingly important role toward defining both soldering processes as well as establishing the long-term reliability of interconnections. This review has illustrated the effects of surface tension, base material composition, and structure (e.g., porosity,

composites, and so on) as well as rate kinetics on interface microstructures and their mechanical properties. Each of these factors will change as future solder joints continue to diminish in size. In addition, new solder alloys, surface finishes, and base materials will require a re-evaluation of many, if not all, of these properties. It is critical that materials scientists and engineers have a fundamental understanding of the roles of these factors and, more importantly, an appreciation of possible unexpected interfaces caused by their pseudo-equilibrium nature. This understanding will become particularly critical in the development of computational models to be used for predicting interface structures and their impact on solder interconnection reliability.

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