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SCAPS Modeling for Degradation of Ultrathin CdTe Films: Materials Interdiffusion

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Ultrathin film solar cells based on CdS/CdTe ($d_{\mathrm{CdTe}} \leq 1$ μm) suffer from two main issues: incomplete photo absorption and high degradation rate. The former is cured by light-trapping techniques, whereas the latter is a matter of fabrication details. Interdiffusion of the material components and formation of subsequent interlayers at the front/back region can change the optical/electrical properties and performance/stability of the device. We model the degradation of the ultrathin CdTe film devices considering the material interdiffusion and interlayers formation: CdTeS, CdZnTe, Cu_xTe (i.e., Te/Cu bilayer), and oxide interlayers (i.e., $CdTeO_3$). The diffusion rate of the materials is considered separately and the reactions that change the interlayer's properties are studied. Additionally, a back contact of single-walled carbon nanotube showed a higher stability than the metallic contacts. A new time-dependent approach is applied to simulate the degradation rate due to formation of any interlayer. It is shown that the materials interdiffusion causes a defect increment under thermal stress and illumination. The metallic back contact accelerates the degradation, whereas single-walled carbon nanotubes show the highest stability. A SCAPS simulator was used because of its ability in defining the properties of the back contact and metastabilities at the interface layers. The properties of the layers were taken from the experimental data reported in the literature.

INTRODUCTION

Materials interdiffusion is as important as pinhole formation in ultrathin film solar cells when thinning the CdTe layer to $d \leq 1$ μm. SIMS depth profiling, x-ray diffraction (XRD) analysis, CV and photoluminescence (PL) measurements on CdS/CdTe junction, and back contact (BC) interface of CdTe/metal indicated that during the deposition process, the adjacent layers diffuse into CdTe and change the optical and electrical properties of the device.[1] SIMS profiling shows the concentration of all the materials across the device, XRD shows the variation of phase and crystallinity as a representative of the interlayer formation, and CV and PL measurements show the defect increment due to interlayer formation. The diffusion mechanism accelerates under the stress condition when the device goes under illumination, bias, and temperature. Depending on the interlayer thickness and its optical properties, the electrical parameters of the device are improved or deteriorated. The XRD analysis of Romeo et al. on the ultrathin films with $d = 0.7$ μm and 1 μm show a similar phase and XRD intensity from an interlayer of Cd_5S_4Te with $d = 0.8$ μm.[2] Because XRD can penetrate the layer down to 1 μm from the surface, they concluded that this interlayer is not far from the back contact and it has been extended to the BC region during the annealing process. Intermixing with sulfur (even with reoptimized treatment condition) reduced the lattice parameter, bandgap ($\Delta E_g = -0.2$ eV), and efficiency (7.4%). Although Cu is known to be essential to obtain a better ohmic contact,[2–4] the Cu interdiffusion was not investigated in that analysis. However, Cu interdiffusion from the BC into the CdTe layer (confirmed by SIMS profiling)[3] forms a thin interlayer of Cu_2Te during annealing.[3] This layer is instable under light soaking (changing from Cu_2Te to CuTe), providing a Cu source that is accumulated at the junction and cause

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instability.[4] Bai et al..[4] have performed an XPS analysis on ultrathin CdTe films with $d = 0.7$ μm and related the low efficiency of $\eta = 7.9\%$ to Cu-related recombination centers at the junction. They detected that relatively stronger interdiffusion of S occurs for ultrathin films with $d = 0.5$ fabricated through a shorter growth time. In contrast, a few other researchers have suggested that the formation of interlayer can be used to enhance the performance and stability. Xia et al..[5] have deposited a Te/Cu bilayer (0.1/0.01 μm) useful for forming ohmic contact to ultrathin p-CdT films. XRD and PL studies indicated that the Te layer controls/mediates the Cu rapid diffusion and thus improves the stability. The proposed ultrathin film of CdS/CdTe/(Te/Cu)/Ni with $d = 1$ μm led to $\eta = 13.5\%$. Postgrowth treatment (temperature and time) were quite effective on the diffusion rate of the elements as was also analyzed by our latest investigations.[6] The stability under thermal stress was improved for thicker Te layer, whereas direct contact of CdTe/Cu (no Te) deteriorated the device much faster. Another type of interlayer is the oxide complexes such as TeO_x, which could improve the back barrier due to its higher work function than Te.[7] However, at higher O_2 concentrations, excessive oxidation occurs through $CdTeO_3$ and CdO compounds, which are chemically stable oxides with low mobility.[8] To remove the surface oxides, etching with bromine-methanol was proposed, which eliminated the roll-over in IV curves by increasing surface Te concentration.[9] Humidity (O_2/H_2O-containing environment) is an important factor in air-induced degradation by accelerating the oxide formation on the CdTe back surface.[10] The research group of Prof. Jaegermann have proposed that the ultrathin films with deposited CdTe double layers in two different temperatures could obtain pinhole free and higher efficiencies.[11] The second thinnest CdTe layer deposited at a low temperature fills the grain boundaries of the first one and helps to avoid formation of pinholes and shunting. For 0.5 and 0.8 μm CdTe layer, the efficiencies of $\eta = 5.2\%$ and 9.5% were obtained still suffering from low open-circuit voltage, $V_{oc} = 0.42$ and 0.56 V. The authors ignored preforming materials profiling (i.e., by SIMS); thus, the interlayer thickness is unclear. However, the increased quantum efficiency (QE) in the blue region is a representative of partial or full CdS consumption layer and shunting of back and front contacts ($d \leq 1$ μm). To simulate the interdiffusion of ZnO into CdS, Barrioz et al. have fabricated ultrathin films with CdZnS/CdTe with $d = 1$ and 0.5 μm, which led to $\eta = 6.8\%$ and 5.8%, respectively.[12] Slightly higher gain in short circuit current density (J_{sc}) was obtained for CdZnS windowed ultrathin CdTe films with bigger bandgap, E_g, than the CdS layer, which is evident in the blue wavelengths λ of the QE results. By $CdCl_2$ treatment, Zn interdiffusion into CdTe makes the CdZnS layer behave like CdS and show a red shift in QE at lower λ. The bandgap of the layers was not extracted and the interdiffusion of metallic BC was not investigated. It is known that $CdCl_2$ and/or heat treatment can increase the interdiffusion of the back metal (Cu ions) and window layers (S atoms) into CdTe. In this work, we will study the interdiffusion of the layers in CdS/CdTe ultrathin films and simulate their degradation behavior under stress of illumination, open bias, and room temperature. Several devices with $d \leq 1$ μm having determined interlayers of CdSTe, CdZnTe, Cu_2Te, $CdTeO_3$, and SWCNT are considered using SCAPS. To our knowledge, the role of each interlayer on the degradation behavior of the ultrathin films has not been considered systematically. Many research groups have reported and detected the formation of a thin interface layer of the adjacent materials; however, their influence on characteristics and reliability of the device requires investigations. To simulate the interlayer's effect, the primary data are taken from the given references. This makes our simulations closer to reality and comparable with the experimental data. The degradation is mostly attributed to thermal stress (heating) for a certain duration (i.e., see Ref. 5). We considered that the interlayer will induce a significant defect density at the junction and BC region over time.

INTERLAYER SCHEMES

The formation of interlayers is shown schematically in Fig. 1. The Cu diffusion path has been drawn through the grain boundaries. Basically, the materials from the back contact (i.e., Cu) can diffuse into the CdTe layer and form the relevant interlayer. In this scheme, the formation of Cu_2Te, CuTe, and Cu/Te bilayer is indicated. On the other hand, the window layer can diffuse into CdTe and form a different interlayer with a thickness that depends mostly on fabrication details such as annealing temperature and duration of treatment. This interlayer is shown as $CdTeO_3$ and CdSTe interlayers. Also, the deposition of a SWCNT is considered as indicated in the scheme. Each interlayer has been shown separately by a different color. We note that all the interlayers will not necessarily form in a single device.

CdTeS Intermixed Layer

Materials interdiffusion at the interface of CdS/CdTe heterojunction can lead to the formation of a very thin $CdTe_{(1-x)}S_x$ interlayer. This interlayer forms with a large x value on CdS side and with a smaller x on CdTe side. The properties of this interlayer impact the optical properties of the device by changing the thickness of either CdS and/or CdTe layers. This change is also seen in the bandgap of CdTeS interlayer via

$$E_g(x) = 1.74x^2 - 1.01x + 1.51 \quad (1)$$

The compositional dependence of the bandgap $E_g(x)$ can be described by interdiffusion of S from the

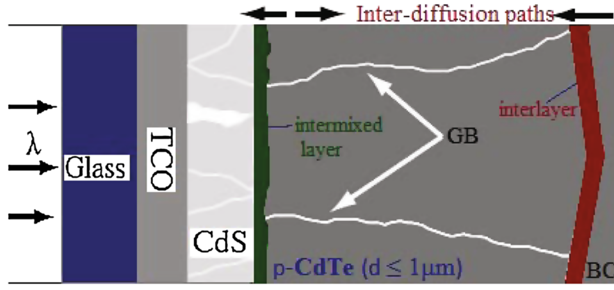


Fig. 1. Schematic of the materials interdiffusion. The interfacial layer represents the formation of CdTeS and CdZnS at the front contact and the interlayer represents the oxidation, CuTe formation at the BC. The migration of Cu ions through the grain boundaries has been shown. The back contact is Cu rich; otherwise, it is SWCNT.

CdS to CdTe layer, which is enhanced by the postgrowth treatment. $CdTe_{(1-x)}S_x$ with wurtzite structure is formed by partial consumption of the CdS layer. Thereby, the CdS thickness is reduced or, in extreme cases, completely consumed. The S interdiffusion process runs through grain boundaries and/or bulk materials that are accelerated in high temperatures. The reverse process can happen where Te diffuses into CdS. SIMS profiling by Dhere et al.[13] showed that $CdCl_2$-treated devices have a high electric field at the junction of Te-rich CdSTe alloy similar to a n^+-p junction with higher V_{oc}.[13] Krishna et al.[14] have measured a ΔE_g = 0.06 eV in a CdTe film where a linearly graded bandgap was detected.[14] The scanning electron microscopy pointed the latter observations by diffusion of S into CdTe. $CdTe_{(1-x)}S_x$ formation near the CdTe/CdS interface with the minimum bandgap of E_g = 1.4 eV is at x = 0.2. Although S has the lowest diffusion constant, the diffusion coefficient of S is increased by three orders of magnitude after postgrowth treatment. The large chemical self-diffusion coefficient of CdTe guarantees a homogeneous growth of CdTe films. The content of S into ultrathin films will be continues, i.e., from 1% or less near the back contact to 4% to 5% near the CdS interface.[4] We will have to limit our simulation to the thin interlayer of CdTeS at the junction with the properties given in Table I. The diffusion coefficient of CdS into CdTe layer through grain bulk, D_{bulk}, and grain boundaries, D_{GB} is given by[8]

$$D_{bulk}(T) = D_{bulk,0}\exp^{\frac{-2.8}{kT}},\ \text{where}\ D_{bulk,0} = 2.4 \times 10^7 \tag{2}$$

$$D_{GB}(T) = D_{GB,0}\exp^{\frac{-2.0}{kT}},\ \text{where}\ D_{GB,0} = 0.34 \times 10^7 \tag{3}$$

CdZnTe

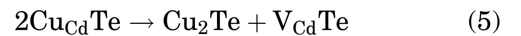
In an interesting attempt by Barrioz's group, the ultrathin CdTe films with $Cd_{(1-x)}Zn_xS$ devices were produced by metal organic chemical vapor deposition technique.[15,16] The incorporation of Zn into the CdS window layer improved cell performance markedly in the blue region of QE curves, showing that the optical transparency of the window layer was enhanced. In other words, the absorption edge enhanced because of the interdiffusion of Zn during the $CdCl_2$ treatment. The interlayer formed at the junction of CdZnS/CdTe was approximately 0.03–0.15 μm. However, this thickness depends on treatment time and temperature. $Cd_{(1-x)}Zn_xS$ is a wide bandgap (e.g., 2.7 eV) and can increase the solar cell performance when reducing the CdTe down to 0.5 μm. This is understood by considering the QE curves where the better response is observed in the blue region, where the absorption length is shorter. The degradation of such device is under question as Zn diffuses into CdTe and the thinner window layer is lowered. The compositional dependence of the energy gap of the synthesised $Cd_{(1-x)}Zn_xS$ layer were extracted by the same group[1]

$$E_g(x) = 0.91x^2 + 0.21x + 2.47 \tag{4}$$

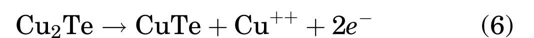
The devices with this window layer showed a better J_{SC}, but the series resistance increases over time. Chemical and structural investigations of CdTe solar cells employing wide bandgap window layers show that recrystallization and interdiffusion effects take place in the CdS and, to a lesser extent, in the CdTe layer. This results in interlayer formation (with a CdS nucleation layer) as well as compositional variations of the $Cd_{(1-x)}Zn_xS$, which strongly depends on chlorine treatment. Another conclusion relevant to our study is that the chlorine treatment enhances both CdS restructuring and interdiffusion of the cation during the heat treatment.[17]

Cu_xTe Interlayer

The primary contact of Cu_xTe is by evaporating a thin Cu layer (~ 3 nm) on etched CdTe.[8] This interlayer produces a back contact with low resistivity (10–10^{-4} Ωcm) by forming highly degenerated p^+-Cu_xTe compounds and dopes the bulk CdTe. XPS measurements of Teeter reveal the formation of a Cu-rich phase of Cu_xTe with $x > 1$.[18] If bulk-diffused Cu ions occupy Cd lattice sites, the Cu_2Te formation can be



$$2Cu_{Cd}Te \rightarrow Cu_2Te + V_{Cd}Te \tag{5}$$



$$Cu_2Te \rightarrow CuTe + Cu^{++} + 2e^- \tag{6}$$

Under the long-term bias condition, the Cu_2Te compound changes to the CuTe layer, leaving Cu^{++} charges via a weakly favored reaction.[19] Cu_2Te assists the majority carrier transport at the back

Table I. The Baseline Parameters Used in SCAPS Platform

Layer	*d* (μm)	Doping (cm^{-3})	E_g (dV)	μ_e (cm^2/v.s)	Ref.
CdS*	0.1	2×10^{18}	2.4	80	23
CdTe	0.8	1×10^{14}	1.45	100	23
CdTeS	0.1	2×10^{17}	2.4	80	25
CdZnTe	0.1–0.8	2×10^{16}	1.45	100	1
Te/Cu,Cu_2Te	0.101–0.103	8×10^{13}	4.5	100	5
$CdTe0_3$	0.002–0.008	3×10^{12}	≥3	80	7
s-SWCNT	0.01	5×10^{15}	≥5	10^5	22

The other parameters were kept as default values of SCAPS. *Except the CdS layer, the other layers have *p*-type doping

contact and diminishes the rollover in current density-voltage (JV) characteristics because it is highly conductive p-type material and makes a good ohmic contact to CdTe. In contrast, CuTe is a poor conductor and could be responsible for the blocking the hole transport to the BC. Based on Eq. 5, disassociated Cu^+ ions diffuse toward device junction through the grain boundaries. XRD results of Demtsu group in NREL support the conclusion that the Cu_xTe phases can be controlled by varying the Cu/Te ratio.[20] They concluded that excess Cu degrades device performance not only through increasing the carrier recombination as a result of excess Cu diffusing to the front region but also through its effect on the barrier height. Thus, controlling the Cu/Te ratio is a critical parameter in device manufacturing when Cu_xTe is used as a back contact. In another XRD investigation, Cu-rich contact followed by thermal treatment led to an increased V_{oc}.[8] Optimal cell performance was obtained for Cu/(Cu + Te) = 0.7. The deposition of Cu/Te bilayer suggests that if CdTe could be sufficiently doped at the BC region (without requiring Cu diffusion from the back contact), then Te metal contacts (i.e., ZnTe) could be developed. This is because Cu diffuses to the junction even under no bias as Cu ions are mobile at room temperature. Although Cu_2Te has the highest conductivity, it is unstable and provides more Cu diffusion into the CdS and CdTe films. Cu diffusion into the CdS causes rollover and Cu diffusion into the CdTe film creates Cu-related defects that decrease photogenerated carrier lifetime and result in voltage-dependent collection. Many other interface layers such as CdTeCl can be formed at the interface or junction. Those layers will be considered elsewhere with emphasis on the relevant induced defect density as Cl controls the uncompensated density very effectively.

Surface Oxidation

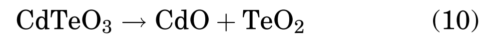
The XRD analysis of McCandless et al., on the surface of CdTe films, indicate that treatment of CdTe films in air and/or $CdCl_2$/air vapor, forms the native oxide $CdTeO_3$ and/or CdO, respectively.[8] The formation of surface oxides reduces S interdiffusion from CdS into CdTe and improves junction stability. However, the $CdTeO_3$ surface oxide cannot effectively limit $CdCl_2$ concentration in CdTe film. The residual oxide phases contribute to series resistance and rollover in the JV profile of the device. The residual oxides are wide bandgap materials ($E_g > 3$ eV: electrically insulating), which cause the formation of high-resistance contacts and affect the stability of JV measurements. The deposition of Cu-rich contacts to the oxidized surface of CdTe does not significantly improve the device characteristics. The surface oxides can form though the following reactions:

$$Te + O_2 \rightarrow TeO_2 \quad (7)$$

$$CdTe + 1.5O_2 \rightarrow CdO + TeO_2 \quad (8)$$

$$CdTe + 1.5O_2 \rightarrow CdTeO_3 \quad (9)$$

We know that TeO_2 can come from the other oxides, CdTe/SWCNT(Au) where the hole majority carrier could be



$$CdTeO_3 \rightarrow CdO + TeO_2 \quad (10)$$

In another case, the growth of $CdTeO_3$ from 2 to 8 nm on the surface of CdTe will cause fast degradation by increasing the back barrier height of 0.1 eV. Oxygen has a high diffusion coefficient,

$$D = D_o \exp\left(\frac{2.53}{kT}\right) \text{ where } D_o = 0.13 \text{ cm}^2/\text{s} \quad (11)$$

By heat treatments, the distribution of oxide particles may change because particles may dissolve when heated and grow when cooled. Oxygen atoms are found to change the effect of other impurities, a process known as internal gettering. Thus, the formation of $CdTeO_3$ on the CdTe surface during the air heat treatment modifies the surface chemistry

that occurs during the subsequent $CdCl_2$ vapor treatment and appears to inhibit the formation of $CdTeO_3$ along grain boundaries. The residual oxides are wide bandgap electrically insulating materials, which prevent formation of low-resistance contacts and affects retrace stability of JV measurements. The addition of Cu to CdTe surfaces containing oxide residues does not significantly alter the device characteristics. It is unclear what the oxide distribution is within the grain boundaries and their electronic effect on device operation. However, the diffusion-inhibiting property may widen the processing latitude with respect to ultrathin CdS window layers and copper doping. Furthermore, the oxide may retard copper-related stress degradation phenomena. Controlling the oxide distribution may lead to enhanced performance overall by reducing back-to-front contact junction paths and may enable devices with thin CdTe, on the order of 1 μm, to reach state-of-the-art performance levels. The advantage of oxide layer formation on the surface is by blocking the GB for Cu diffusion into CdTe. It was reported in the literature that when stressing was carried out in humid air, a more pronounced degradation was observed due to the polar and screening nature of water that facilitated the oxide formation by reducing the barrier in the actual oxidation reaction.[21]

Carbon Nanotubes

Very recently, semiconductor single-wall carbon nanotubes (s-SWCNTs) were simply spray deposited onto thin film CdTe devices as a back contact.[22] The efficiencies of SWCNT back contacted devices were slightly lower (6.15%) than Au/SWCNT contacted ones (10.40%). The reason for the lower efficiency (η) of the SWCNT without alloying with Au is that the work function of pure SWCNT is lower than the one doped with Au. Thus, the back barrier is an issue for the pure one while the Au-doped nanolayer can transfer the carriers easier. The other reason is that the lateral resistance of the pure SWCNT without Au doping is high, and thus the carrier collection is a big issue using the external electrodes to this structure.[22] Thus, the device back contacted with SWCNT lost the efficiency to about 3.12% and the latter contact showed to be thermally stable (10.99%) during accelerated life testing. The interesting result was that the V_{oc} of SWCNT and Au/SWCNT contacted devices were slightly higher after thermal stress (0.746 $\rightarrow$ 0.773 V and 0.778 $\rightarrow$ 0.783 V), respectively. The reason for such stability was correlated to the lack of metallic atoms present and that the temperature is too low to initiate oxidation. In fact, the interdiffusion of metallic atoms was perfectly controlled by the CNT network. Moreover, the grain boundaries were covered by the CNTs and the interdiffusion of metallic ions (present due to tools and environment) was impeded. Clearly, the high V_{oc} is attributed to the low back barrier between the collected without need for Cu incorporation. The other interesting result was that the higher efficiency of Au/SWCNT back contact was attributed to the lower sheet resistance due to Au addition. Scanning electron microscopy images can verify that SWCNT film acts as a blanket that covers and conforms to the topography of the polycrystalline CdTe thin film. Au particles only decorate SWCNT bundles but do not wet or penetrate the film. On the surface of CdTe where SWNTs contact the individual CdTe grains, there will be nanoscale junctions and each individual grain will be in contact with SWCNT with a lower barrier.

MODELING PROCEDURE, SCAPS BASELINE

The modeling was performed using SCAPS program.[23] SCAPS has the ability of defining the properties of the back contact, which is not possible in AMSP-1D simulator.[24,25] Also the higher values of defect density cannot be diverged in AMPS, but SCAPS can extend the simulations to more than 10^{20} cm^{-3}. The other strength of SCAPS is that it allows the interband transition as well as auger recombination and band–band transition to occur simultaneously, which can make the simulations rather closer to reality. It is believed that this program is more suitable to consider the back contact issues as it can also take into account the tunneling enhance recombination and thermionic emission together thus rather appropriate to be used for nanostructured devices.[25] Under normal working conditions, the need for a large number of input parameters (50–100) makes the modeling difficult. Many parameters depend on the fabrication conditions and deposition details. Therefore, we limited our modeling to change only certain values that are practically in an accepted range and could reproduce the experimental reports in literature. Generally, we tried to keep the parameters constant and vary only one of them, defect density, for each optimization at a time. The simulation results on the degradation studies were based on the interesting approach (time dependent) that was introduced by Nardone,[24] where also we were partially involved in developing this approach. Table I represents the baseline parameter values used in SCAPS for simulations. Note that in the literature, there were very limited experimental data for material interdiffusion in ultrathin CdTe films. We will use the optimum values reported on interlayer thickness, back barrier ϕ_b, bandgap E_g, and performance parameters of the devices fabricated in the relevant references. The interlayer is introduced in the SCAPS platform as an additional layer between the CdS/CdTe or CdTe/BC. The best performance parameters obtained by the respective interlayer and reported in the literature are as given in Table II. The data limited to ultrathin CdTe films only except SWCNT that was deposited on thin CdTe and there is no report on its application on ultrathin film CdTe devices.

Dzhafarov et al.[26] have estimated the effective diffusion coefficients of Cu for thermal D_T, and photo diffusion D_{ph} in the CdTe films has been estimated from resistivity versus duration of thermal or photo-annealing curves.

$$D_T(T) = D_{to}\exp^{\frac{-0.33}{kt}},\ \text{where } D_{to} = 0.73 \times 10^{-6}\,\text{cm}^2/\text{s} \quad (12)$$

$$D_{ph}(T) = D_{pho}\exp^{\frac{-0.20}{kt}},\ \text{where } D_{pho} = 0.047 \times 10^{-6}\,\text{cm}^2/\text{s} \quad (13)$$

In the temperature range of 60°C to 200°C, the diffusion coefficient of photo-stimulated migration of Cu is larger than that of thermal diffusion by two to four times.[26] Thus, the degradation of performance was tentatively assigned to electrodiffusion of Cu in CdTe under stressing at a high temperature when the Cu concentration is redistributed. The acceleration of Cu diffusion under illumination can be tentatively attributed to photo-ionization of Cu, resulting in faster diffusing interstitial Cu^+. Moreover, using heating stress time t for degradation studies, the parameter D_t can be estimated as

$$D_T(x,t) = \frac{kT.x}{e.E.t} \quad (14)$$

where x is the thickness of CdTe film, k is Boltzmann's constant, e is electric charge, E is the electric field across the CdTe thickness (≈ 1 MV/m), and T is the heating temperature. Defect diffusivity by temperature T is given by[27]

$$D(T) = A\exp^{\frac{-\Delta E}{kT}},\ \text{where } A = \frac{nr^2v}{6} \quad (15)$$

where n is the number of available neighboring sites, r is the jump distance, v is effective frequency, and ΔE is the barrier height. For Cu^+, it was calculated: $A = 0.0073\ \text{cm}^2/\text{s}$ and $\Delta E = 0.51$ eV.

RESULTS AND DISCUSSIONS

Now consider the ultrathin device in Fig. 2. The CdTe layer was divided into interlayers at the junction, bulk part and BC region. For example, the front contact is assumed to be CdTeS/CdTe and for another case as CdZnTe/CdTe. Instead, the back contact is divided to CdTe/Cu_xTe (or Te/Cu) and once as CdTe/SWCNT. The thicknesses of the interlayers are as given in Table I. The properties of the devices are reported in detail in relevant references. The simulation procedure takes into consideration the increment in the defect density across the CdTe layer. In reality, thermal stressing the device will run the defects (i.e., Cu^+) to the junction. Those defects are disassociated from the interlayer and for a longer stressing may reduce the thickness of interlayer. The theory of this work is based on defect-related degradation equation[24]

$$\frac{dN}{dt} = \alpha n - \beta N \rightarrow N_i^{(t+1)} = N_i^{(t)} + \alpha\Delta t\left(n_i^{(t)} - n_i^{(0)}\right) \quad (16)$$

where α and β are defect creation and annihilation coefficients, and N and n are generated defect and electron concentrations, respectively. The second term is neglected as we consider that the saturation is very small in a short time ($\beta t < 1$). The structures with properties given in Tables I and II are modeled in SCAPS. The simulation results are presented in Figs. 3, 4, 5, and 6 where the efficiency, fill factor, open-circuit voltage, and short-circuit current are tracked for degradation over time when the defect density is increased step by step according to Eq. 16. Note that the structures were all kept at room temperature when performing the iterations. Increasing the defect density from $2 \times 10^{14}\ \text{cm}^{-3}$ to $8 \times 10^{15}\ \text{cm}^{-3}$ and recording the electrical parameters gives us the degradation rate. The simulation was performed under a greater stress condition than open-circuited condition as shown in Fig. 2. This is due to the fact that the illumination voltage will be opposite of the space charge region (SCR) electric field and it can be assumed that the electric field is zero at the junction. This simulation must be performed under illumination; otherwise, the electrical parameters cannot be obtained in SCAPS. However, we keep the illumination constant (1 sun) for all iterations. SCAPS has the ability to model the open-circuited device. The thermal stress is

Table II. The best performance parameters reported in the literature for the ultrathin ($d \leq \mu$m) film CdTe devices with an interlayer

Structure	V_{oc} (V)	J_{sc} (cm^2/v.s)	FF (%)	η (%)	Ref.
CdS/CdTeS/CdTe/BC[a]	0.580	18.5	58.7	7.9	4
CdZnTe/CdTe/BC	0.622	21.5	66.1	8.9	12
CdS/CdTe/(Te/Cu)/BC	0.790	20.4	69.0	11.1	5
CdS/CdTe/$CdTeO_3$/BC	0.780	22.1	67.2	10.2	8
CdS/CdTe/s-SWCNT	0.783	14.0	28.45	6.15	22

[a]BC refers to the metallic back contact (mainly Cu-rich)

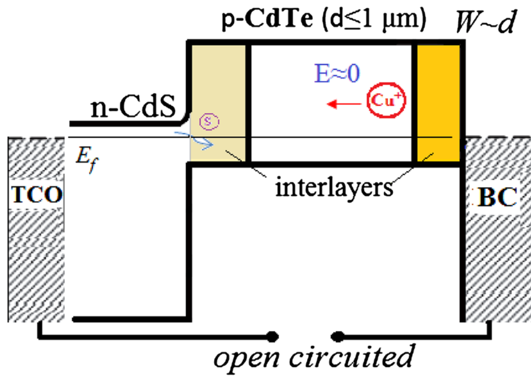


Fig. 2. The energy band diagram and structure of CdS/CdTe ultrathin open-circuited film. The CdTe layer is divided in two interlayers at the CdS/CdTe and CdTe/BC junctions. For each structure, we assume a different interlayer adhered to CdTe.

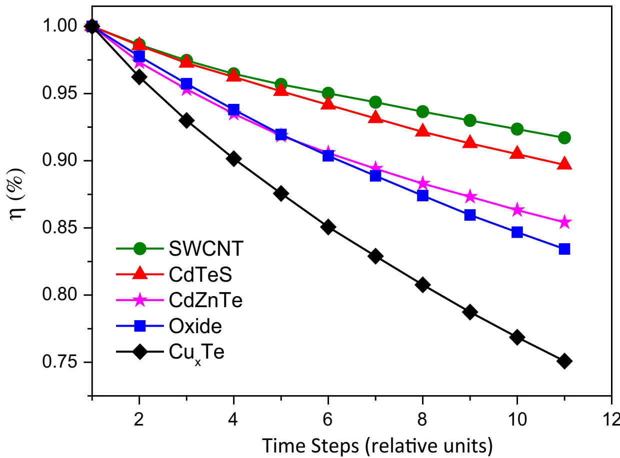


Fig. 3. Degradation rate of efficiency for five different devices with very thin interlayers formed at the junction or BC region. The faster degradation belongs to Cu-contained interlayers.

required to increase the defect diffusion into the CdTe layer. The structures presented in Table II are inserted in the SCAPS platform separately.

Figure 3 shows the degradation of the structures with different interlayers. The SWCNT back contacted device showed the lowest degradation rate. This was also confirmed by the experiments in Ref. 22. This might be due to the fact that the pure SWCNT layer without any doping was not responsible for any defect accumulation at the junction. Note that the metallic contacts will provide the extra defects to the junction, and the accumulation of those defects will increase the recombination rate leading to faster performance degradation performance. Both CdTeS and CdZnTe interlayers showed slightly faster degradation still lower than the other cases. The interdiffusion of S and Zn is not a deteriorative effect but can increase the bandgap. However, either material can be impurity in the junction of the CdS/CdTe and distort the electric field and cause lower carrier collection. The effect

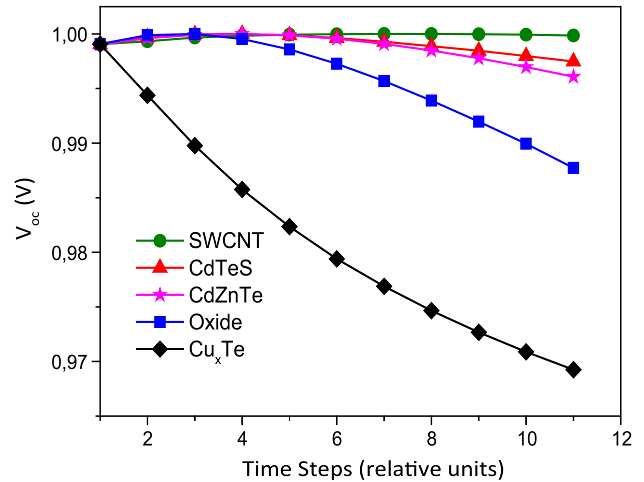


Fig. 4. Degradation rate of open-circuit voltage for five different devices with very thin interlayers formed at the junction or BC region. The stress was assumed to be open circuited while stressing. The lowest rate belongs to a SWCNT back contacted device as it cannot be a defective layer.

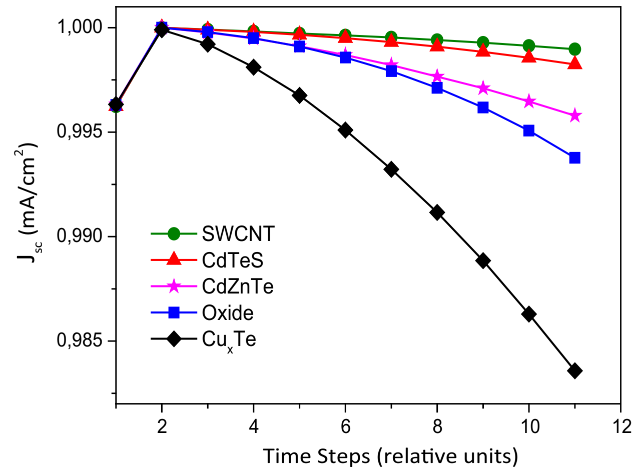


Fig. 5. Degradation rate of short-circuit density for five different devices with very thin interlayers formed at the junction or BC region. The first steps of defect increment are relevant with increased carrier collection due to increased electric field at the junction.

of oxide and Cu_xTe interlayers is extremely deteriorative.

Clearly, the low mobility of oxides as insulating layer can cause a barrier for the carrier collection. Under stress, this layer can create defects from deoxidation reactions as presented in Eq. 10. These defects can be a physical barrier to the carrier transport or to be accumulated and cause degradation and permanent deterioration of the device. Moreover, the secondary complex formation of oxygen molecules can act as acceptor defects at the CdTe layer, which can alter the conductivity. The last interlayer, Cu_xTe, is worse as it is a source of Cu^+ mobile ions. The thermal stress of this structure (CdS/CdTe/Cu_xTe) is a good force for Cu ions to move toward the junction and accumulate there.

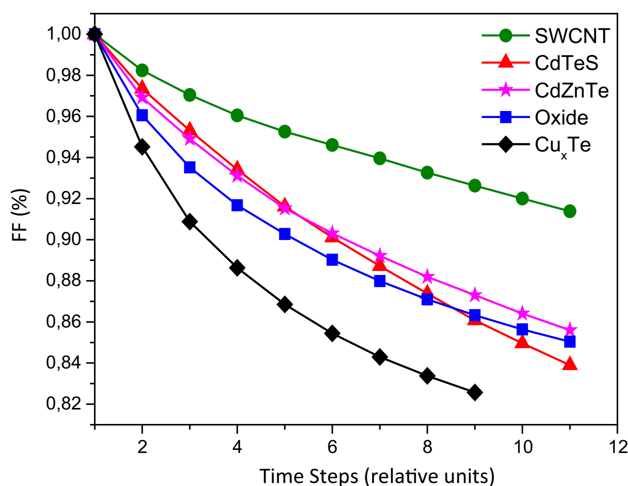


Fig. 6. Degradation rate of FF for five different devices with very thin interlayers formed at the junction or BC region. The faster degradation of FF reminds the deteriorative effect of series resistance.

Figure 4 shows that V_{oc} was not reducing very fast. It was expected as we did not change the back barrier of the interlayers during the stress. This is closer to the experimental reports. An interesting conclusion from Fig. 5 is at the first steps of defect creation that is followed by an increase in the carrier collection shown in J_{sc}. This is probably because of the increased electric fields by the defect density, which were inserted as the shallow defects across the CdTe layer. In both latter parameters, V_{oc} and J_{sc} did not decrease rapidly, meaning that the device was not too sensitive to defect creation and the deteriorative effect of interlayers is not considerable. Even in some cases, the carrier collection and photoabsorption can be improved by increased bandgap (CdZnTe) and/or saturation current impediment at the back contact interface (oxide interlayer). In contrast, the degradation rate of fill factor (FF) (Fig. 6) is fast, reminding us that R_s is responsible for device degradation. The Cu_xTe and oxide interlayers obtained a faster rate that is in agreement with the known phenomena that an increase in series resistance can be caused by the metallic defects and impurities (oxides). When stressing is carried out in humid air, a more pronounced degradation is observed probably due to the polar and screening nature of water that facilitates the oxide formation by reducing the barrier in the actual oxidation reaction. In the humid environment, water vapor tends to be adsorbed at the junction interface and the ionic species become mobile. The electric field at the junction and the application of forward bias under illumination favors the migration of ionic species across the junction surface. The surface current varies with humidity in the environment and couples to other components of dark current at the junction. Therefore, the junction surface should be protected from the environment, which makes the surface ions immobile.

All the results were normalized to their maximum values as represented in Table II. The defect density increment under thermal stress is not too strong on some of the structures that do not contain Cu or metallic ions. The application of SWCNT on the back contact of the device will not have the negative effects of interdiffusion if it is not doped with metallic alloys (i.e., Cu and Au). Last year, we had investigated the SWCNT application as buffer layer of CdS/CdTe.[28] Rather precise influence of the thin interlayers on the photocurrent density and QE can be obtained taking into account the absorption coefficient and optical properties of the layers and inserting them into transmission and reflection coefficients.[25,29,30] The results indicate that this nanostructure can be a cheap and simpler material for carrier transport at both junction and BC regions. The degradation rates of all the structures tend to be very slow after 11 iterations.

This finding is in agreement with Eq. 14, where diffusion of the defects is reversely relevant to time. Thus, the interdiffusion rate is reduced and the degradation rate slows down consequently. We also examined the temperature variation of the iterations (not shown here). For example, the operation temperature of $T = 333$ K was applied when the defect concentration N was increasing repeatedly. However, the variation on degradation rate was negligible ($< 3.71\%$).

SUMMARY

Although CdTe with a typical thickness of 1–2 μm would be optimal for both optical and electrical applications, in practice it is very hard to achieve ultrathin films without a subset of problems. The submicron absorber thickness deteriorates the device performance quickly due to increased defect densities accompanied by the loss of photocurrent. In addition, the absorber layer thickness becomes much smaller than the photon absorption length, leading to incomplete optical absorption with a thin absorber (deep penetration loss). This article presents a time-dependent degradation of ultrathin film devices based on CdS/CdTe. The modeling was performed in SCAPS while the properties of the materials were kept constant from the default of simulator except for a few particular parameters of the interlayers. The interlayer formation at the junction and/or back contact of the solar cells is widely reported in the literature. A detailed study is required to understand the role of materials interdiffusion on the efficiency and stability of the device. Some of the more conventional interlayers were considered in this investigation. We examined the effect of S and Zn interdiffusion at the junction of CdS/CdTe as well as formation of an oxide and a Cu_xTe thin layer at the interface of CdTe/BC. Moreover, the SWCNT back contact was simulated where the newest experimental report on this material was interesting. The simulation results

show that thermal stress of the open-circuited devices that contain an interlayer is considerable if the defect density increases relatively by time. Interlayers will be the source of defect generation and/or barrier for carrier collection. The SWCNT back contacted device was the most stable one with the lower reported efficiency of 6.15%. The diffusion of mobile ions such as Cu^+, impediment of Oxide molecules, bandgap widening by the Zn and S alloys is attributed to the degradation rate of the relevant device.

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