Impact of Processing Conditions and Solder Materials on Surface Mount Assembly Defects

Rajen S. Sidhu, Raiyo Aspandiar, Steve Vandervoort, Dudi Amir, and Gregorio Murtagian

The conversion to lead-free solder alloys and increasing dynamic warpage due to the coefficient of thermal expansion (CTE) mismatch and thinner microelectronic packaging technology has resulted in a significant increase in the risk of solder joint defects for ball grid array (BGA) components. This paper will review head-and-pillow (HnP) defects observed after surface mount assembly with specific focus on fine-pitch BGA technology on motherboards. The mechanisms related to various aspects of design and materials characteristics that affect the creation of these defects within the solder joints will be discussed. Finally, potential material solutions for eliminating these defects will be reviewed.

INTRODUCTION

Concerns over the environmental and health impacts of Pb-based solders in consumer electronics has led to the development of Pb-free solder alternatives. The electronics industry has begun proliferating Sn-Ag-Cu alloys due to their superior mechanical properties, good solderability, and relatively low cost.[1,2] Although these materials are very suitable as replacements for Pb-Sn, the surface mount reflow process (i.e. the melting and solidification of solder interconnects) remains a technical challenge due to the higher solder melting temperature (~217°C) compared to Pb-Sn compositions (180°C–190°C).[1] Near-ternary eutectic Sn-Ag-Cu alloys yield three phases upon solidification: β-Sn, Ag_3Sn, and Cu_6Sn_5. The β-Sn phase requires significantly greater undercooling in order to induce nucleation and bring about final solidification.[3–5] As a consequence of this difference in required undercooling for nucleation, large plate-like Ag_3Sn structures can grow rapidly within the liquid phase during cooling and prior to final solidification of solder joints.[6–8] These plates can adversely affect the plastic deformation properties of the solder and cause strain localization at the boundary between the Ag_3Sn and the bounding β-Sn phase. Additionally, from an assembly manufacturing perspective, increased peak temperatures during reflow increase the amount of total dynamic warpage the microelectronic package will experience as a result of the CTE mismatch between various metallic and polymeric components. With the microelectronics industry trending toward environmentally friendly manufacturing, smaller and thinner packages, and increasing board density, all of these amplify the challenges of surface mount board assembly.[9–14] As a result of these challenges, there is increased risk of forming surface mount (SMT) non-wet joint defects called head-and-pillow (HnP) defects. This defect phenomenon is defined as a joint comprised of two metallurgically distinct masses formed from a ball grid array (BGA) sphere and reflowed solder paste with incomplete or no coalescence. Figure 1 shows a typical cross section of the head and pillow defect, highlighting the clear separation between the two solder masses. These defects are detrimental to electronic packaging as they impact both performance and overall reliability. This article will review a number of the key mechanisms and risk factors that influence BGA non-wet failure rates related to package design, process, and material interactions.

How would you…

…describe the overall significance of this paper?

This paper describes the fundamental mechanisms behind the creation of surface mount assembly defects in fine-pitch ball grid array microelectronic packages. It details the impact of process factors and materials characteristics that can help eliminate these defects for Pb-free solder assembly.

…describe this work to a materials science and engineering professional with no experience in your technical specialty?

Due to the thermal expansion mismatch between different materials within the microelectronic package, dynamic warpage is a major risk for yield and reliability performance. This research highlights the impact of flux acids in effectively removing tin oxides from Pb-free solders to prevent improper solder joint formation. In addition, the impact of dopants and impurities in the solder sphere on surface oxide formation and solidification behavior are discussed.

…describe this work to a layperson?

To ensure handheld devices and computers can withstand the rigors of day-today-day life, it is crucial that the materials used to solder the circuitry together are robust enough to pass electricity uniformly. Similar to a crack in plumbing which can prevent water from flowing smoothly, thousands of lead-free solder interconnects need to be joined on a printed circuit board to allow a device to power on and off.

DISCUSSION

One of the main factors influencing HnP defects during lead-free reflow assembly (i.e. heating from 25°C to ~240–260°C and cooling down to 25°C) is due to loss of contact between the package solder spheres and SMT paste. The main reason for this phenomenon is due to the coefficient of thermal expansion (CTE) mismatch between different materials within the

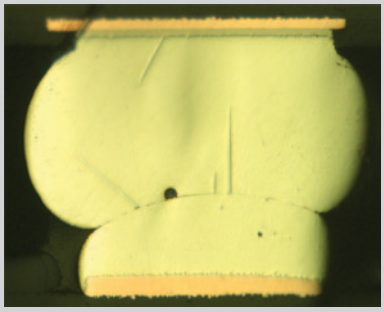

Figure 1. Optical cross-section of head-in-pillow SMT non-wet defect.

electronic package stack-up. Various factors influence the resulting warpage including die size, substrate material (i.e. thickness and copper layer ratio) ,and mold compound material.[10–12] Figure 2a highlights the change in shape and gap formation between the package and printed circuit board (PCB) at a reflow temperature ~240°C using Shadow Moiré mapping. Essentially, the package warps >100 µm away from the PCB in the defect area. It is clear from this map that the edge rows interconnects will be at highest risk (dark contour regions) during reflow. This was verified during defect mapping over several tests runs as shown in Figure 2b where interconnects which had HnP defects form in clusters correlating directly with maximum warpage locations. The separation gap has been confirmed by direct observation of the reflow process (e.g. Figure 2c), in which the package typically reaches a warpage value >100 µm at the solder melting temperature and lifts the solder balls out of the solder paste. As the package and PCB are cooled, the warpage decreases and the solder balls drop back into the paste. The resulting poor contact causes two major issues during SMT processing 1) additional oxidation of the solder ball surface and 2) detrimental degradation on the solder paste wetting characteristics.

Solder Paste Impact

Separation between the solder ball on the package and the solder paste occurs between the flux activation time and time above liquidus between the temperature range (150°C–220°C). During this time, significant degradation of the SMT paste flux can occur. Figure 3a shows the thermogravimetric analysis (TGA) flux weight loss data for paste A, a Pb-free Sn-3.0Ag-0.5Cu using a representative reflow profile. The majority of weight loss results from solvent evaporation at the onset of paste melting. Simultaneous with solvent loss, the activator acids begin to react with the surface oxides (i.e. SnO and SnO_2) of the solder powder within the paste as shown in Equations 1 and 2, reducing the concentration of activators available for solder ball oxide reduction.

Hydrogen Bromide:

$$SnO + 2HBr \rightarrow SnBr_2 + H_2O_{(g)} \quad (1)$$

Carbolxylic Acid:

$$SnO + 2RCOOH \rightarrow Sn(RCOO)_2 + H_2O(g) \quad (2)$$

This is an important observation: if the flux is not in contact with the solder ball at this time, it will be unable to efficiently remove the surface oxides on the ball, delaying or preventing proper joint formation. The impact of flux effectiveness on HnP defects is further validated with dynamic wetting metrology experiments conducted using a Rhesca Solder Checker SAT-5100 (Tokyo, Japan).[13,14] The advantage of this tool, unlike conventional solder wetting balances, is that it allows for investigation of solder paste in amounts similar to the actual paste volumes used during the SMT process. In this apparatus, a solder ball is lowered into a molten paste deposit and the dynamic

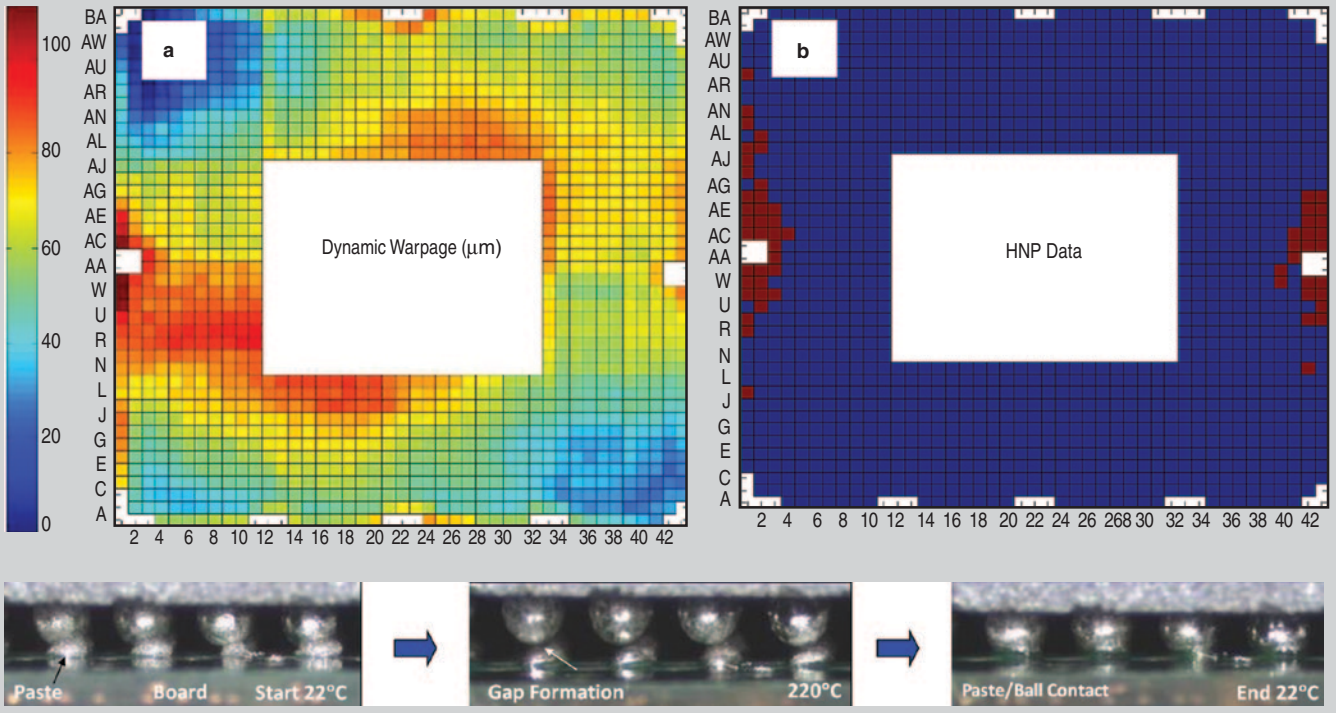

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Figure 2. (a) Shadow Moiré map of dynamic warpage between a package and PCB at 220°C. (b) Defect map correlating cumulative HnP defects (dark regions) at maximum warpage locations over several test runs. (c) Reflow visualization showing the gap between solder sphere and SMT solder paste during a reflow cycle.

Table I. HnP Defect Rates for Various SMT Pastes

Paste Type	Head and Pillow Rate
Paste A	40%
Paste B	0%
Paste C	100%

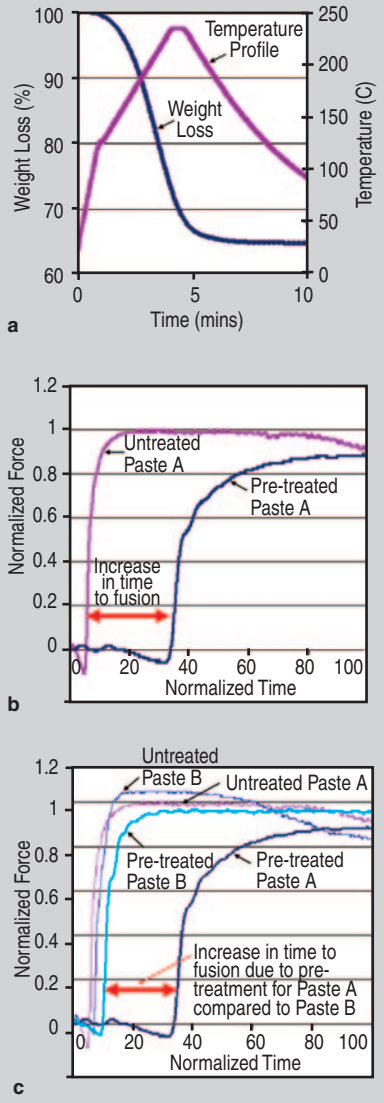


Figure 3. (a) TGA weight loss for paste A as a function of reflow profile. (b) Normalized paste wetting force versus time curve showing the increase in coalescence time of paste and solder balls due to pre-treatment. (c) The significant reduction in time to coalescence for Paste B compared to Paste A.

wetting force and time are then measured down to a ±0.01 mN resolution. Figure 3b shows the delay in wetting time (i.e. time for coalescence between the solder ball and paste) for paste A in both the un-treated and a pre-treated state. Un-treated paste A simulates no loss of contact between the paste and ball. Pre-treated paste A was pre-heated for several minutes above 200°C prior to coming into contact with the ball surface, which resulted in a 30% increase in coalescence time. This indicates that if the paste is allowed to begin activation prior to contact with the ball, the combined impact of oxidation and degradation of flux acids poses a high risk to form HnP defects. This delay in coalescence strongly correlates with the package HnP defects observed in actual builds, where locations of maximum dynamic warpage (i.e. shortest contact time) showed the highest frequency for HnP defects.

To assess the effect of flux activators on HnP defect formation, a systematic experiment was conducted using three different SMT pastes, each with composition Sn-3.0Ag-0.5Cu. Paste A was the control, whereas paste B was a known high activity paste with an acid activator package that resists degradation during reflow at elevated temperatures (>217°C), and paste C was a low temperature activation paste (~120–170°C). The results are detailed in Table I. As can be seen, there is a clear difference in HnP formation when paste type is modulated. Paste B showed no HnP defects, while paste C had 100% fallout under the same processing conditions. Thus, the flux activator has a significant impact on defect formation.

To validate the differences observed in HnP formation between pastes A and B during the SMT build, the Rhesca wetting technique was used to understand the fundamental differences in paste behavior. As shown in Figure 3c, paste B had much shorter time-to-coalescence than paste A (3× shorter) after an oxidizing pre-treatment. It can be reasoned then, that for a given reflow process, the flux activator within a solder paste allows for enhanced wetting during the "time above liquidus" and thus provides a significant process window where HnP defects are reduced. Additionally, the Rhesca wetting technique enables an efficient metrology to assess paste performance, and can be used to reduce the number of costly and time consuming package level experiments when solder candidates for SMT processing.

The actual volume of solder paste deposited onto the printed circuit board is another important aspect of HnP defect formation. The solder paste volume is directly controlled by the stencil aperture design and a good stencil design (i.e. aperture opening area and aspect ratio of the stencil aperture as compared to stencil thickness) is critical to ensure good release and transfer efficiency. Figure 4 shows data from five incremental aperture designs used to vary printed solder paste volume. As can be seen in the figure, HnP defects are observed at low paste volume (plus signs) while bridging defects are observed (crosses) at high paste volume. In this experiment, the packages were also baked in air at 125°C to increase the oxide thickness on the BGA solder ball, specifically to increase the signal of HnP fallout.

Effect of Solder Sphere Composition

Figure 5 shows a bar chart that depicts the HnP defect rate within electronic packages assembled on motherboards in an air reflow atmosphere using Sn-3.0Ag-0.5Cu solder balls from three different suppliers (designated W, X, and Y). As can be seen, HnP defect rates vary widely based on solder ball supplier—between 0% HnP defects for Y and 100% defects for X. Hence, although the nominal composition of all four solder balls is the same, the impurity levels must vary significantly.

Further evidence of the effect of solder sphere supplier, and impurity levels, is presented in Figure 6, which shows the solidification temperatures

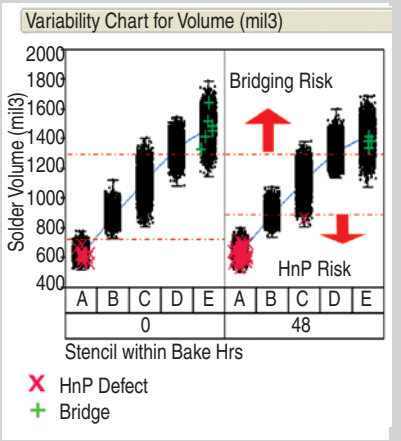


Figure 4. Impact of paste volume on the type of defects observed during SMT.

Table II. Surface Composition Analysis of Solder Balls from Four Different Suppliers Using TOF-SIMS Measurements*

Ion	Solder Ball Supplier W	X	Y
Tin	100.0	100.0	100.0
Silver	1.8	1.5	2.4
Copper	0.8	1.9	0.4
Element Q1	Medium	Low	Medium
Element Q2	Low	High	Low
Element Q3	ND	ND	High

* Values listed are the ratio of the counts for the ion/counts for Tin. ND = not detectable.

for the various solder balls from four different suppliers based on Differential Scanning Calorimetry (DSC) measurement when cooled at 2°C/sec (i.e. a standard cooling rate during SMT reflow). As can be seen, each supplier solder ball solidifies over a different temperature range with W showing the lowest solidification regime (between 166° and 180°C), whereas X has the highest, with solidification occurring between 206° and 196°C. The ternary eutectic in the Sn-Ag-Cu system occurs at a melting temperature of 217°C. Solder balls with lower solidus temperatures are beneficial in order to avoid HnP defects, since those solder balls stay molten for a longer time, provide a better wetting opportunity with the molten solder paste during reflow, and hence effectively increase the contact time needed to form a solder joint. The observations in Figure 6 correlate well with previous work conducted by Kang et al. which highlighted the link between impurity level, solder volume ,and the degree of undercooling in Sn-rich solders.[15–17]

To further investigate the elemental composition differences, time of flight secondary ion mass spectroscopy (TOF-SIMS) was used to characterize the surface of the solder balls. The literature is replete with studies that indicate that addition of certain elements to tin-based solder alloys causes these elements to segregate to the surface of the solder and change the surface tension and oxidation rate when molten.[18–22] Table II lists the surface composition analysis of the ball alloy from the three solder ball suppliers; for proprietary purposes, special elements are undisclosed and designated as element Q1, element Q2 and element Q3.

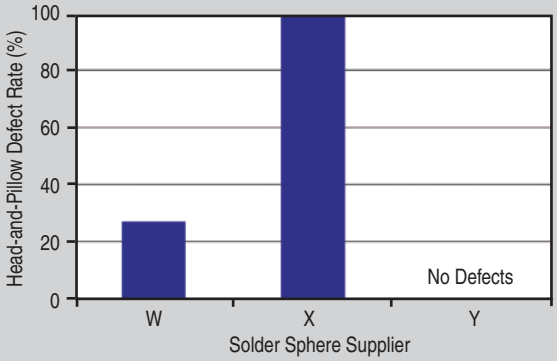


Figure 5. HnP defect rate variation with package supplier, solder ball supplier, and package type, for three different experiments involving package SMT assembly.

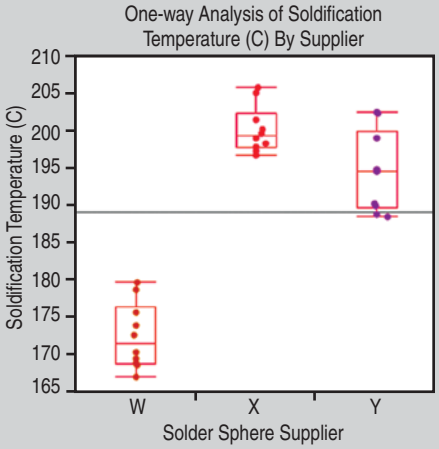


Figure 6. Solidification temperatures for Sn-3.0Ag-0.5Cu solder balls from four different suppliers, when cooled at 2°C/sec from above the liquidus temperature.

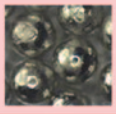
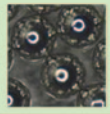
Solder Ball Supplier	W	X	Y
Element Q2	No	Yes	No
Element Q3	No	No	Yes
Appearance	Discoloration	Dull	Shiny
Discoloration			

Figure 7. The effect of element Q2 and element Q3 presence in Sn-3.0Ag-0.5Cu solder balls from 4 different suppliers on the appearance of solder balls after being oxidized in air at 200°C for 10 minutes.

The effect of elements Q2 and Q3 on the oxidation in air at elevated temperatures of Sn-3.0Ag-0.5Cu solder balls is illustrated in Figure 7. When these elements are not present (as is the case with solder balls from W), oxidation in air at 200°C for 10 minutes results in severe discoloration. When element Q2 is present as a dopant but element Q3 is not, as is the case with balls from Supplier X, oxidation under similar conditions results in a dull surface appearance, indicating a lower lever of oxidation as compared to W. However, when only element Q3 is present, as is the case in Y, oxidation is severely reduced as shown by the shiny appearance of the solder balls.

Lowering of the surface tension of the solder balls also enhances wettability of the molten solder balls[23] and reduces the contact time necessary for coalescence and solder joint formation. The presence of oxides on the surface of the molten solder balls will act as a barrier to wetting,[24] delaying coalescence between the solder ball and paste until the oxides are removed by the flux from the solder paste. If the oxidation level is lower on the surface of the solder balls, the time necessary for oxide removal is shortened, which will result in fewer HnP defects. Thus from a metallurgical standpoint, the presence or absence of the right elements provide the largest process window for SMT manufacturing through two key modulators: (1) increasing undercooling by removing impurities which act as heterogeneous nucleation sites for solidi-

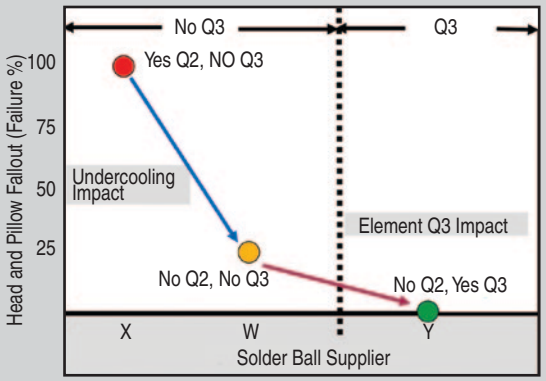


Figure 8. Illustration of how element Q2 and element Q3 in solder balls from three different suppliers affects the HnP defect rate when reflowed in air on to motherboards.

fication, and (2) decreasing the level of solder oxidation. Figure 8 provides a graphical representation of these two variables, and their effect of HnP defect rates for BGA packages.

CONCLUSIONS

The HnP defect is of great industrial importance in the electronics industry. Understanding of the solder ball/paste solidification/reflow behavior at the process-level is crucial for solving industry-wide microelectronic HnP defects concerns. The benefit of improved solder wetting has also been demonstrated. Solder pastes with more active fluxes help speed the process of wetting the two liquids by rapidly removing surface oxides allowing joints to form even if the contact time between molten balls and paste is short. Improved wetting can also be accomplished by controlling the solder alloy elements so that either the oxides are reduced to enable quick wetting, or the solidification undercooling is extended, which will increase the time available for good wetting.

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References

1. J. Bath, C. Handwerker, and E. Bradley, *Circ. Assemb.,* 11 (2000), pp. 30–40.
2. I.E. Anderson, J.C. Foley, B.A. Cook, J. Harringa, R.L. Terpstra, and O. Unal, *J. Electron. Mater.,* 30 (2001), pp. 1050–1059.
3. K.W. Moon et al., *J. Electron. Mater.,* 29 (10) (2000), pp. 1122–1136.
4. M.E. Loomans and M.E. Fine, *Metall. Mater. Trans. A,* 31A (4) (2000), pp. 1155–1162.
5. S.K. Kang, W.K. Choi, D.-Y, Shih, D.W. Hendreson, T. Gosselin, A. Sarkhel, S. Goldsmith, and K.J. Puttlitz, *JOM,* 55 (6) (2003), pp. 61–65.
6. D.R. Frear, J.W. Jang, J.K. Lin, and C. Zhang, *JOM,* 53 (6) (2001), pp. 28–32.
7. K.S. Kim et al., *Mater. Sci. and Eng.,* A333 (2002), pp. 106–114.
8. D.W. Henderson et al., *J. Mater. Res.,* 17 (11) (2002), pp. 2775–2778.
9. M.P. Renavikar et al., *Intel Tech. J.,* 12 (1) (2008), pp. 1–15.
10. J. Bath and R. Garcia, *Proceedings of SMTAi Conference* (Edina, MN: SMTA Pub. Dept., 2009), pp. 430–437.
11. W.W. Chin et al., *Proceedings of SMTAi Conference* (Edina, MN: SMTA Pub. Dept., 2006), pp. 100-106.
12. D. Amir et al., in Ref. 10, pp. 430–437.
13. M. Shimamura et al., in Ref. 10, pp. 422–429.
14. S. Vandervoort et al., in Ref. 10, pp. 438–446.
15. S.K. Kang et al., *Electr. Comp. and Tech. Conf.* (Piscataway, NJ: IEEE, 2007), pp. 1597–1603.
16. M.G. Cho et al., *J. Mater. Res.,* 23 (2008), pp. 1147–1158.
17. S.K. Kang et al., *J. Mater. Res.,* 22 (2007), pp. 557–560.
18. K.L. Lin and T.P. Liu, *Oxidation of Metals,* 50 (1998), pp. 3–4.
19. X. Chen et al., *Proc. 6th Int. Conf. of Electr. Packag. Tech. (ECTC)* (Piscataway, NJ: IEEE, 2005), pp. 211–217.
20. E.E. de Kluizenaar, *J. Vacuum Sci. and Tech.,* 1 (3) (1983), pp. 1480–1485.
21. Y.Y. Lee, H.W. Tseng, Y.H. Hsaio, and C.Y. Liu, *JOM,* 61 (6) (2009), pp. 52–58.
22. F. Guo, M. Zhao, Z. Xia, Y.P. Lei, X.Y. Li, and Y. Shi, *JOM,* 61 (6) (2009), pp. 39–44.
23. D. Cavasin, *Proc. 6th Int. Conf. of Electr. Packag. Tech. (ECTC),* (Piscataway, NJ: IEEE, 2005), pp. 1060–1063.
24. Y.H. Wang et al., *Mater. Trans.,* 46 (2005), pp. 2431-2436.

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