The Material Optimization and Reliability Characterization of an Indium-Solder Thermal Interface Material for CPU Packaging

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Developing new thermal interface materials (TIMs) is a key activity to meeting package thermal performance requirements for future generations of microprocessors. Indium solder is capable of demonstrating end-of-line performance to meet current technology targets due to its inherent high thermal conductivity. However, improving its reliability performance, particularly in temperature cycling, is a challenge. This study describes the failure mechanisms and reliability performance of indium solder TIM as a function of integrated heat spreader metallization thickness, TIM bond line thickness, and die size. Also studeied were the steps taken to improve its temperature cycle performance. Analyses were performed using thermal resistance measurements, scanning-electron microscopy, scanning-acoustic microscopy, and transmission-electron microscopy to characterize the solder TIM thermal performance, interfacial microstructure, and failure mechanisms.

INTRODUCTION

As the number of transistors on the chip double every 18 months, a host of new micro-architectures from factors that leverage Moore's Law are evolving. These will continue to demand thermal solutions to dissipate power density from the chip to meet thermal requirements and thus ensure its reliable performance. Currently, a copper heat spreader is used to spread the heat away from the die. A thermal interface material (TIM) connects the copper heat spreader to the silicon die, as shown in Figure 1.

At a higher level, the two critical functions of a TIM in a flip-chip package are to dissipate heat from the die to allow higher processing speeds and to absorb strain resulting from the mismatch of coefficients of thermal expansion (CTE) of the die, substrate, and the integrated heat spreader (IHS) during temperature cycling. Historically, at Intel Corporation, a polymer TIM has been used as a thermal interface material solution. Polymer TIMs with maximum possible loading of conductive fillers demonstrate bulk thermal conductivities in the 4–5 W/mK range. But with higher operating die temperatures, a material with

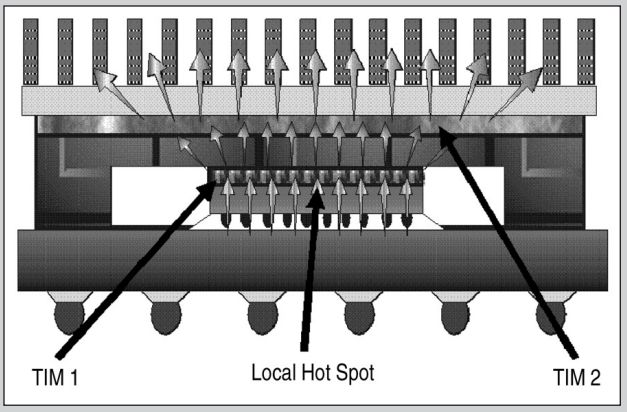


Figure 1. A flip-chip ball grid array package with thermal interface materials between the die and the IHS and the heat sink.

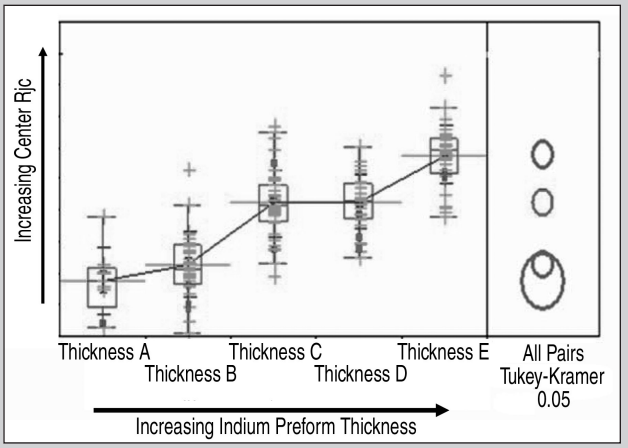


Figure 2. The EOL center Rjc versus preform thickness.

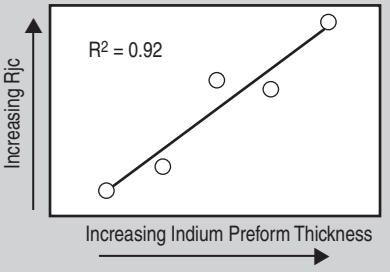


Figure 3. The mean EOL Center Rjc versus bond line thickness.

OPTIMIZATION OF IHS GOLD METALLIZATION THICKNESS

During the development of solder thermal interface material (TIM) packaging technology at Intel Corporation, considerable work was put into optimizing the gold plating thickness to maximize thermal performance while minimizing gold plating thickness (and therefore cost).

Gold is used on the integrated heat spreader (IHS) cavity to provide an oxide-free surface that facilitates soldering. A continuous porosity-free gold layer that completely covers the nickel is desired. In general, thinner gold is desirable on the IHS. Not only are raw material costs reduced, but also the presence of thick gold indium intermetallics, which are known to compromise mechanical properties, can be avoided.[4–7]

However, excessively thin gold must also be avoided. In practice, gold plating thickness is limited by the electrolytic gold plating process used by Intel's suppliers wherein at extremely low thicknesses the gold starts to become discontinuous. As seen in Figure A, electrolytic gold plating onto nickel starts begins with the nucleation of gold "islands" on a "sea of nickel." As the nucleation sites grow, they converge to form a continuous layer of gold covering the nickel (see Figure B).

Materials and Methods

A single experiment was run using IHSes of varying gold plating thickness. To make the parts, Intel's IHS supplier was asked to intentionally vary the plating time. These units were built into simulated electronic packages at Intel Corporation.

The units were split into two groups and the solder was reflowed using the two oven profiles, hereafter referred to as "reflow process A" and "reflow process B." Following assembly (i.e., end-of-line [EOL]), the packages were subjected to thermal resistance measurements (i.e., Rjc measurements) as well as ultrasonic voiding measurements. Rjc is the thermal impedance from the junction to the case in the assembled package and was measured in the center as well as the corner of the package. The same measurements were also made after thermal cycling.

Results

As seen in Figures C and D, gold thickness had no effect on EOL thermal performance for reflow profile A. However, degradation in the center Rjc increases with increasing thermal cycling and increasing gold thickness. The corner Rjc also increases with increasing thermal cycling; however, slightly thicker gold appears to be beneficial to thermal performance with profile A.

The interaction between increasing gold thickness and increasing thermal cycling

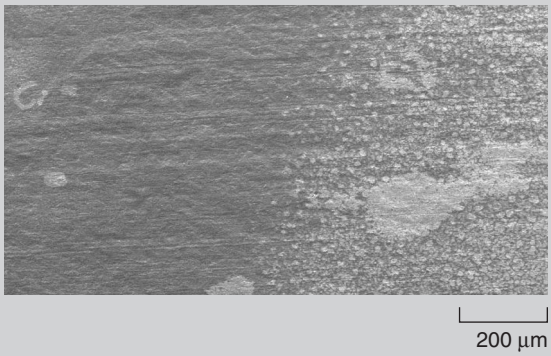


Figure A. A scanning-electron micrograph (upper portion) showing discontinuous gold plating (light phase) on the nickel-plated IHS (dark background) for an IHS plated below the supplier's lower manufacturing limit.

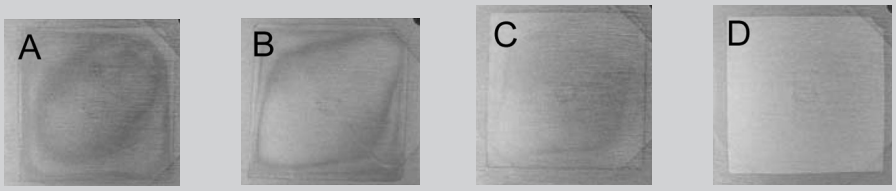


Figure B. Photographs of the gold plating in the IHS cavity (plating thickness A<B<C<D).

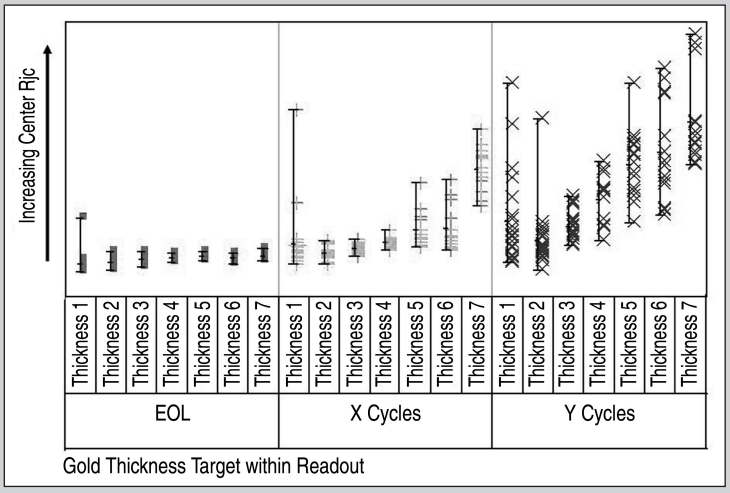


Figure C. The center Rjc as a function of target gold plating thickness for reflow profile A. "Thickness 1 to 7" indicates increasing gold thickness.

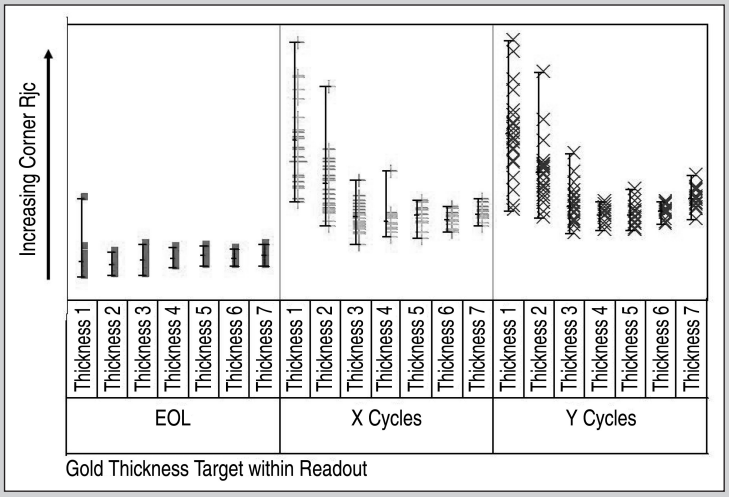


Figure D. The corner Rjc as a function of target gold plating thickness for reflow profile A. "Thickness 1 to 7" indicates increasing gold thickness.

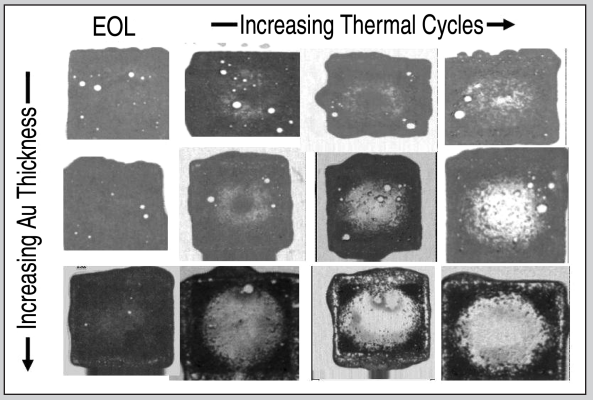


Figure E. Ultrasonic images of the solder TIM bondline in packages as a function of gold thickness and thermal cycles.

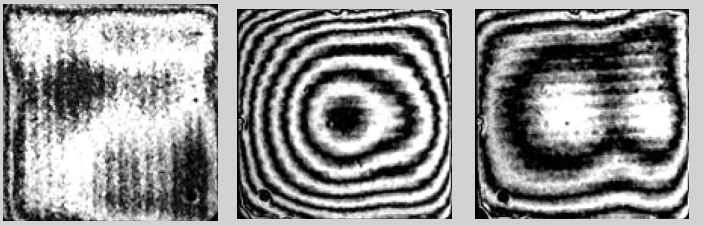


Figure F. Moiré fringe images of Intel IHSes (a) in the as-received condition; (b) attached to a package and measured at room temperature; (c) attached to a package and measured under isothermal elevated temperature conditions. Each fringe (black to white to black) corresponds to 12.5 μm.

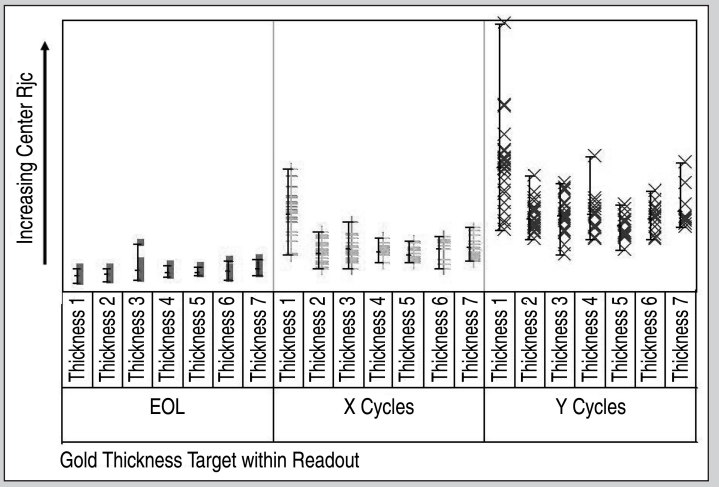


Figure G. The center Rjc as a function of target gold plating thickness for the reflow profile B. "Thickness 1 to 7" indicates increasing gold thickness.

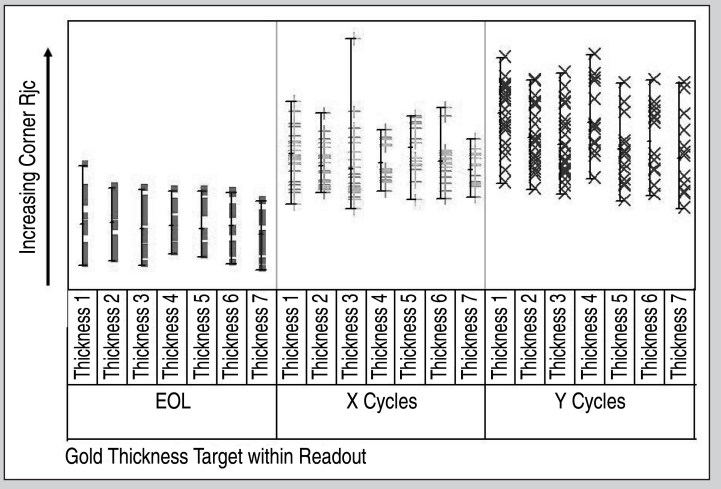


Figure H. The corner Rjc as a function of target gold plating thickness for reflow profile B. "Thickness 1 to 7" indicates increasing gold thickness.

has been seen in other experiments conducted at Intel Corporation (details on the experiment will not be given here, see Figure E for results) and is attributed to thermal-cycling-driven fatigue cracking between the indium and the indium-gold intermetallic. Stresses are created in the solder bondline in the assembled package as during thermal cycling due to the differing coefficients of thermal expansion of the package components (see Figure F). When thermally cycled to extremely long readouts, the stresses in the package can lead to growth of fatigue cracks in the solder TIM.

With the reflow profile B there was no effect of gold plating thickness on thermal performance (either EOL or post-thermal cycling) over intermediate thickness ranges, as shown in Figures G and H. However, inferior thermal performance was seen when the IHS supplier attempted to plate at the lowest thickness range.

Discussion

Experiments executed to date on reflow profile B show that thermal performance is unaffected by gold thickness over the majority of the range investigated. This is in contrast to reflow profile A which showed a "sweet spot" in gold plating thickness. It is known from the literature that excessively thick gold can lead to thick intermetallic formation, which in turn, can compromise mechanical properties. However, in the regime investigated in Intel Corporation's experiments more subtle trends were seen, and in some cases improved performance was actually seen with slightly thicker gold.

The optimal gold plating thickness on an IHS, in principle, depends on many factors including the reflow oven profile, the geometry of the electronic package, and the coefficients of thermal expansion of the package components.

a higher bulk thermal conductivity is required to carry heat away from the die and therefore meet the package thermal resistance requirements.

The feasibility of solder, and in particular indium, as a thermal interface material to shift the package resistance down to the required limits has been demonstrated.[1–3] Although solders have a significant thermal advantage over polymer TIMs (5X to 20X higher in bulk thermal conductivity), implementation of solder TIMs is challenging due to significant reliability and process issues.

This study deals with optimizing the small-die indium solder TIM materials set and subsequently the characterization of the typical failure mechanisms during temperature cycling.

See the sidebar on pages 68–69 for details on the optimization of IHS gold metallization thickness.

BOND LINE THICKNESS

The current study centers on tailoring the indium solder bond line thickness (BLT) to meet the end-of-line (EOL) thermal targets and to provide for optimal package thermal and reliability performance. Experiments were conducted on five preform thicknesses.

The results in the following sections show that the TIM BLT had a profound effect on the EOL thermal resistance measurements (TRES) and the reliability performance of the package. It was demonstrated that the EOL thermal resistance decreased as the TIM BLT decreased and the temperature cycling performance improved as the solder TIM BLT increased.

Materials and Methods

The solder preform thickness was varied. Reliability testing readouts were taken at numerous intermediate points. These readouts included TRES and scanning acoustic microscopy (CSAM) images. Samples were then thermally cycled with readouts taken after several hundred cycles.

RESULTS

Figure 2 is a plot of center Rjc versus initial preform thickness. Figure 3, which displays the mean EOL center Rjc versus preform thickness, shows a positive linear correlation between Rjc and preform thickness ($R^2 = 0.92$).

Figure 4 displays the EOL solder TIM voiding and a function of preform thickness. As seen, voiding can be kept low by keeping the preform thick.

Figure 5 displays the center Rjc after several hundred thermal cycles. The thicker preforms are statistically equivalent. The thinnest preform degraded substantially.

Figure 6 shows the corner Rjc after several hundred thermal cycles. The thicker preforms are statistically equivalent. The thinnest preform degraded substantially.

Discussion

The EOL Rjc is driven by the inherent thermal conductivity of indium (86 W/mK) and the associated preform thickness. Theoretical calculations show that thermal resistivity of indium increases by 0.0029°Ccm^2/W per 30 μm increase in

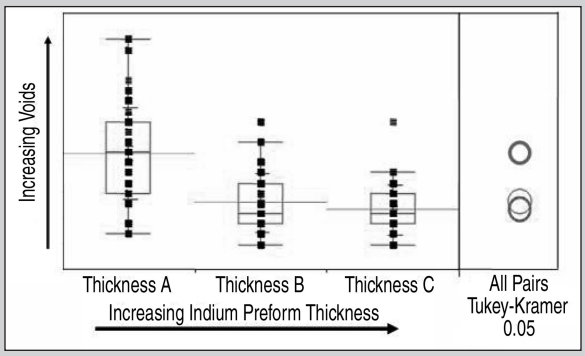


Figure 4. The EOL void percentage versus preform thickness.

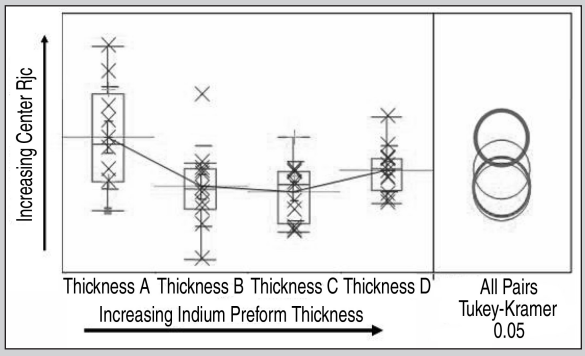


Figure 5. The center Rjc versus preform thickness after several hundred thermal cycles.

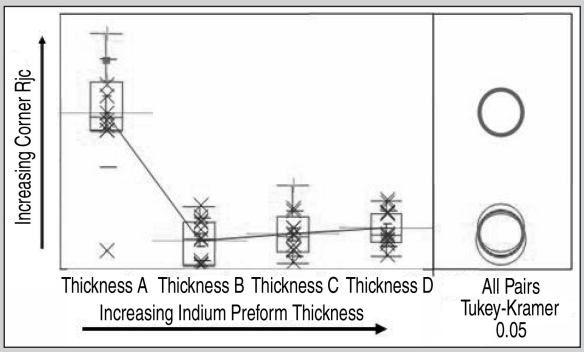


Figure 6. The corner Rjc versus preform thickness after several hundred thermal cycles.

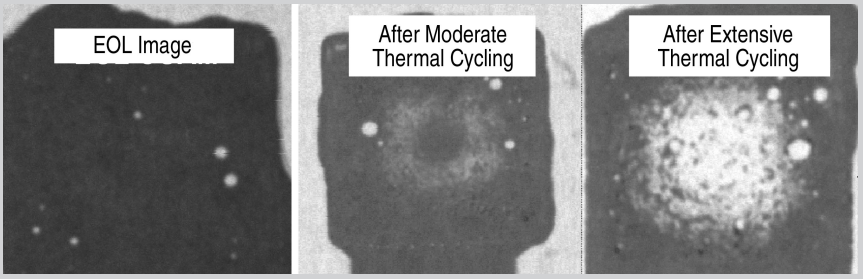


Figure 7. Typical non-enabled small die TIM-to-IHS CSAM images from multiple stress readouts.

Table I. Material Set, Stress Conditions, and Package Type

Input Factor	Description	Notes
Stress Condition	Temperature cycle (undisclosed)	
Package Type	FCXGA w/IHS	35 × 35 mm for small and medium die
Package Type	FCXGA w/IHS	42.5 × 52.5 mm for large die
Die Size	Small die	x ~ 10 mm
		y ~ 13 mm
Die Size	Medium die	x ~ 18 mm
		y ~ 15 mm
Die Size	Large die	x ~ 23 mm
		y ~ 23 mm

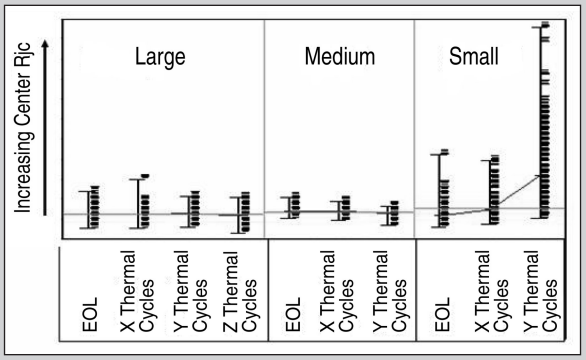


Figure 8. A variability chart for center Rjc for multiple die sizes as a function of thermal cycles where X < Y < Z.

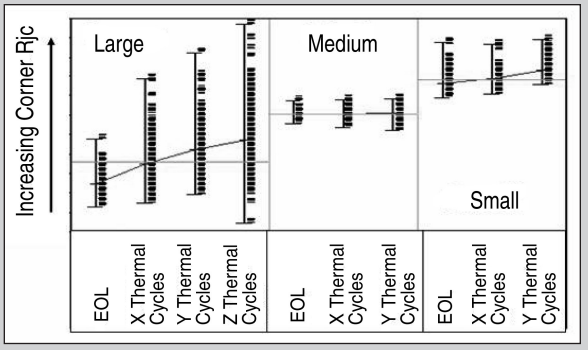


Figure 9. A variability chart for corner Rjc for multiple die sizes as a function of thermal cycles where X < Y < Z.

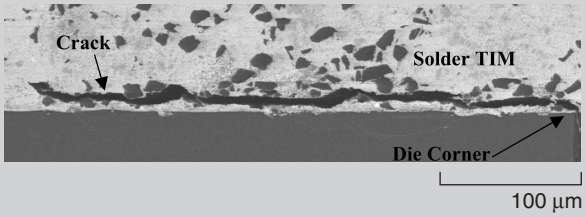


Figure 10. Small die corner cracking.

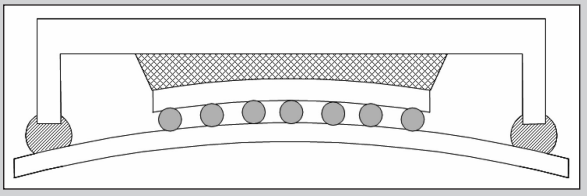


Figure 11. A cross-section representation of a C4 package with IHS post end-of-line processing (warpage exaggerated).

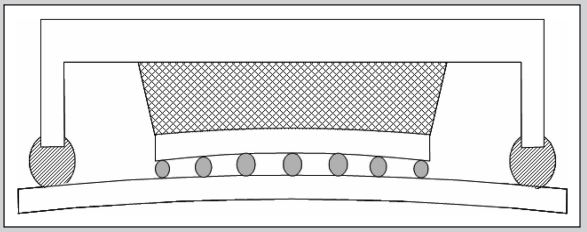


Figure 12. An exaggerated cross-section representation of a "flattened" C4 package with IHS at elevated temperatures.

preform thickness. The linear fit model, Figure 3, exhibited a good correlation to theory with a 0.003°Ccm^2/W increase (slope of line) in thermal resistance per 30 μm preform thickness.

Thicker preforms reduce corner and center Rjc degradation during temperature cycling (Figures 5 and 6, respectively). The enhanced degradation at lower preform thicknesses appears to be due to the inability of the thinner interface to absorb the associated package stresses during temperature cycling. Further, modeling results have shown that thinner preforms increase thin film cracking risk through temperature cycling because of the associated enhanced lid-to-die coupling.[1] Clearly, there is a tradeoff between optimal performance at EOL (thinner preforms) and after temperature cycling (thicker preforms). There appears to be a sweet spot where good EOL thermal performance and adequate reliability performance exist.

DIE-SIZE DEPENDENCE

The change from polymer to solder-based materials has resulted in a change in TIM performance over the product life. The combined changes of CTE, tensile strength, elastic deformation, and other material properties have changed the thermal degradation and failure mechanisms of small to large die products. The materials set, stress conditions, and package types utilized in this experiment are displayed in Table I.

Results

The center degradation of solder TIM units can be divided into a crack initiation phase and a crack propagation phase. Figure 7 shows typical small-die CSAM images taken at different intervals of unit testing. At low thermal cycles the initiation of small micro-cracks can be seen, but does not impact thermal performance. At higher thermal cycles the cracks have propagated across the entire center region of the die and significantly degrade thermal performance. This failure mechanism is predominant on small die form factors.

The center degradation mode is not observed, as the die size is increased to the large and medium sizes (Figure 8).

Corner degradation is observed on the small, medium, and large die sizes. The degradation rate generally increases with

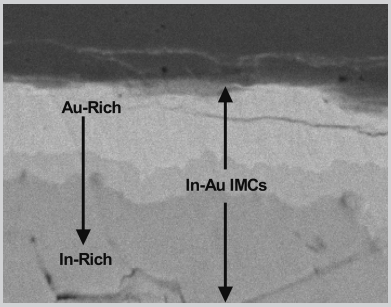
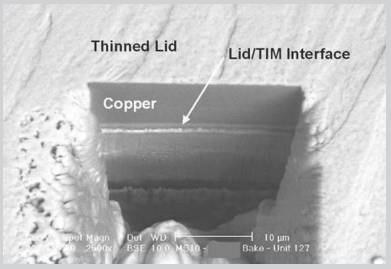
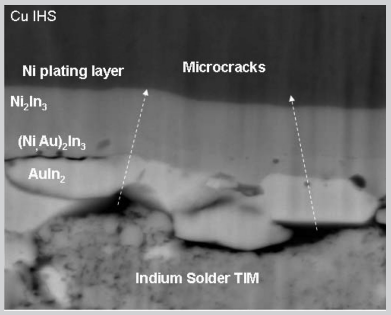


Figure 13. A backscattered-electron SEM image showing three distinct In-Au IMCs.



a



b 3 μm

Figure 14. (a) A FIB cross section with (b) subsequent SEM-EDS of lid/TIM interface after several hundred thermal cycles.

die size (see Figure 9) and is linear in behavior. Cracking (Figure 10) originates at the die corner and propagates into the bulk TIM.

Discussion

Figure 11 is a cross-section representation of a C4 package with an integrated heat sink that shows how the package changes over a temperature range. An assembled package at room temperature (Figure 11) has a fixed amount of die and package substrate warpage. As the temperature is increased the package will flatten (Figure 12). The flattening is primarily driven by the thermal expansion of the substrate. As the package warpage is reduced, the die is pulled away from the relatively rigid integrated heat sink (this behavior is exaggerated in Figure 12), which creates a tensile stress and ultimately a crack in the solder TIM. The stress concentration of this tensile force is roughly dependent on the die size and will change how the material degrades during stress.

Conclusions

In small-die form factors, center degradation due to tensile stresses in the TIM occurs and results in a degradation of the IHS-to-TIM interface. Large-die degradation is dominated by a combination of tensile and shear stresses that cause cracks to originate at the die corners at the die-to-TIM interface.

INTERFACIAL CHARACTERIZATION

In order to properly understand the failure modes in solder TIM, it was necessary to gain an in-depth understanding of the metallurgical system near the die/TIM and IHS/TIM interfaces. To this end, many analyses were performed to determine the thickness, stoichiometry, and morphology of intermetallic compounds (IMCs) forming at these interfaces of the plan-of-record materials set.

Materials and Methods

Techniques including scanning-electron microscopy (SEM) with energy-dispersive-x-ray analysis (EDS), focused-ion beam (FIB), and transmission-electron microscopy (TEM) were utilized depending on the level of detail needed. Traditional cross-sectioning and the use of techniques such as IHS or lid pull with subsequent SEM-EDS analysis allowed the confirmation of the presence of IMCs, a rough estimate of their thickness, and a qualitative idea regarding stoichiometry.

For example, using backscattered-electron imaging, multiple In-Au IMCs were distinguished by their grayscale, with gold-rich IMCs appearing relatively brighter than indium-rich IMCs. This is shown in Figure 13. Although EDS confirmed the differences, it was unable to properly quantify the stoichiometry.

Due to the inherent smearing of indium and its IMCs during traditional polishing, crack paths and IMC thickness can be ambiguous and misleading. More detail and accurate measurements can be obtained by employing FIB cross-sectioning with subsequent SEM-EDS. During FIB sectioning, a wedge-shaped section of material is removed, with the wedge wall containing the cross section of interest, as shown in Figure 14a. Figure 14b shows the successful application of FIB and subsequent SEM-EDS to characterize the lid/TIM interface after several thousand hours of bake well above 100°C. With FIB, the interfaces and stratification of In-Ni IMCs and In-Au IMC remains intact, allowing for accurate thickness measurements. In this case, the IMC composition could also be well detected, as shown, using EDS. While the stoichiometry was also determined in detail from a separate TEM analysis of a similar part, the composition determined from the FIB/SEM/EDS characterization is rather consistent with TEM findings.

Results on POR Materials Set

The most accurate details regarding the stoichiometry, morphology, and thickness of the IMCs were obtained

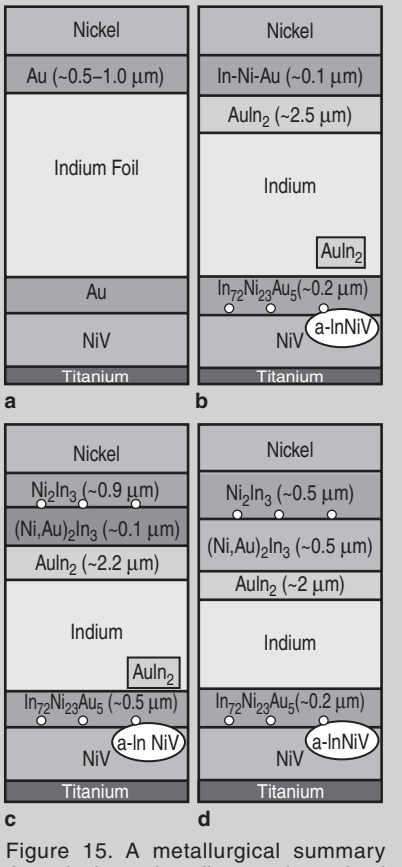


Figure 15. A metallurgical summary through thermal cycling as determined by TEM analyses. (a) Pre-assembly, (b) after assembly, (c) after moderate thermal cycling and (d) after extensive thermal cycling.

from the TEM. Through TEM analyses, the complete evolution of the microstructure and stoichiometry of the In-Ni-Au system through temperature cycling was obtained.

The comprehensive results, illustrated in Figures 15 and 16, provided a deeper understanding of the metallurgical system. This allowed for the proper identification of the IMC involved with the interface failing during thermal cycling. When molten indium reacts with thin gold lid metallizations, the self-limiting formation of $AuIn_2$ occurs between the indium and gold. The driving force for formation of the particular intermetallic is the zero solubility of gold in indium and the concentration of elements at the interface (e.g., high concentration of indium). The kinetics of the Au/In interfacial reaction follow the parabolic law and the growth of the IMC is diffusion controlled.[8]

A secondary ternary In-Ni-Au IMC also forms between the nickel layer and the $AuIn_2$ IMC (the exact stoichiometry was not determined). The reaction is believed to be between nickel- and gold-rich IMC, instead of nickel and indium.

Subsequently, after several hundred thermal cycles, three distinct IMCs are formed on the IHS side. Energy-dispersive x-ray analysis indicates that the layer adjacent to the nickel coating is Ni_2In_3, the middle IMC was $(Ni,Au)_2In_3$, and $AuIn_2$ is adjacent to the indium. The $AuIn_2$ thickness decreases and the underlying In-Ni IMC thickness increases at elevated temperatures. As documented in the literature, indium and gold combine to form $AuIn_2$ during initial reflow and disperse into the indium during elevated-temperature exposure.[4] Conversely, the In-Ni IMC continues to grow since the majority of the nickel does not appear to precipitate and disperse from the In-Ni IMC. The small Kirkendall voids along the $(Ni, Au)_2In_3/Ni_2In_3$ interface (Figure 15) accompanied the formation of Ni_2In_3 layer. The fact that small voids were formed between $(Ni,Au)_2In_3/Ni_2In_3$ instead of Ni_2In_3/Ni interface indicates indium diffuses faster than nickel through the Ni_2In_3 IMC. Although the Kirkendall voids are present throughout temperature cycling, they do not play a role in the failure mechanism of the system.

The stoichiometry of the $AuIn_2$ layer is consistent with the Au-In phase diagram and the stoichiometry of the Ni_2In_3 layer is consistent with the Ni-In phase diagram.[9]

On the solder-to-die side, two IMCs form immediately after reflow, $AuIn_2$ and $In_{72}Ni_{23}Au_5$. The $AuIn_2$ IMC is discontinuous due to the lower gold thickness on the die side and disperses into the indium after solid-state elevated temperature exposure (Figure 16). The $In_{72}Ni_{23}Au_5$ IMC is continuous and thickens through temperature cycling. It appears that this ternary IMC is the $In_{72}Ni_{28}$ IMC with some gold substituting for the nickel. Kirkendall voids do occur along the solder-to-die interface, but they do not contribute to the failure of the system.

From lid pull and subsequent SEM-EDS, it could be determined that the failure was between an In-Au IMC and

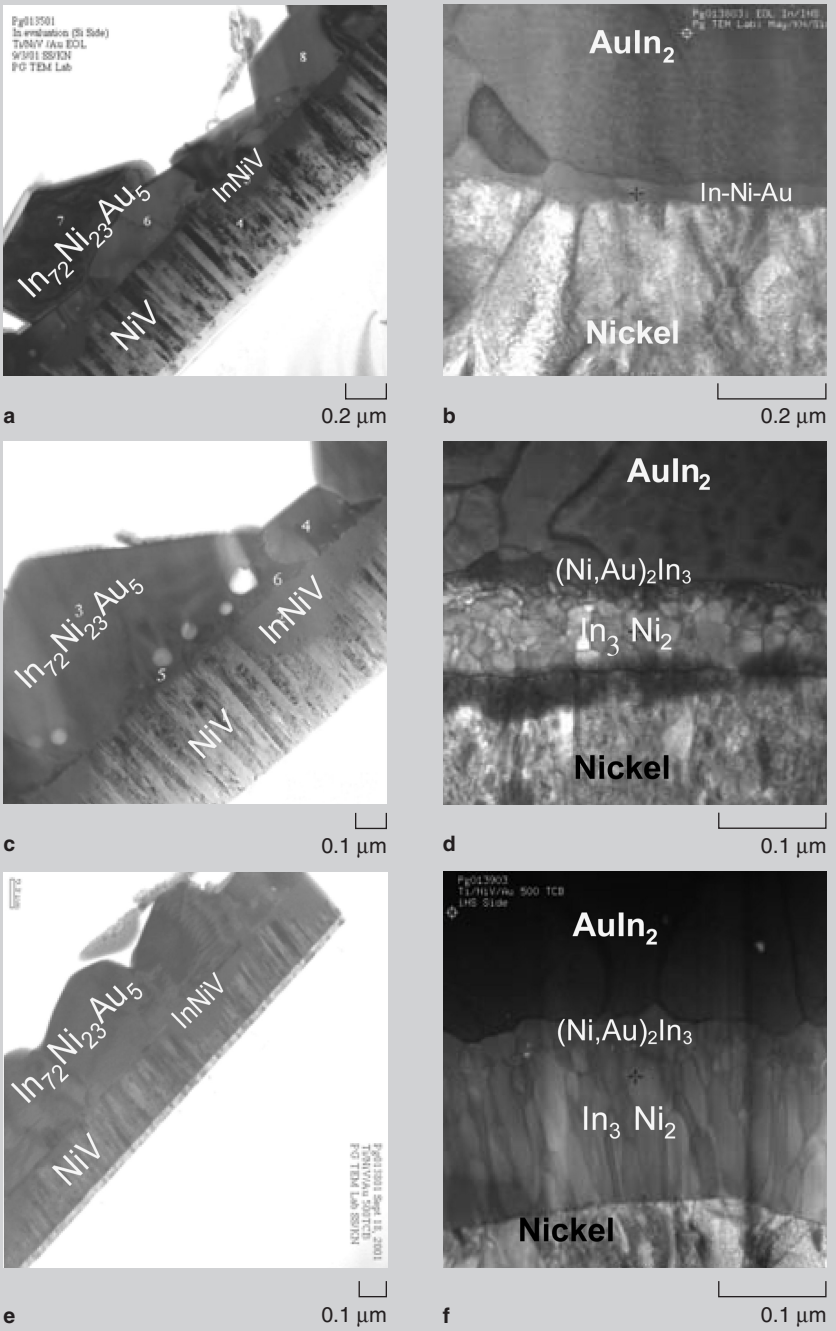


Figure 16. A metallurgical summary through thermal cycling as determined by TEM analysis. (a) die side–EOL, (b) lid side–EOL; (c) die side after moderate thermal cycling; (d) lid side after extensive thermal cycling; (e) die side after moderate thermal cycling; (f) lid side after extensive thermal cycling (courtesy of Khairul Mohammad and Sim Kian Sin).

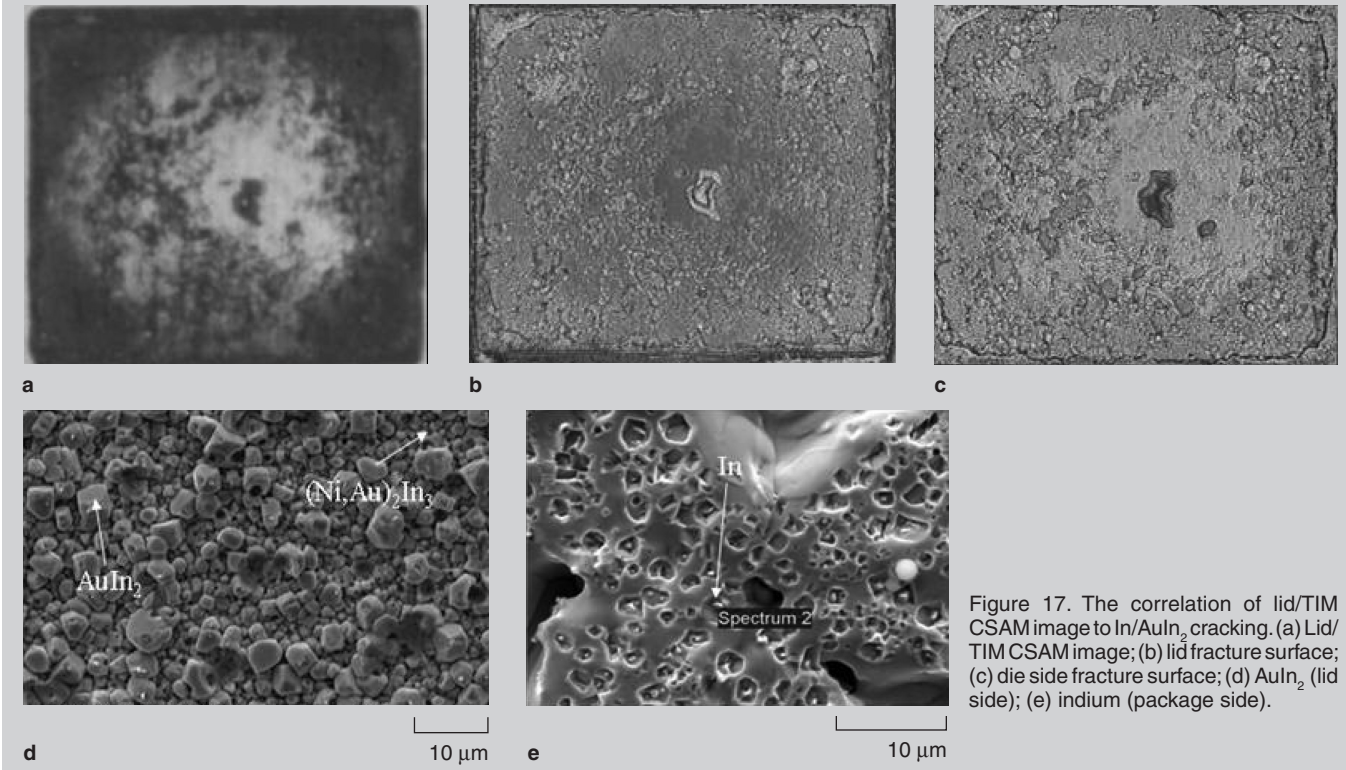


Figure 17. The correlation of lid/TIM CSAM image to $In/AuIn_2$ cracking. (a) Lid/TIM CSAM image; (b) lid fracture surface; (c) die side fracture surface; (d) $AuIn_2$ (lid side); (e) indium (package side).

bulk indium, predominantly on the lid side. However, it was the TEM analysis, which identified the IMC as $AuIn_2$, that proved to be important, as this is the predominant failure mode for solder TIM on small die.

Figure 17 illustrates this failure mode, its correlation to lid/TIM CSAM, and the morphology of the $AuIn_2$ IMC. Figure 17a shows the CSAM image of the lid/TIM interface after several hundred thermal cycles, with light areas indicating cracking. The corresponding optical images of the fracture surfaces are shown in Figure 17b and c. These images exhibit a direct correlation to the CSAM image. Figure 17d and e are SEM images of the fracture surfaces on the lid and die side, respectively. The nodular nature of the $AuIn_2$ and the ternary In-Ni-Au IMCs can be observed from the SEM images on the lid side. On the substrate or die side, pure indium is observed (dimpled from contact with the gold-based nodules). During temperature cycling, cracks are formed at this interface between gold-based IMCs and indium and lid-pull confirms that to be the weakest interface that fractures during the post-thermal cycling pull test. As can be expected, the nodular nature of the gold-based IMCs likely results in the nodules acting as stress concentration sites during thermal cycling, resulting in the fracture.

When both sides of the fracture were examined, it was found that the lid surface consisted of $AuIn_2$ while the package side was comprised of indium, dimpled from contact with the $AuIn_2$. This is illustrated in the SEM micrographs of Figure 17d and e.

CONCLUSION

The reliability performance of indium solder TIM is generally improved by decreasing the IHS gold metallization thickness and increasing the BLT. However, excessively thin gold must be avoided and slightly thicker gold actually performs better in some cases. Further, there is a tradeoff between optimal performance at EOL (lower BLT) and after temperature cycling (higher BLT). The sweet spot is where good EOL thermal performance and adequate reliability performance exist. The failure mode of the indium TIM modulates with the dimensions of the die from tensile to shear. For small die products, the predominant failure mode is between the $AuIn_2$ IMC and bulk indium at the solder-to-IHS interface.

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