## An improved multiplier-free feed-forward carrier phase estimation for dual-polarization QPSK modulation format\*

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An improved multiplier-free feed-forward carrier phase estimation algorithm is proposed for dual-polarization quadrature-phase-shift-keying (DP-QPSK) with coherent detection. The bit error rate (BER) performance, block length effect and linewidth tolerance of the proposed algorithm are evaluated for a 112 Gbit/s DP-QPSK system. A linewidth symbol duration product of  $2.9\times10^{-4}$  is demonstrated for 1 dB optical signal-to-noise-ratio (OSNR) penalty at BER of  $10^{-3}$  for the proposed algorithm. The hardware complexity of the proposed multiplier-free algorithm is demonstrated to be much lower than that of the 4th power algorithm.

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Recently, dual-polarization quadrature phase-shift keying (DP-QPSK) combined with coherent detection has attracted considerable attention for long-haul transmission due to its high spectrum efficiency and its resilience to physical impairments, such as optical filtering<sup>[1]</sup>, chromatic dispersion<sup>[2]</sup> and polarization mode dispersion<sup>[3]</sup>.

For coherent optical transmission systems, carrier phase estimation (CPE) is one of the important receiver functions implemented with digital signal processing (DSP). There are two kinds of carrier phase estimations: feed-back and feed-forward methods. For feed-back method, such as phase locked loop (PLL), it suffers from the poor linewidth tolerance and feed-back processing latency<sup>[4]</sup>. For QPSK modulation format, the most widely used feed-forward CPE algorithm is the well-known 4th power algorithm<sup>[5]</sup>. However, the chip resource consuming multiplier operation in 4th power algorithm becomes a challenge for current DSP technology for optical signals with high symbol rate. Recently, Tao et al<sup>[6]</sup> proposed a multiplier-free algorithm based on pre-decision in order to reduce the hardware complexity. Nevertheless, the feed-back pre-decision results in a processing latency and complicates the hardware implementation, which was not considered in Ref.[6]. Qi et al<sup>[7]</sup> introduced another multiplier-free CPE algorithm based on a reference phase. However, due to the limitation of the proposed

algorithm, a feed-back pre-compensation was required, which results in additional hardware complexity for the carrier phase recovery. The proposed algorithms in Refs.[6] and [7] are not real feed-forward architecture, which would suffer from feed-back processing latency critical for parallelized implementation.

In this paper, we propose a novel multiplier-free feed-forward CPE algorithm for low-complexity carrier phase recovery for DP-QPSK modulation format. For the proposed algorithm, a reference vector is introduced by only using adder, logic operation and look up table (LUT) for CPE. Multiplier-free is achieved for the proposed algorithm. The bit error rate (BER) performance, block length effect, linewidth tolerance and the hardware complexity of the proposed algorithm are investigated.

The symbols for the QPSK modulation format with phase noise can be expressed as

$$S = R \times \exp[j(\theta_s + \theta_{N})], \qquad (1)$$

where  $R=\sqrt{2}$  is the radius,  $\theta_s \in \{\pi/4, 3\pi/4, 5\pi/4, 7\pi/4\}$  is the phase modulation, and  $\theta_N$  represents the laser phase noise. In order to avoid the 4th power operation, a phase reference is introduced for CPE<sup>[7]</sup>

$$\theta_{\text{ref}} = \text{sign}(I) \cdot \text{sign}(Q) \cdot (|I| - |Q|),$$
 (2)

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where  $\operatorname{sign}(\cdot)$  is the sign function, I is the in-phase component of the signal, and Q is the quadrature component of the signal. Considering the phase modulation for each quadrant separately, Fig.1 shows that the phase reference  $\theta_{\text{ref}}$  is identical for all quadrants for QPSK symbols, and the phase modulation of the signal is removed.

Quadrant 2 Quadrant 1
$$\theta_{ref} = R[-|\cos(\theta_{N} + 3\pi/4)| + |\sin(\theta_{N} + 3\pi/4)|] = -\sqrt{2}R\sin(\theta_{N})$$

$$\theta_{ref} = R[|\cos(\theta_{N} + \pi/4)|] = -\sqrt{2}R\sin(\theta_{N})$$

$$\theta_{ref} = R[|\cos(\theta_{N} + 5\pi/4)|] = -\sqrt{2}R\sin(\theta_{N})$$

$$\theta_{ref} = R[-|\cos(\theta_{N} + 7\pi/4)| + |\sin(\theta_{N} + 7\pi/4)|] = -\sqrt{2}R\sin(\theta_{N})$$
Quadrant 3
Quadrant 4

Fig.1 Phase reference for symbols in each quadrant

In Ref.[7], laser phase noise was directly estimated from the reference phase. However, due to the limitation of this method, a feed-back pre-compensation was required for correct estimation. In order to avoid the feedback pre-compensation operation, four times laser phase noise product  $4\hat{\theta}_{\rm N}$  is first estimated according to

$$4\hat{\theta}_{N} \approx -\pi / R \cdot \theta_{ref} \approx -9/16 \cdot \theta_{ref}$$
 (3)

Then the four times estimated phase noise product  $4\hat{\theta}_N$  is used to create a reference vector by using  $\exp(j\cdot)$  operation. The  $\exp(j\cdot)$  operation can be easily achieved by using LUT operation. In this paper, we consider the computationally efficient block averaging approach. Then an estimation of the laser phase noise for a block of M symbols is obtained by

$$\theta_{\text{est}} = \frac{1}{4} \arg \sum_{k=1}^{M} \exp(\mathbf{j} \cdot 4\hat{\theta}_{N,k}) \quad . \tag{4}$$

The multiplications in Eqs.(3) and (4) can be achieved by shift operations and adders. No multiplier is required in the proposed feed-forward CPE algorithm. The principle of carrier phase recovery based on the proposed multiplier-free CPE algorithm is illustrated in Fig.2. We denote it as the MF algorithm. Compared with the previous algorithms in Refs.[6] and [7], multiplier-free feed-forward carrier phase recovery without any feed-back pre-decision or feed-back pre-compensation is demonstrated.

The setup of 112 Gbit/s DP-QPSK back-to-back (B2B) system is shown in Fig.3. The laser phase noise is modeled as a Wiener process.  $2^{16}$  de Bruijn bit sequences are used for the bit to symbol mapping with differential coding. For X and Y polarizations, the de Bruijn bit sequences are de-correlated by 600 bits before the bit to symbol mapping. The arbitrary waveform generator (AWG) generates four 28 GSym/s electric driver signals with raised cosine pulse shaping with a roll-off factor of 1.

The in-phase and quadrature (I/Q) modulators are conducted for electric-optical conversion. Different amount of amplified spontaneous emission (ASE) noise is loaded to realize different optical signal-to-noise ratios (OSNRs). At the receiver side, a 4th order Gaussian optical filter with a 3 dB bandwidth of 50 GHz is used to filter out-of-band ASE noise. Along with the light from local oscillator (LO), the signal is fed into a 90° hybrid followed by 4 balanced photodiodes for coherent detection. For the intra-dyne coherent detection, the frequency offset between the transmitter and local oscillator lasers is set to 100 MHz.

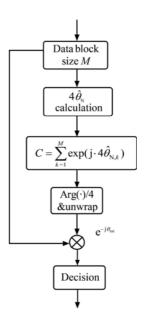
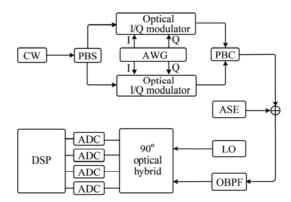


Fig.2 Principle of carrier phase recovery based on the proposed multiplier-free feed-forward CPE algorithm



AWG: arbitrary waveform generator; PBS: polarization beam splitter; PBC: polarization beam combiner; ASE: amplified spontaneous emission source; OBPF: optical band-pass filter; LO: local oscillator

## Fig.3 Simulation setup for a single-channel 112 Gbit/s back-to-back DP-QPSK system

The digital signal processing includes: (1) quadrature imbalance compensation<sup>[8]</sup>, (2) resampling to 2 samples per symbol, (3) digital timing recovery<sup>[9]</sup>, (4) adaptive equalizers with a butterfly configuration and the constant

modulus algorithm which are employed for polarization recovery and residual impairment compensation<sup>[10]</sup>, (5) carrier frequency recovery<sup>[11]</sup>, (6) carrier phase recovery, (7) symbol decision. The bit error is obtained by direct bit error counting.

Fig.4(a) shows the estimated phase noise for the proposed MF algorithm and the 4th power method with linewidth per laser of 2 MHz and OSNR of 14 dB. The inset shows the detail of the estimated phase noise by using two different algorithms. Results show that the proposed MF algorithm presents comparable performance with the well-known 4th power method. Fig.4(b) shows the constellation after frequency offset compensation, in which symbols rotate due to the residual frequency offset and the laser phase noise. By using the MF algorithm, a good carrier phase recovery for the 112 Gbit/s DP-QPSK signal is investigated as shown in Fig.4(c).

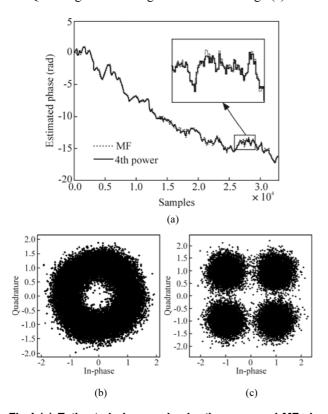


Fig.4 (a) Estimated phase noise by the proposed MF algorithm and 4th power algorithm; (b) Constellation after frequency offset compensation; (c) Constellation after carrier phase compensation by using the MF algorithm

Fig.5 shows the dependence of the BER on OSNR for 112 Gbit/s DP-QPSK B2B systems with different CPE algorithms. Results are presented for a linewidth per laser of 2 MHz. N is the block length of the corresponding CPE algorithm. Optimal block lengths are selected after a parameter sweeping to provide the best performance at OSNR of 14 dB. Results show that the proposed MF algorithm has the similar performance to the 4th power method. For BER of  $1 \times 10^{-3}$ , a required OSNR of 14.53 dB is investigated for the two CPE algorithms.

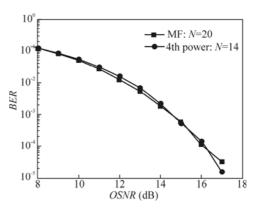


Fig.5 Dependence of BER on OSNR for different CPE algorithms in a 112 Gbit/s DP-QPSK B2B system

Similar to the 4th power method, the performance of the MF algorithm also suffers from the block length effect. The contour plot of the OSNR sensitivity penalty at BER of 10<sup>-3</sup> for the MF algorithm is shown in Fig.6 with respect to the combined laser linewidth (the sum of linewidths for lasers at transmitter and receiver) and block length. The reference is the OSNR at BER of 10<sup>-3</sup> for 0 Hz linewidth without CPE algorithm. The results illustrate that the larger the laser linewidth is, the smaller the optimum block length is. For a small laser linewidth, the laser phase noise varies slowly. The long block length is preferred to average the ASE noise, and exhibits better performance than the short block length. However, with the increase of laser linewidth, the optimum block length decreases due to the rapid variation of laser phase noise.

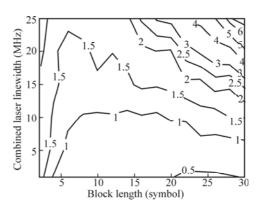


Fig.6 OSNR sensitivity penalties at BER of 10<sup>-3</sup> versus the combined laser linewidth and block length for the proposed MF algorithm

Fig.7 shows the simulation results for the OSNR sensitivity penalties at BER of  $10^{-3}$  for different CPE algorithms with different linewidth symbol duration products for a DP-QPSK signal. Each required OSNR is obtained by using the optimum parameters for each algorithm at each linewidth symbol duration product. As shown in Fig.7, the MF algorithm can tolerate a linewidth symbol duration product of  $2.9 \times 10^{-4}$  for 1 dB OSNR penalty at BER of  $10^{-3}$ , which is comparable with the 4th power method.

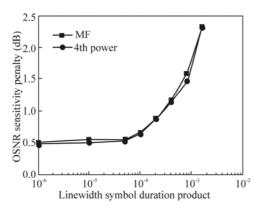


Fig.7 Simulated OSNR sensitivity penalty at BER of 10<sup>-3</sup> for a DP-QPSK signal versus linewidth symbol duration product for different CPE algorithms with optimum parameters

The hardware complexities for different CPE algorithms are shown in Tab.1. Assume M=512 and according to the parameter values used in Fig.5, N=16 for both the 4th power algorithm and MF algorithm, which is the closest to the optimal value when M/N is integer. Compared with the 4th power algorithm, zero multiplier is required for the MF algorithm. The number of LUT operations is increased. However, considering the zero multiplier requirement and large reduction in the required number of adders, the overall hardware complexity for the MF algorithm is still much lower than that of the 4th power algorithm.

Tab.1 Hardware complexities for different CPE algorithms

	Multiplier	Adder	Comparator	LUT
4th power	8M(4096)	6M-M/N(3104)	M(512)	M/N(32)
MF	0(0)	4M-M/N(2080)	M(512)	M+M/N(544)

In conclusion, a novel multiplier-free feed-forward CPE algorithm with low-complexity carrier phase recovery for DP-QPSK modulation format is proposed and verified by numerical simulation. The BER performance,

block length effect and linewidth tolerance of the proposed algorithm are evaluated for a 112 Gbit/s DP-QPSK system. A linewidth symbol duration product of  $2.9 \times 10^{-4}$  is demonstrated for 1 dB OSNR penalty at BER of  $10^{-3}$  for the proposed algorithm, which is comparable with the well-known 4th power algorithm but reduces the hardware complexity.

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