Trinary registers and counters using savart plate and spatial light modulator for optical computation in multivalued logic

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Registers and counters are the most important devices in any system of computations. In this paper we have communicated the trinary registers and counters in modified trinary number (MTN) system. It is suitable for the optical computing and other applications in multivalued logic system. Here the savart plate and spatial light modulator (SLM) based optoelectronic circuits have been used to exploit the optical tree architecture (OTA) in optical interconnection network.

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The carry and borrow-free mathematical operations are possible with modified trinary number (MTN) system[1-3]. The basic logic gates and the flip-flops are also reported[4-10] in MTN system using spatial light modulators (SLM) and savart plates. The flip-flops are the basic building block of sequential logic system. Any sequential logic system can be designed by using the flip-flops and the combinational logic units. One of the most important sequential circuits used in computing system is the register. A register consists of a group of flip-flops that can store information. Since a trinary flip-flop[10] can store 1 trit of information, a *n*-trit word register requires *n* number of flip-flops connected in cascaded, i.e. the output of one flip-flop is connected to the input of another.

In this paper we have communicated the implementation of trinary valued different shift registers and counters by using the clocked *D*-trinary flip-flops. The basic optical logic gates in MTN system have been used to implement the same. The basic clock pulse in trinary system is also used here. A mode control selector (MCS) is used to convert the *D*-trinary flip-flop into clocked *D*-trinary flip-flop. To implement the shift registers the MCS is used to implement the parallel and serial shift. The circuit implementations and the truth tables for the shift counter, ring counter and the ripple counters are discussed in details.

Before going into the details a short introduction to the basic logical system of trinary along with the process of implementation is given. The three states of the trinary representation are classified as the true, false and contradiction as shown in Tab.1. The truth states for the trinary logic gates required to implement the trinary flip-flops, registers and counters are mentioned in Tab.2. The basic logic gates and their output functions have been defined earlier[5]. The required gates as mentioned may be implemented[5] by using the basic building block discussed hereunder.

Tab.1 Trinary logic system

Logical state	Representation	Dibitrepres.	State of Polarization
True /	1	01	Vertical
Complete false /	$\bar{1}$	10	Horizontal
Wrong contradiction/ Partial	0	11	Both the horizontal and vertical
Don′t care state		00	–

For the implementation of the logical operations as mentioned we have used a basic building block given in Fig.1. A light from a laser source *L* through a polarizer *P* is incident on the first savart plate S_1. The basic property of a savart plate is that if a light polarized at a direction of 45^0 with the vertical axis as shown in the Fig.1, is incident on it, the output will be two parallel beams shifted between themselves. The state of polarization of the output beams is orthogonal to each other as shown. The output beams may be controlled (the presence or absence) by using two input signals through spatial light modulators (SLMs) P_1 and P_2. The SLMs are of two types- positive and negative. The nature of the negative

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SLM is such that it is transparent when there is no electric voltage applied on it and it becomes opaque when an electric voltage is applied on it. The property of positive SLM is just reverse. In the output two beams are combined by using a second savart plate S_2 for which the crystal axes are opposite that of first savart plate S_1. Different logic gates mentioned in Tab.2 may be implemented by combining this very basic module.

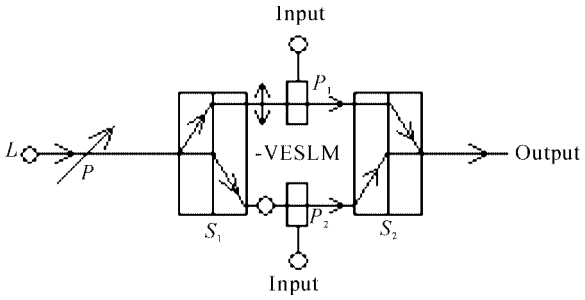

Fig.1 The basic building block.

Tab.2 Truth states for OR,AND,XOR,NOR,NAND,XNOR, Complement, true Selector, false Selector, exclusive true selector and exclusive false selector gates.

A	1	1	1	0	0	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	Operation
B	1	0	$\bar{1}$	1	0	$\bar{1}$	1	0	$\bar{1}$	
A∨B	1	1	0	1	0	$\bar{1}$	0	$\bar{1}$	$\bar{1}$	A OR B
A∧B	1	0	0	0	0	0	0	0	$\bar{1}$	A AND B
A⊕B	0	1	0	1	0	$\bar{1}$	0	$\bar{1}$	0	A XOR B
$\overline{A \vee B}$	$\bar{1}$	$\bar{1}$	0	$\bar{1}$	0	1	0	1	1	A NOR B
$\overline{A \wedge B}$	$\bar{1}$	0	0	0	0	0	0	0	1	A NAND B
$\overline{A \oplus B}$	0	$\bar{1}$	0	$\bar{1}$	0	1	0	1	0	A XNOR B
$\bar{A}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1	Complement
A↑	1	1	1	1	1	1	0	0	0	True selector
A↓	0	0	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	False selector
A↓	1	1	1	0	0	0	0	0	0	0 Exclusive true selector
A↑	0	0	0	0	0	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$ Exclusive false selector

Sequential circuits are commonly synchronized with a train of pulses, called clock pulses. Such a series of clock pulses are shown in Fig.2. Here, 1 represents the high state of this clock pulses, 0 represents the state between 1 and $\bar{1}$, and the low stere is represented by $\bar{1}$.

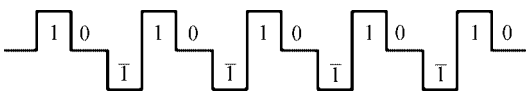

Fig.2 A series of clock pulses

Circuit diagram of mode control selector network is shown in Fig.3. The MCS network acts as a digital filter. When the mode control is 1, the data can pass through it; but when the mode control is 0 or $\bar{1}$, it stops the data to pass. The function of the circuit is described in Tab.3.

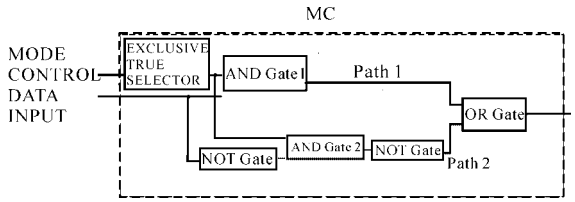

Fig.3 Logic diagram of mode control (MC) selector network

Tab.3 JK Trinary flip-flop

J	K	Q_A	Q_B	Q_C
1	1	1	1	1
1	0	1	$\bar{1}$	0
1	$\bar{1}$	1	0	$\bar{1}$
0	1	0	$\bar{1}$	1
0	0	0	0	0
0	$\bar{1}$	0	1	$\bar{1}$
$\bar{1}$	1	$\bar{1}$	0	1
$\bar{1}$	0	$\bar{1}$	1	0
$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$

The truth table of *D*-trinary flip-flop is shown in Tab.4 and the block diagram of a clocked *D* flip-flop is shown in Fig.4. Here the clock pulses are applied through the mode control selector (MCS) networks prior to the inputs of *D*-trinary flip-flop.

Tab.4 *D*-Trinary flip-flop

D	Q_A	Q_B	Q_C
1	1	0	$\bar{1}$
0	0	0	0
$\bar{1}$	$\bar{1}$	0	1

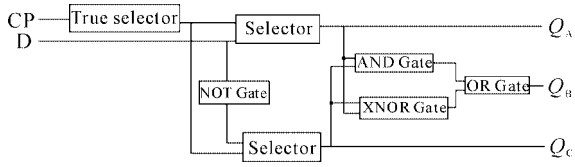

Fig.4 Clocked *D*- trinary flip flop.

Case-I: When mode control (M) = 1, the output of the exclusive true selector = 1.

Case-II: When mode control = 0 or $\bar{1}$, then after passing through the exclusive true selector it becomes 0 and as a result, one of the two inputs of the two AND gates 1 and 2 is always 0. So the outputs of both the AND gates 1 and 2 are always 0. As a result, the output of OR gate is always 0 and is independent of the data input D.

So with this combination, the operations of *D* flip-flop remain the same when *CLK* = 1, but when *CLK* = 0 or $\bar{1}$, it stops its operation.

The trinary information of a register can be shifted either to the right or to the left. Depending upon the mode of operation a shift register can be classified into four types: serial in serial out; serial in parallel out; parallel in serial oul; and parallel in parallel out.

To design this universal trinary shift register we have used 4-*D* trinary flip-flops, 1 NOT gate, 4 OR gates and 8 mode control selector (MCS) networks. The circuit and the trinary flip-flop are shown in Fig.5 and Tab.5, respectively.

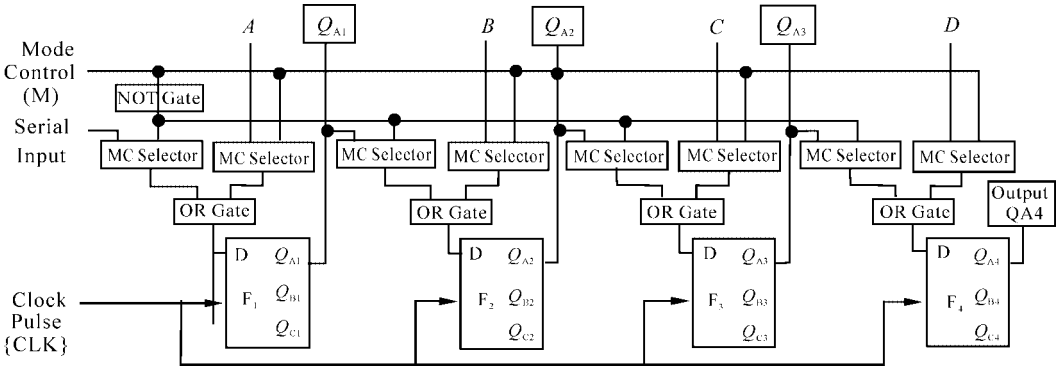

Fig.5 4-trit universal trinary shift register

Tab.5 *T*-trinary flip-flop

T	Q_A	Q_B	Q_C
1	1	1	1
0	0	0	0
$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$

The logic diagram and the truth trinary counter are shown in Fig.6 and Tab.6, respectively.

Tab.6 Truth trinary shift counter

CLK	Q_{A1}	Q_{A2}	Q_{A3}
0	$\bar{1}$	$\bar{1}$	$\bar{1}$
↑	1	$\bar{1}$	$\bar{1}$
↑	1	1	$\bar{1}$
↑	1	1	1
↑	$\bar{1}$	1	1
↑	$\bar{1}$	$\bar{1}$	1
↑	$\bar{1}$	$\bar{1}$	$\bar{1}$

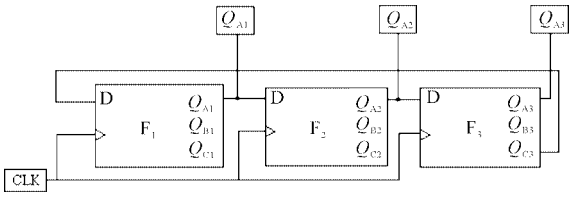

Fig.6 Block diagram of trinary shift counter

In every clock pulse, the data will be shifted towards the next flip-flop and it will be continued as shown in Tab.7. As a result, we will get a ring counter suitable for the different applications. The logic diagram is shown in Fig.7.

Tab.7 Truth table for trinary ring counter

CLK	Q_{A1}	Q_{A2}	Q_{A3}	Q_{A4}
↑	$\bar{1}$	0	0	0
↑	0	$\bar{1}$	0	0
↑	0	0	$\bar{1}$	0
↑	0	0	0	$\bar{1}$
↑	$\bar{1}$	0	0	0

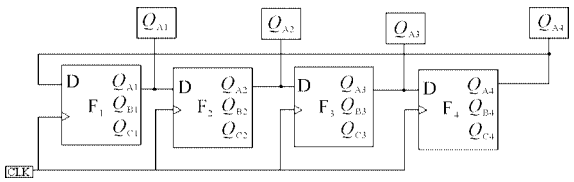

Fig.7 Block diagram of trinary ring counter

Using *D*-trinary flip-flops we have constructed the trinary ripple counter as shown in Fig.8. Here the input (*D*) of the first flip-flop F_1 is taken from its output Q_{A1} through the combinational circuit, consisting of exclusive false selector, exclusive true selector, true selector, false selector, NOT gate,

AND gate and OR gate. The clock pulse (CLK) is connected directly to the flip-flop F_1. The changing states of Q_{A2} in the next clock pulse for the combinations of Q_{A1} and Q_{A2} are obvious from the Tab.8.

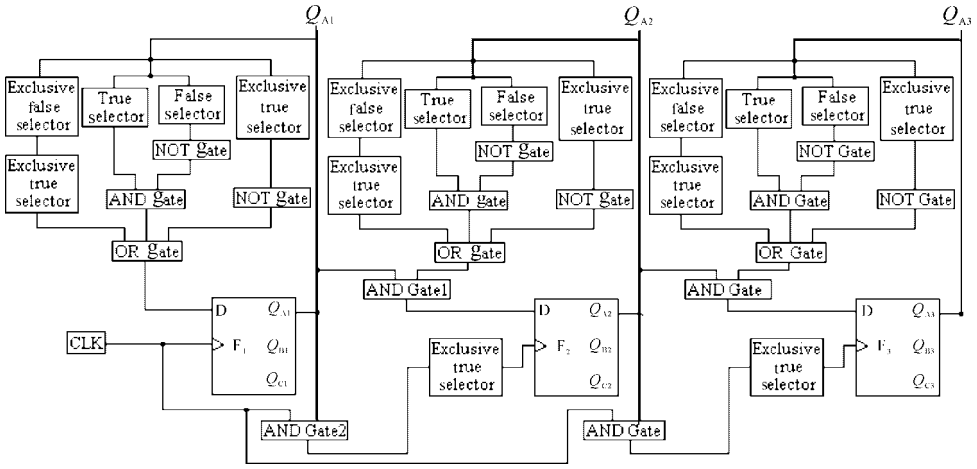

Fig.8 Block diagram of trinary ripple counter

Tab.8 Truth Table for trinary ripple counter

State	Output			State	Output		
	Q_{A3}	Q_{A2}	Q_{A1}		Q_{A3}	Q_{A2}	Q_{A1}
1	$\bar{1}$	$\bar{1}$	$\bar{1}$	15	0	0	1
2	$\bar{1}$	$\bar{1}$	0	16	0	1	$\bar{1}$
3	$\bar{1}$	$\bar{1}$	$\bar{1}$	17	0	1	0
4	$\bar{1}$	0	$\bar{1}$	18	0	1	1
5	$\bar{1}$	0	0	19	1	$\bar{1}$	$\bar{1}$
6	$\bar{1}$	0	1	20	1	$\bar{1}$	0
•	•	•	•	21	1	$\bar{1}$	1
•	•	•	•	22	1	0	$\bar{1}$
•	•	•	•	23	1	0	0
10	0	$\bar{1}$	$\bar{1}$	24	1	0	1
11	0	$\bar{1}$	0	25	1	1	$\bar{1}$
12	0	$\bar{1}$	1	26	1	1	0
13	0	0	$\bar{1}$	27	1	1	1
14	0	0	0				

In conclusion, in this paper we have communicated the different sequential trinary logic circuits, such as different registers and counters using clocked *D*-trinary flip-flops suitable for the optical computations and other applications. The clocked *D*-trinary flip-flop and their practical implementations by using the opto-electronic devices are also suitable for the fast operations. Due to the signed digit implementations, the mathematical operations are also very simple. This trinary logic finds its applications in gray image processing, cellular automata, fuzzy logic systems, fractals and other emerging areas where fast operations are needed.

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