40-to-10-Gb/s demultiplexing using an electro-absorption sampling window*

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The demultiplexing experiment from a 40 Gb/s optical time-division multiplexing signal is completed by using electro-absorption sampling window based on electronic phase-locked loop circuit for clock recovery. Error-free demultiplexing is achieved when the launched optical power into electro-absorption sampling window reaches 5.5 dBm without optical filter following the EDFA.

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Optical demultiplexers, which extract a signal channel at the base rate of a time-multiplexed high-bit-rate data stream, become an important functionality in optical time-division-multiplexed (OTDM) networks. Optical demultiplexers with ultra-short switching gates can be realized by utilizing fiber nonlinearities and semiconductor devices[1-3]. Fiber-based optical switches can provide an ultra-broad conversion band and ultra-high-speed operation but at the expense of high optical powers and performance instability. Electro-absorption sampling window (EASW)-based demultiplexing techniques are particularly attractive because they feature small size, high stability, lowing switching energy, and high integration potential[4,5].

In this letter, the demultiplexing of 10 Gb/s base-rate channels out of 40 Gb/s OTDM data stream is completed using EASW based on optoelectronic phase-locked loop (PLL) circuit for clock recovery. This is the basis of further higher bit rate demultiplexing in OTDM system in the future.

The experimental setup as shown in Fig.1 consists of an OTDM transmitter and an OTDM receiver in a back-to-back configuration. The setup is constructed with commercially available components. An actively mode-locked fiber ring laser generates pulses at a 1550.17 nm wavelength with 10 GHz repetition rate. 10 Gb/s PRBS 2^{23}-1 data generated by bit error rate (BER) is encoded onto the MLFL output using an external modulator. A passive optical multiplexer is used to generate a 40 Gb/s data stream. The receiver comprises the demultiplexer and 10 Gb/s clock recovery unit. Our demultiplexer is made out of an EASW and its driving circuit includes Bias T and microwave amplifier. The 10 GHz clock signal is recovered with an optoelectronic hybrid phase-locked loop (H-PLL) [6,7].

The incoming 40 Gb/s signal is optically demultiplexed to 10 Gb/s by the EASW driven by a 10-GHz clock. Then the 10 Gb/s is sent to a coupler with 75:25, where 25% optical signal is sent to an oscilloscope (Agilent DCA 86100 B) in order to monitor the demultiplexed signal, and 75% optical signal is sent to H-PLL. Strictly speaking, four EASWs are required for a 1:4 demultiplexing as well as the multiplexer. Also, in this case, the authentic demultiplexing module will be realized by employing the free-space structure similar to the optical multiplexer.

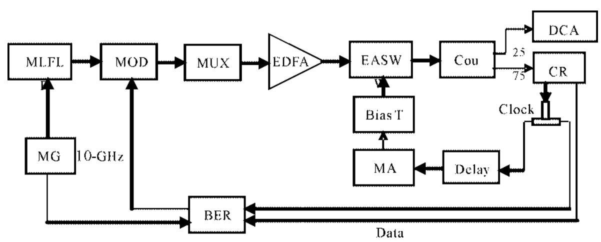

Fig.1 Experimental setup. MLFL: mode-locked fiber ring laser. MG: microwave generator. MOD: $LiNbO_3$ modulator. MUX: passive 10-to-40-Gb/s multiplexer. Cou: coupler. MA: microwave amplifier. CR: clock recovery unit. Delay: variable electrical delay.

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The EASW is a high-speed, semiconductor device capable of generating <25 ps (FWHM) temporal optical sampling windows with a repetition rate up to 10 GHz. Fig.2 shows the trace of sampling window in the experiment. The MLFL produces an optical pulse train at repetition rates 10 Gb/s, and its eye diagram is shown in Fig.3 (a). Fig.3 (b) shows the eye diagram modulated. The lob of the trace is caused by reflection of the ends of fiber connection. If the ends are all APC or UPC, it will be very small or canceled.

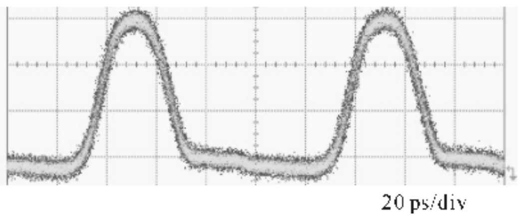

Fig.2 Optical sampling traces of EASW

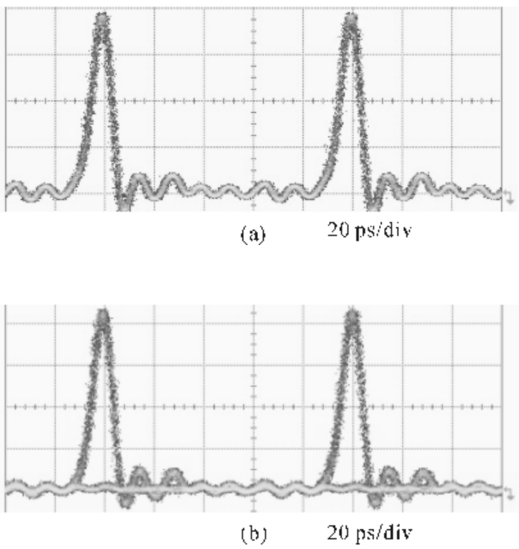

Fig.3 Eye diagram of 10 Gb/s. (a) pulse source, (b) modulating pulse

The eye diagram of multiplexed 40 Gb/s signal is shown in Fig.4. The multiplexer is made up of optical variable delay, and one of branches is direct, and the other three are indirect. So we can see the amplitude of one branch is higher than that of the other three. Besides, the noise of the eye diagram is large, because we don't use the filter following the EDFA. But this has little influence on the sequential experiment for it is only 40 Gb/s. If it is 80 Gb/s or higher bit rate, the filter is necessary. Then the signal is sent to the demultiplexer. At first, we can't gain the clear demultiplexed signal as shown in Fig.5(a). By adjusting the electrical variable delay and the bias voltage of the EASW carefully, we obtain the good eye diagram of the demultiplexed signal at last, as shown in Fig. 5(b). At the moment, the error is free, so one branch is demultipl- exed successfully. Then we can obtain the demultiplexed signal of the other three branches by adjusting the variable electrical delay.

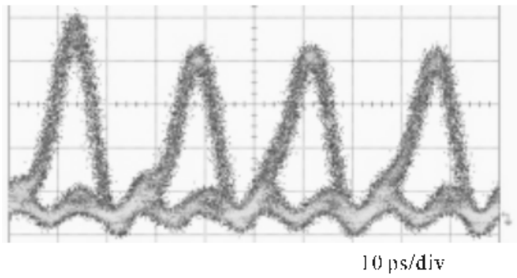

Fig.4 Eye diagram of multiplexing 40 Gb/s

Comparing Fig.3 (b) with Fig.5 (b), it is evident that there is almost no difference except Fig.5 (b) has larger jitter than that of Fig.3 (b). We think this phenomenon is caused by the ASE of EDFA for we don't have a filter. In this case, the error-free is achieved when the launched optical power into EASW reaches to 5.5 dBm. In the following demultiplexing experiment of 80-Gb/s or 160-Gb/s, the filter should be used. Therefore we are trying to make a filter for higher bit rate.

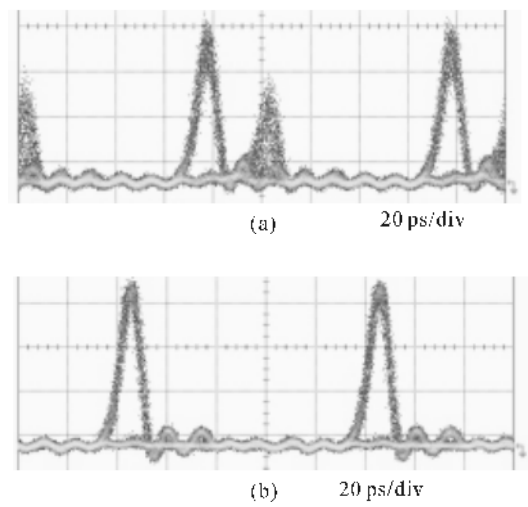

Fig.5 Eye diagram of demultiplexing 10 Gb/s.(a) bad, (b) good .

In conclusion, the successful 40-to-10 Gb/s demultilexing using an EASW based on H-PLL for clock recovery is described and demonstrated. Error-free is completed without filter following EDFA when the launched optical power into EASW reaches 5.5 dBm. In the following experiment, we'll set about the demultilplexing of 80-to-10 Gb/s and 160-to-10 Gb/s.

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