Design and implement of LED drive circuit chip with the controllable constant output current*

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Owing to the fact that the LED drive circuit must have constant output current control, we propose a controlled current driver with a high precision for the white light LED. Three discrete constant current settings are available and may be selected at the supply voltage from 2.9 V to 4.4 V, which is up to 1 A. An autozero transconductance amplifier is proposed, which effectively improves the precision, reduces the offset voltage and the noise. The variation in the ratio of the external resistor current to the LED load current is less than 2.3%, when the LED load current changes from 200 mA to 800 mA.

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In order to lower the influence on the precision of output current, an autozero technique is applied to remove the offset of the amplifier and improve the precision of the output current[1].A serial connection is superior to a parallel connection, because a constant current can be simply supplied to each LED that belongs to an array. However, the total voltage and total current of a serial connection vary, depending on the occurrence of short circuit LED breakdowns. Consequently,the LED drive circuit must have constant output current control and/or constant-luminance control.

In this paper we use an external resistor to control the output driving current, which has a wide range, and the maximum of 1 A. The circuit structure is shown in Fig.1, which consists of the band-gap reference voltage source, the programmable control current circuit and the current source control output circuit. The programmable control current circuit is composed of external resistors R_{SET1} and R_{SET2}, which is controlled by enable signals *EN*1 and *EN*2. In the different enable case, the different reference voltages of V_{REF1} can be obtained by changing the value of external resistors R_{SET1} and R_{SET2}. The current source control circuit consists of 8 identical modules connected in parallel.

In Fig.1, R_{S} is the sampling resistance, and I_{LED} is the drive current of LEDs and is represented as,

$$V_{\mathrm{REF1}} = K \cdot V_{\mathrm{REF}} \ , \tag{1}$$

$$I_{\mathrm{LED}} = 8 \cdot \frac{V_{\mathrm{REF1}}}{R_{\mathrm{S}}}. \tag{2}$$

From eq.(1) and eq.(2), it can be seen that I_{LED} is dependent on the gain K, the reference voltage V_{REF} and R_{S}. But the gain K is associated with the external resistors. Therefore, if V_{REF} is given, the output current is controlled by the external resistor.

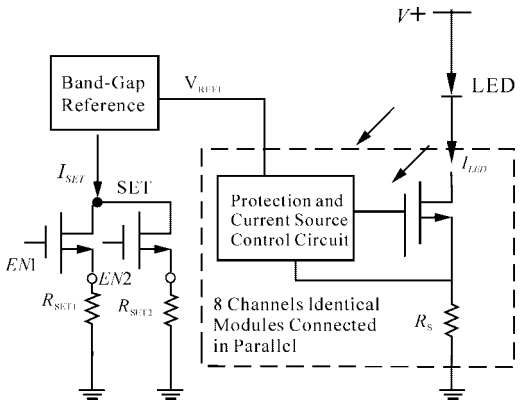

Fig.1 Schematic diagram of constant current driver

Fig.2 shows the complete circuit schematics in the design. The current source control circuit and the complete band-gap reference consist of four circuit blocks: the bias circuit,

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the startup circuit, the core reference and the controlled reference.There are two state equilibrium points in the bias circuit. One is a designed operating point that we need (which can be referred to as a non-zero state equilibrium point), that is to say, current mirrors formed by *M*1-*M*4 that enforce branch currents equal to a proportional-to-absolute-temperature(PTAT)I, which is generated by *Q*1,*Q*2 and *R*1. The emitter area of *Q*1 is eight times of *Q*1 in the bias circuit. So *M*1-*M*4 respectively has the same current that is shown in the eq.(3).The bias current of the other circuits can be supplied by I_1 mirroring.

$$I_{1\text{-}4} = \frac{k \ln 8}{qR_1} T \quad . \tag{3}$$

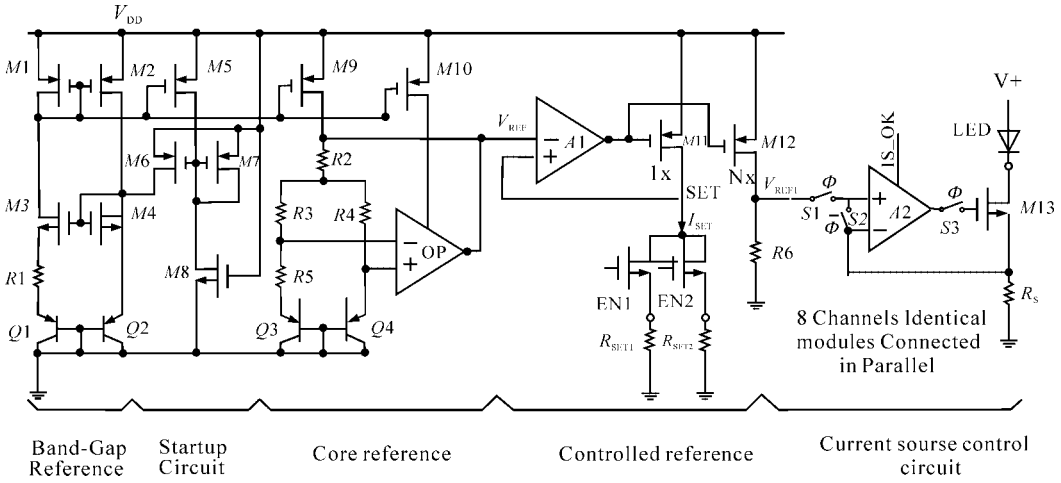

Fig.2 Schematic of the band-gap reference and the controlled current

Another state equilibrium point of the bias circuit is the state that *M*1-*M*4 is turned off (which can be referred to as a zero state equilibrium point) and I_1-I_4 is zero. A startup circuit is required to make sure that enough current flows to force operation at the designed operating point.

The startup circuit used in the design is constituted by *M*5-*M*8. When the supply is turned on and the gate of *M*8 is pulled high and the drain of *M*8 is pulled low, consequently the gates of *M*6-*M*7 are pulled low which inject current to the bias circuit. Once the currents flow through the bias circuit, the drain of *M*4 becomes high and this pulls the gates of *M*3-*M*4 high which pulls the gate of *M*5 down, as a consequence, the gates of *M*6-*M*7 are pulled high leaving this transistor in cut off and eventually making the startup circuit idle.

The reference core circuit consists of *R*3-*R*5, *Q*3-*Q*4 and the operation amplifier. The operation amplifier enforces the invert and non-invert ports to have the same potential, and due to *R*3 = *R*4, currents flowing through *R*3 and *R*4 are equal as consequence currents flowing through *Q*3 and *Q*4 are equal. Considering that the ratio emitter area of *Q*3 and *Q*4 is 8:1, the output voltage of the reference can be expressed as follows,

$$V_{\text{REF}} = V_{BE4} + \frac{2R_2 + R_4}{R5} \frac{k \ln 8}{q} T \,, \tag{4}$$

The controlled reference circuit consists of *R*6, *M*11-*M*12 and the operation amplifier *A*1. The voltage follower formed by *A*1 and *M*11 enforces the voltage of node SET following the output voltage of the reference. The gain of the current mirror formed by *M*11 and *M*12 is *N*, which amplifies the current of I_{SET}. The output voltage of the controlled reference is controlled by external resistors and the enabling port (*EN*1 and *EN*2).

$$V_{\text{REF1}} = N \cdot \frac{V_{\text{REF}}}{R_{\text{SETX}}} \cdot R_6 \quad . \tag{5}$$

The current source control circuit is formed by an operation amplifier *A*2, *M*13 and the sampling resistance R_S. When the output driving current is under the value V_{REF1}/R_S, the drop voltage of R_S is smaller than the voltage of V_{REF1}, and therefore, the output of the operation amplifier is pulled high which increases the output current. In the balance state, the drop voltage of R_S can be clamped to the value of V_{REF1}. In order to enhance the driving capability, there are 8 identical current source control circuits in parallel to drive the LEDs. Considering the offset voltage of the operation amplifier, the eq.(2) is modified, and we get the eq.(6),

$$I_{\text{LED}} = 8 \cdot \frac{V_{\text{REF1}} + V_{\text{OS}}}{R_S} \quad . \tag{6}$$

The eq.(6) tells us that the offset voltage of the operation

amplifier has great influence on the precision of the output current, so an autozero technique is applied to reduce the offset voltage of the operation amplifier.

The basic schematic of the autozero technique (AZT) operation amplifier[5,6] is shown in Fig.3, which includes the base amplifier G_{m1}, the compensating amplifier G_{m2}, the second stage amplifier A_4, the feedback amplifier A_3, the holdcapacitor C_h and two switches S_1 and S_2. R_o is the output impedance of G_{m1} and G_{m2}.

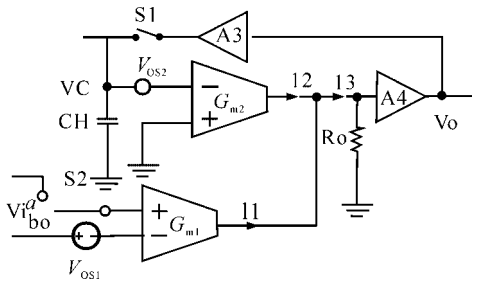

Fig.3 AZT amplifier principle schematic

1) During the sampling phase, the S_2 switch is connected with the point b, so that it connects the G_{m1} stage inputs together, so G_{m1} has only its own offset voltage applied at the input. As a result, it generates an output offset current,

$$I_1 = G_{m1} \cdot V_{os1} \quad . \tag{7}$$

The S_1 switch is also on and A_3 amplifier feedbacks the output voltage to the G_{m2} inverting input. G_{m2} outputs current, I_2 is given by

$$I_2 = -G_{m2} \cdot (A_3 V_o - V_{os2}) \quad , \tag{8}$$

$$V_o = R_o (I_1 + I_2) A_4 \quad , \tag{9}$$

where V_{os2} is the input offset voltage of G_{m2}, and V_o is output voltage. This current tries to compensate the base amplifier offset current, so it has an opposite direction and is proportional to the output offset voltage.

With eqs. (7) and (8) , we can get the offset voltage V_C

$$V_C = A_3 V_o = A_3 A_4 \frac{G_{m1} R_o V_{os1} + G_{m2} R_o V_{os2}}{1 + A_4 A_3 R_o G_{m2}} \quad . \tag{10}$$

2) During the signal processing phase, the S_2 switch is connected with the point a, and it causes that the base amplifier G_{m1} is connected to the signal path. The feedback loop is disconnected (S_1 is off). At this time, V_C is stored in C_h. Because the switches are implemented by MOS transistors in CMOS circuit, the AZT operation analysis must include the charge injection effects that take place during the transition among phases[7].

When the switch S_1 is turned off, the part of the channel charge is injected in the V_C node, changing the voltage stored on C_h. The variation of the voltage is,

$$\Delta V_c = q_{inj} / C_h \quad . \tag{11}$$

The total output voltage is,

$$V_o = G_{m1} R_o A_4 V_i + A_4 \frac{G_{m1} R_o V_{os1}}{1 + G_{m2} R_o A_3 A_4} + \\ + A_4 \frac{G_{m2} R_o V_{os2}}{1 + G_{m2} R_o A_3 A_4} - A_4 G_{m2} R_o \frac{q_{inj}}{C_h} \quad , \tag{12}$$

where V_i is the input signal, and the residual offset voltage V_{OSres} is an output voltage for a zero differential input, divided by the differential voltage gain.

$$V_{OSres} = \frac{V_o \mid_{Vi=0}}{G_{m1} R_o A_4} = \\ \frac{V_{OS1}}{G_{m2} R_o A_3 A_4} + \frac{V_{OS2}}{G_{m1} R_o A_3 A_4} - \frac{G_{m2}}{G_{m1}} \frac{q_{inj}}{C_h} \quad . \tag{13}$$

From the equation (13), we can know that the offset voltage of G_{m1} is divided to the $G_{m1} R_o A_3 A_4$ ratio, and the offset voltage of G_{m2} is reduced by $G_{m2} R_o A_3 A_4$ ratio.

The AZT amplifier complete schematic is presented in Fig.4. There are five switches in the circuit. During the sampling phase, S_2, S_3 and S_4 are short connected, and S_1 and S_5 are turned off. The two transconductance stages, G_{m1} and G_{m2} are respectively composed of two differential pairs.G_{m1} is implemented by *MP*1 and *MP*2. G_{m2} consists of the fold-cascode parts *MP*3, *MP*4 and *MN*3, *MN*4. Amplified by three stages, the offset voltage is stored in C_{h1} by the follower MN9.

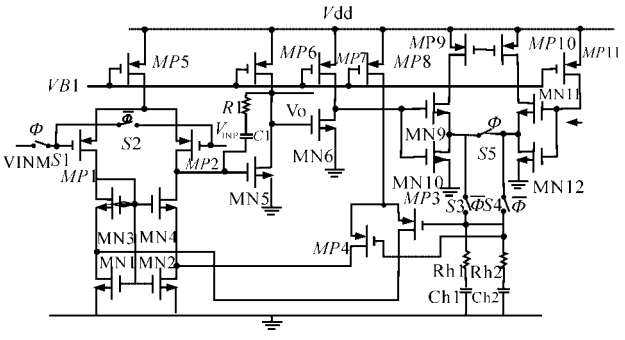

Fig.4 AZT amplifier implementation

During the signal processing phase, S_2, S_3 and S_4 are turned off, but S_1 and S_5 are short connected, so it makes the offset voltage subtracted from the input signal. The bias circuit is composed of *MP*5-*MP*16. *VB*1 and *VB*2 are external bias signals. R_1 and C_1 form the miller compensation circuit.

Based on the Hynix 0.6 μm CMOS process , the circuit is

simulated using Hspice. Fig.5 shows the temperature response of the corners when the supply voltage is 3 V. We observe that the output variation of the band-gap reference in the temperature range from -40 °C to 85 °C is 1 mV, and the difference is smaller than 15 mV at all three process corners.

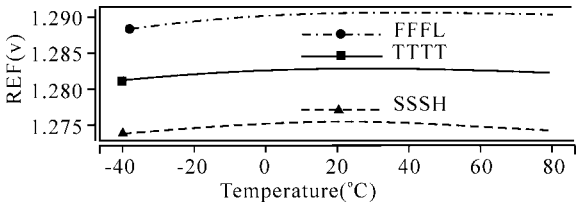

Fig.5 The reference voltage under three process corners

The twenty-five samples measurement results of the output current I_{LED} and I_{LED}/I_{SET} are shown in Fig.6. The value of I_{LED}/I_{SET} is between 3314 to 3165. The current precision is 2.3%.

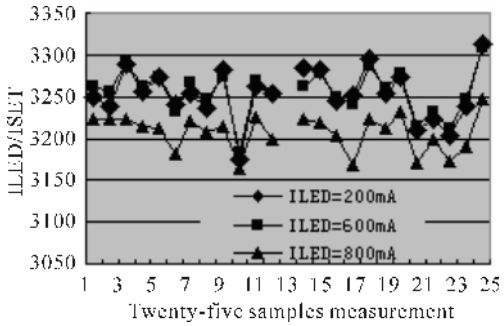

Fig.6 The measurement result of the output current I_{LED} and I_{LED} / I_{SET}

Tab.1 shows the electrical characteristics of the chip with the constant current driving circuit. We observe that the leakage voltage of I_{LED} will increase with the increase of the driving current, and the leakage voltage is 115 mV when the driving current is 200 mA.The overcurrent detection current I_{SET} should not exceed 330 μA. When it is above 330 μA, the overcurrent protection will make the driving output current zero.

Tab.1 Electrical characteristics of the chip with constant current driver

V_{IN}=3.6 V, T_A = 25 °C	(LED is externally connected with 5V)			
Parameter	Test conditions	Min	Typ.	Max.
Current Ratio(I_{LED}/I_{SET})	I_{LED} = 200 mA to 800 mA	3165	3243	3314
I_{LED} dropout voltage (mV)	I_{LED} =200 mA		115	
I_{SET} overcurrent current (μA)				330
Overtemperature protection (°C)		140		160

In summay, this paper refers a high precision constant current driving circuit that can be applied in LED charge-pump DC-DC chip. With an autozero technique, the internal circuit can reduce the offset voltage of the operation amplifier and improve the precision of the output current greatly. By regulating the value of the external resistors, different constant driving current can be provided, which is up to 1A. When the driving current varies from 200 mA to 800 mA, the variation of I_{LED}/I_{SET} is less than 2.3%. This circuit also can be applied to drive large LED array.

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