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Nanoscale Barrier Layers to Enable the Use of Gallium-Based Thermal Interface Materials with Aluminum

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Performance of thermal interface materials (TIMs), such as thermal pastes and mats, hinders the advance of integrated circuit (IC) devices. Current state-of-the-art TIMs suffer from low thermal conductivity, thick cross sections, and poor long-term performance. Gallium (Ga) and gallium-based alloys and amalgamations, in liquid and solid form, have demonstrated up to three times greater thermal conductivity than conventional TIMs, but rapidly alloy with and destroy aluminum (Al) components, which are commonly found in IC devices. In this work, we investigate the use of thin-film barrier layers on Al to prevent Ga alloying and characterize their performance through accelerated Ga exposure experiments and scanning electron microscopy. It is found that 100-nm-thick layers of the common passivation materials niobium and 304 stainless steel do not sufficiently prohibit Ga migration, but a 100 nm layer of titanium (Ti) does. No alloying is evident in Ti-coated Al samples after exposure to a liquid Ga alloy droplet at 300 °C for 168 h, 250 thermal cycles from room temperature to 150 °C with 30-min dwell, or 50 thermal cycles from room temperature to 300 °C with 2-min dwell. The results present a clear and direct path to the use of Ga and Ga alloys as TIMs through the addition of a thin inexpensive barrier layer on Al components and may enable future IC device technologies.

Keywords barrier layer, liquid metal, physical vapor deposition, thermal interface material, thermal management

1. Introduction

As IC devices continue to push toward smaller sizes, higher speeds, and greater power density, demands on thermal management are ever-increasing (Ref 1, 2). TIMs play a key role in thermal management of IC devices through moving heat from the heat generating component to heat mitigation components like spreaders and heat transfer devices such as heat exchangers (Ref 1, 2). Often, the heat mitigation components are made of Al due to its low cost, high thermal conductivity, ease of manufacturing, and corrosion resistance (Ref 3). The most prevalent TIMs are composed of metallic or carbon-based micro- or nanoparticles in an organic binder (Ref 2). Although advantageous due to ease of handling and low cost, these materials are not ideal due to their relatively low thermal conductivity, thick bond cross sections, short service life and low maximum operating temperatures (Ref 2, 4).

The overall performance of TIMs on the device scale is composed primarily of thermal performance and lifetime (Ref 1, 2). Important thermal performance parameters are thermal conductivity, thermal resistance due to bond width, and maximum operating temperature (Ref 2). Leading TIMs have a thermal conductivity approaching ~ 10 W/m-K, compared to ~ 200 W/m-K for the adjacent Al-based components (Ref 1). Available TIMs have thick bonds on the order of hundreds of microns to one millimeter (Ref 1). The coupling of the thick bond line and the low thermal conductivity creates a high thermal resistance between the heat-producing IC device and the thermal management device (Ref 1). Further, due to their organic constituents, leading thermal pastes can only operate at a short duration peak temperature of 180 °C, and for extended times at 130 °C (Ref 1, 5). Even if the high thermal resistance is allowable, next-generation semiconductor devices operate at temperatures exceeding the maximum temperature of thermal paste (Ref 6). Improvement in TIMs is vital to further advances in minimization and power density of ICs. At a minimum, removal of the organic constituent from TIMs is necessary to enable higher power density and temperatures.

Abbreviations	
TIMs	Thermal interface materials
IC	Integrated circuit
Ga	Gallium
Al	Aluminum
Ti	Titanium
Nb	Niobium
PVD	Physical vapor deposition
304SS	304 stainless steel
SEM	Scanning electron microscopy
EDS	Energy-dispersive spectroscopy
CPU	Central processing unit

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Investigation into metal-based TIMs has developed over the last decade, and several solutions are present in the literature and commercially (Ref 7, 8). In the most ideal embodiment, pure metallic nanostructures, primarily of gold, silver, or copper, are used in a thermocompression bonding configuration (Ref 7, 9, 10). Thermal performance of these nanostructures is excellent, owing to pure metal constituents and bond lines on the order of microns. However, the path to device-level application of metallic nanostructures remains unclear. Metallic nanostructure TIMs require high application pressures, often $>$ 50 MPa, and bonded components to have nanometer scale smoothness (Ref 11). Unfortunately, few IC components can withstand high pressures without mechanical damage (Ref 12). Device-level thermal management components often have intrinsic micron scale or greater surface roughness from their fabrication techniques, and improvements in polishing are prohibitively expensive (Ref 3). Ga-based materials have come to the forefront of investigation due to the ease of application and desirable thermal properties. Ga-based materials are easy to apply in paste or liquid form due to their low melting temperatures (Ref 7, 13). Thermal conductivity of Ga-based materials at 39 W/m-K is roughly three times greater than the best organic-based thermal pastes (Ref 14, 15). Ga and its alloys have been investigated as TIMs in liquid state and solid state in the form of amalgamations (Ref 16). Unlike thermal paste, Ga and Ga-based metallic mixtures have significantly increased operating temperatures and will not break-down over time, unlike organic TIMs (Ref 1, 17). The main hindrance to the use of Ga-based TIMs is incompatibility of Ga with materials used in heat mitigation components. Ga rapidly alloys and destroyed Al heat mitigation components by migrating along grain boundaries and causing rapid exfoliation corrosion (Ref 18, 19).

To enable the use of Ga-based TIMs with Al devices, a thermally conductive barrier to migration of Ga is necessary. The ideal interface film must be mechanically and chemically stable under thermal cycling, minimize impact on device-level thermal conductivity, and be cost effective. Logical solutions are anodization of the native Al, or additive metal or ceramic layers deposited through physical vapor deposition (PVD). Despite the low cost and ease of fabrication, anodizing is not an ideal solution. The layer of anodic oxide formed on the bulk Al is generally $\sim$ 10 to $\sim$ 100 microns thick and highly porous (Ref 20). The combination of the thickness of the layer and the relative portion that is occupied by air create poor thermal properties. PVD is used extensively in the manufacture of ICs, facilitating adoption of PVD barrier layers. Metal and metal oxide films grown using PVD have been successfully used as diffusion barrier layers in IC devices for several decades, at thicknesses of $\sim$ 10 to $\sim$ 100 nm (Ref 21). The ideal material must exhibit immiscibility with Ga at all operating temperatures, as well as tolerance to thermal cycling and the potentially large mismatch of thermal expansion with the bulk Al.

In this work, we investigate the ability of several prototypical thin-film barrier layers on bulk Al to prevent the migration and alloying of a commercially available Ga-based alloy, Galinstan. The refractory metals niobium (Nb) and Ti are investigated, as well as 304 stainless steel (304SS). These thin films are subjected to high-temperature Galinstan exposure as well as extended thermal cycling and characterized using scanning electron microscopy (SEM) and energy-dispersive spectroscopy (EDS). It is found that Nb and 304SS do not provide a sufficient barrier, allowing Ga penetration into the underlying bulk Al. The Ti layer provides sufficient protection to the Al and prevents alloying under all of the experimental conditions.

2. Methods

Candidates for the barrier layer and Ga-based TIM are selected for their availability and ease of industrial adoption. Ti and Nb have been used in IC devices as barrier layers for over two decades and have demonstrated performance in preventing migration of other metals (Ref 22, 23). These materials have high melting points and form stable oxide species upon heating in air (Ref 3, 24). 304SS is chosen for its low cost and industrially demonstrated passivation and longevity (Ref 3, 24). Galinstan is chosen because pure Ga may solidify when cooled to room temperature during thermal cycling. In the solid phase, Ga has less potential for attack on Al. Therefore, liquid Galinstan emulates worst-case conditions. Galinstan has also been a leading alloy presented in the literature and commercially as a TIM (Ref 17).

To develop samples, a commercially available 3003 series Al sheet (McMaster Carr P#2471T91) is machined into appropriately sized 1 cm $\times$ 1 cm $\times$ 0.5 cm test coupons. The as-received surface finish is left on the surface of the coupons, replicating the surface of as-manufactured commercially available heat mitigation components. Coupons are cleaned with mechanical agitation in room temperature water, followed by ultra-sonication in acetone, ethanol, and DI water. PVD coating of the samples is performed via sputter coating at high vacuum. The source-to-substrate distance is approximately 20 cm, and the substrate is rotated at approximately 5 rpm to allow even and conformal coating to the features on the as-received Al surfaces. The chamber is evacuated to a base pressure of 0.001 Pa and 99.995% pure argon (Ar) is used as the sputtering gas. Deposition takes place at a working pressure of 0.6-0.7 Pa and a flow rate of 15 sccm Ar. Ti is sputtered from a commercially pure Ti target (Lesker P#EJTTIXX272A2) for 1 h at a constant current of 0.35 A, and a voltage that is allowed to fluctuate in the range of 350–450 V. Nb is sputtered from a high purity target (Lesker P#EJTNBXX352A2) for 30 min and is held at the same constant current with variable voltage. Sputtering time is reduced to compensate for the increased sputter rate of Nb. 304SS is sputtered from a target machined from a large rod of the material (Lesker P#89535k65) at a constant current of 0.2 A, with voltage maintained below 550 V for 30 min. The resulting films are uniform across the small sample coupons, are dense without the appearance of micron-scale pores, and are polycrystalline in nature. All films are approximately 100 nm thick, and thickness is uniform within 10% across the sample coupons, as measured via SEM imaging.

One coated sample for each barrier layer candidate is examined by SEM prior to testing. These images are used as a baseline to evaluate any changes in morphology caused by testing or Galinstan exposure. SEM characterization is carried out immediately after deposition.

Three thermal testing protocols are performed: long-term thermal stability, rapid high-temperature cycling, and extended thermal cycling. Each test uses a freshly prepared sample with minimal time between deposition and testing. Thermal tests are performed in ambient on a temperature-controlled laboratory

hot plate. Galinstan used in thermal testing is first created by mixing 68.5% Ga, 21.5% indium, and 10% tin (RotoMetals SKU: LMP-2) by weight in a beaker held at 50 °C. Barrier layers which fail any stage of the testing process are not tested further.

Long-term thermal stability is tested by placing a 5 µL droplet of Galinstan onto the surface of the coated Al coupon. The coupon is positioned on top of a temperature-controlled laboratory hot plate. The temperature is set and controlled to 300 °C, approximately four times the normal operating temperature of a computer central processing unit (CPU). Samples are held static at this temperature for up to 168 h (7 days).

Rapid high-temperature cycling is performed on freshly prepared samples by placing a 5 µL droplet of Galinstan onto the coated coupon. The coupon is placed on the hot plate surface which is maintained at 300 °C. The sample is held on the surface of the hot plate for 120 s and then placed onto a large Al plate, subject to a cross-flow of room temperature air for 60 s. Thermocouple measurements verify that the coupon top surface first reaches 300 °C and subsequently room temperature in each cycle. Cycling is performed either for 50 cycle increments or until color change is evident in the coupon bulk.

Extended thermal cycling is meant to replicate conditions of accelerated device-level use. This test is performed by placing the fresh test coupon with a 5 µL droplet of Galinstan onto the temperature-controlled hot plate. The hot plate is powered on and controlled to 150 °C for 30 min. This temperature is chosen because it is approximately twice the operating temperature of a standard CPU. The samples are exposed to 250 cycles in this extended thermal cycling test sequence. The hotplate is then powered off and allowed to cool in ambient for 30 min.

SEM and EDS characterization are carried out using a Tescan Mira operating at 10-30 keV, equipped with an Oxford EDS unit. Characterization is performed within 24 h of thermal cycling completion. Prior to characterization, the Galinstan droplet is removed from the surface of the sample by ultrasonic cleaning in DI water for 5 min. Samples are then allowed to dry in air. It is noted that any regions of the coating or Al coupon that had become disjoined or mechanically weak are susceptible to removal during this step.

3. Results

Figure 1 shows the surface morphology of the as-received Al coupon. Scratches, pits, and grooves are evident on both the micron and nanometer scale. As a baseline, the uncoated Al coupon is exposed to the long-term stability test of 300 °C for 168 h. Wetting of the Galinstan droplet is evident within 5 min and a color change to dull gray occurs within 10 min. Upon cooling, the entire coupon turned black in color, indicating the formation to Ga-Al intermetallic, and lost all mechanical integrity when moved. An optical image of the transformation is available in the Supporting Information.

During the long-term stability test, the Nb barrier layer showed wetting within 30 min. Delamination of the Nb film was visible within 60 min. After allowing the sample to cool, the region wetted by the Galinstan experienced dramatic volumetric expansion and was black in color. When allowed to sit undisturbed for 12 h at room temperature, the entire bulk of the coupon turned black and lost all mechanical integrity. Due to the state of the coupon, no SEM analysis was performed on the Nb-coated sample.

The 304SS-coated coupon showed no changes in the wetting state or color of the Al coupon after 168 h (7 days) at 300 °C. After cooling, the sample was sonicated to remove the Galinstan droplet and any of the coating or bulk that had lost mechanical integrity. Figure 2 shows a SEM micrograph of a portion of the surface under the droplet. In this region, bottom of the figure, the barrier layer was compromised, and cratering of the underlying bulk can be seen after sonication.

Unlike the other barrier layers, Ti barrier layer-coated coupons did not exhibit damage after 168 h at 300 °C. Figure 3 presents SEM micrographs of the resulting surface features on the Ti-coated sample in progressively greater magnification. Inspection of the micrographs shows that no visible cracks have formed on the surfaces on the respective length scales of each of the micrographs. Even through sonication, no gaps in the coatings are visible in the micrographs and none of the underlying Al coupon has been cratered. However, it is evident that material from the droplet has deposited onto the surface and was not removed during sonication. An additional SEM micrograph of the Ti surface as fabricated is available in the Supporting Information.

SEM microscopy with EDS was used to determine the composition of the deposits on the surface that remain after sonication. This analysis rules out migration of Al through the

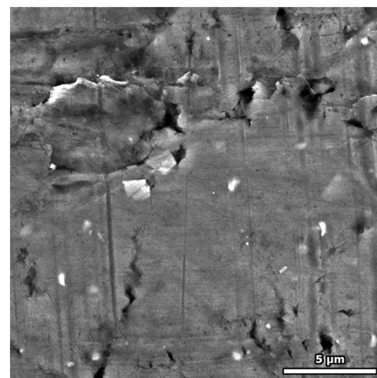

Fig. 1 SEM micrograph of the as-received Al coupon surface

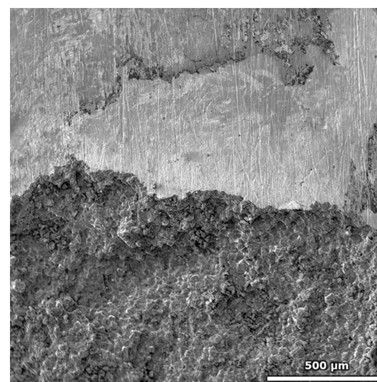

Fig. 2 304SS-coated Al coupon surface micrograph, showing an undamaged region at the top and cratered damaged region at the bottom

Ti layers. Figure 4 presents the SEM micrograph and EDS elemental panel of a Ti-coated coupon after long-term stability testing. The EDS panel shows deposits of two distinct compositions, inferring two different materials have been deposited onto the surface. One region is composed of Ga and oxygen, indicating Ga-oxide deposition, and the second region is composed of Ga, tin, and indium, indicating intermetallic compositions. Sharp faceted surfaces are evident in Fig. 3 and 4, indicating a high probability of crystallinity in some regions.

Only Ti-coated samples were tested further. Ti-coated samples were cycled from 300 °C to ambient within 3 min in the rapid thermal cycling experiment. After 50 cycles, cracking and oxidation of the Ti coating is evident in the SEM micrographs presented in Fig. 5. Deposits of Ga and oxygen, as well as Ga, tin, and indium similar to those observed in the long-term thermal stability test are also present. It is noteworthy that the cracks remain on the order of nanometers, and penetration by high surface area Galinstan is not apparent due to lack of deposition inside the cracks. Further, after the cycling intervals were completed, the sample remained undisturbed for 24 h and no color change was evident in the underlying Al coupon. After sonication, some areas of the Ti coating ~ 10 µm in size detached from the underlying coupon.

SEM examination of the areas below the detached regions shows no modification to the morphology of the underlying Al coupon. EDS analysis of the area shows no presence of Ga, In, or Sn in the region, indicating that no Galinstan was able to navigate to the underlying coupon. These results are shown in Fig. 6.

A Ti-coated sample was then subjected to extended thermal cycling tests at 150 °C. Figure 7 shows a SEM micrograph of the coated coupon after testing. Unlike the higher temperature cycling at 300 °C, the surface after 250 cycles of 30 min in duration shows no cracking or deposition, remaining nearly indistinguishable from the as-fabricated surface (SEM micrographs shown in the Supporting Information).

4. Discussion

A brief justification of the choices of materials and methods is in order. Experimental methods were selected to replicate cases of accelerated exposure and worst-case scenarios in device-level applications. Barrier coating materials were chosen from materials widely used in industry and readily adoptable into existing fabrication processes. Instead of using a solid-state Ga-based amalgamation in this investigation, a liquid alloy was used to provide the greatest possible Ga mobility. Temperatures of testing were chosen to remain below the melting point of Al, but at intervals above the current operational temperature of CPUs and IC devices. Chosen temperatures are in the range expected for next-generation ICs.

Based on prior literature results, it is unlikely that the barrier layers of 304SS and Nb failed due to chemical reaction with Ga, as both materials are known to be non-reactive with Ga (Ref 18). Due to a large mismatch of thermal expansion coefficient between the barrier film and the Al substrate, crack formation is possible in all barrier layers, as observed in Fig. 5 (Ref 24). If a crack is to form

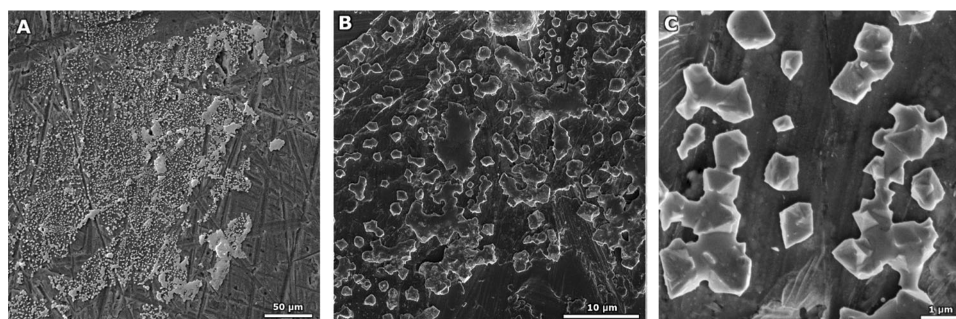

Fig. 3 SEM micrographs of Ti-coated coupons subject to a droplet of Galinstan for 168 h at 300 °C in ambient at progressively greater magnifications (a)–(c). Increasing magnification is carried out in the top right quadrant of each image

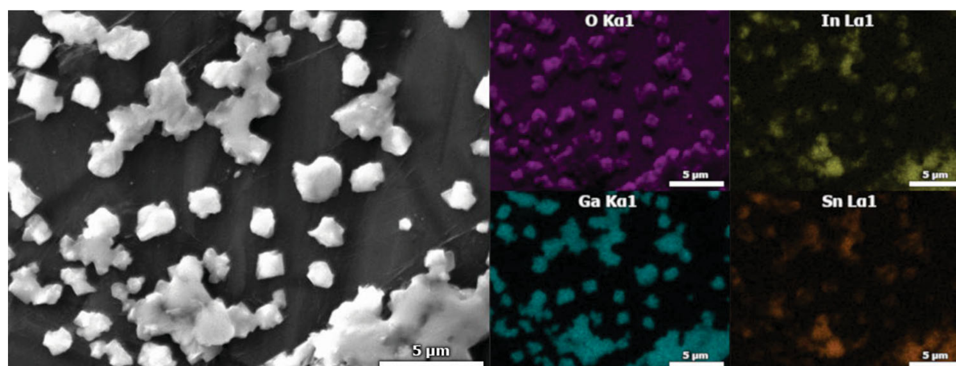

Fig. 4 An SEM micrograph of the Ti surface deposits, with accompanying EDS maps, after exposure to Galinstan for 168 h at 300 °C

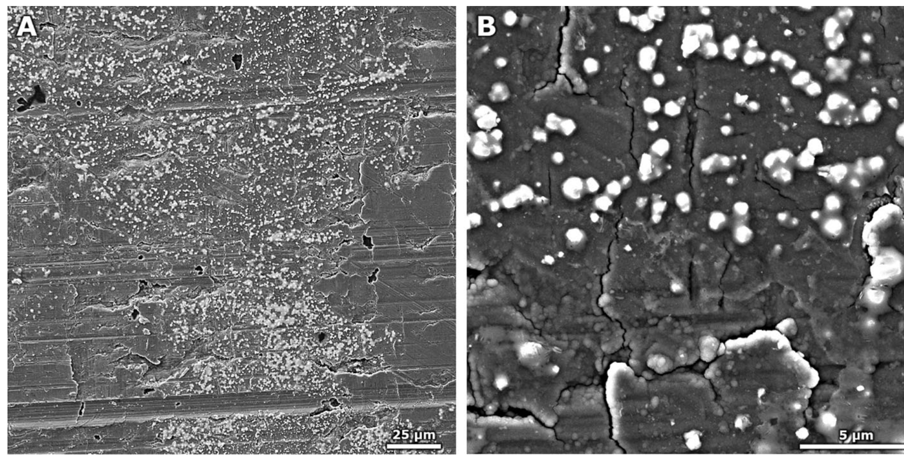

Fig. 5 SEM micrographs of rapidly thermally cycled Ti-coated coupons which have been exposed to 50 cycles from 300 °C to room temperature. The left panel (a) is a wide area image, and the right panel (b) is a higher magnification image

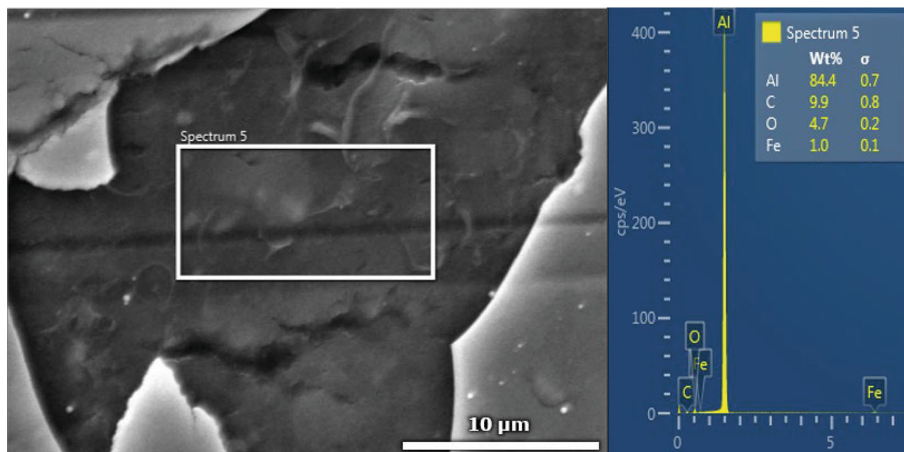

Fig. 6 SEM analysis of a region of the Al coupon where the Ti coating came detached after thermal cycling and sonication. Selected area, the white box, EDS analysis shows no presence of Ga, In, or Sn in the spectra

and Galinstan wets the exposed material at the crack edge, the crack can fill and Ga may reach the substrate, such as in the Wenzel wetting state (Ref 25). Alternatively, if Galinstan does not wet the exposed material at the crack edge, a Cassie-Baxter wetting state with air or vacuum occupying the crack is possible (Ref 26, 27). Here, we hypothesize that the Ti barrier layers may be further oxidized than the Nb and 304SS films under the same conditions, due to more rapid oxidation kinetics at elevated temperatures in air. Expanding on measured trends from results observed in the literature, the authors estimate that the oxide layer is less than 10 nm before heating and is between 10 and 20 nm when heated to 300 °C in air (Ref 28). Because of the Ti oxide, the Galinstan does not wet the exposed crack edges of Ti, unlike Nb and 304SS. Wetting characteristics of Ga-based alloys on metals and metal oxides are not well represented in the literature, and further investigation is needed to fully understand the transport mechanism. Further, the excellent chemical stability of both Ti and its oxides aids in the long-term stability at elevated temperatures that was observed in this work. Additionally, further investigation into the long-term interfacial and chemical interactions between Ti and its oxides and Ga-based alloys is needed.

This study exposes several opportunities for industrially relevant improvements in thermal management of ICs and CPUs. First, the experiments here may simulate the case where Galinstan is used as a TIM between a CPU die and a barrier layer-coated Al heat sink. The Ti barrier layer subjected to thermal cycling experiments at 150 °C showed no failure under simulated worst-case conditions. This suggests that real-world use of liquid Ga thermal interfaces at current CPU temperatures of ~ 75 °C only requires the addition of a Ti barrier layer. Devices operating at higher temperatures may result in deposition of solid Ga-, In-, and Sn-based materials. These crystalline nanostructures at the interface may result in increased interfacial area and improved heat transfer across the interface (Ref 28). Further study of these structures may open a pathway to further improvements in TIMs and bonding of thermal interfaces for next-generation devices.

5. Conclusions

In this paper, we investigate the use of thin-film barrier layers deposited using PVD to prevent the intrusion and alloying of Ga into Al, a material which is commonly used in thermal management for integrated circuit devices. Through accelerated thermal exposure experiments of a liquid Galinstan droplet in ambient, it is found that Nb and 304SS thin films do not provide sufficient protection of Al. Ti films of 100 nm

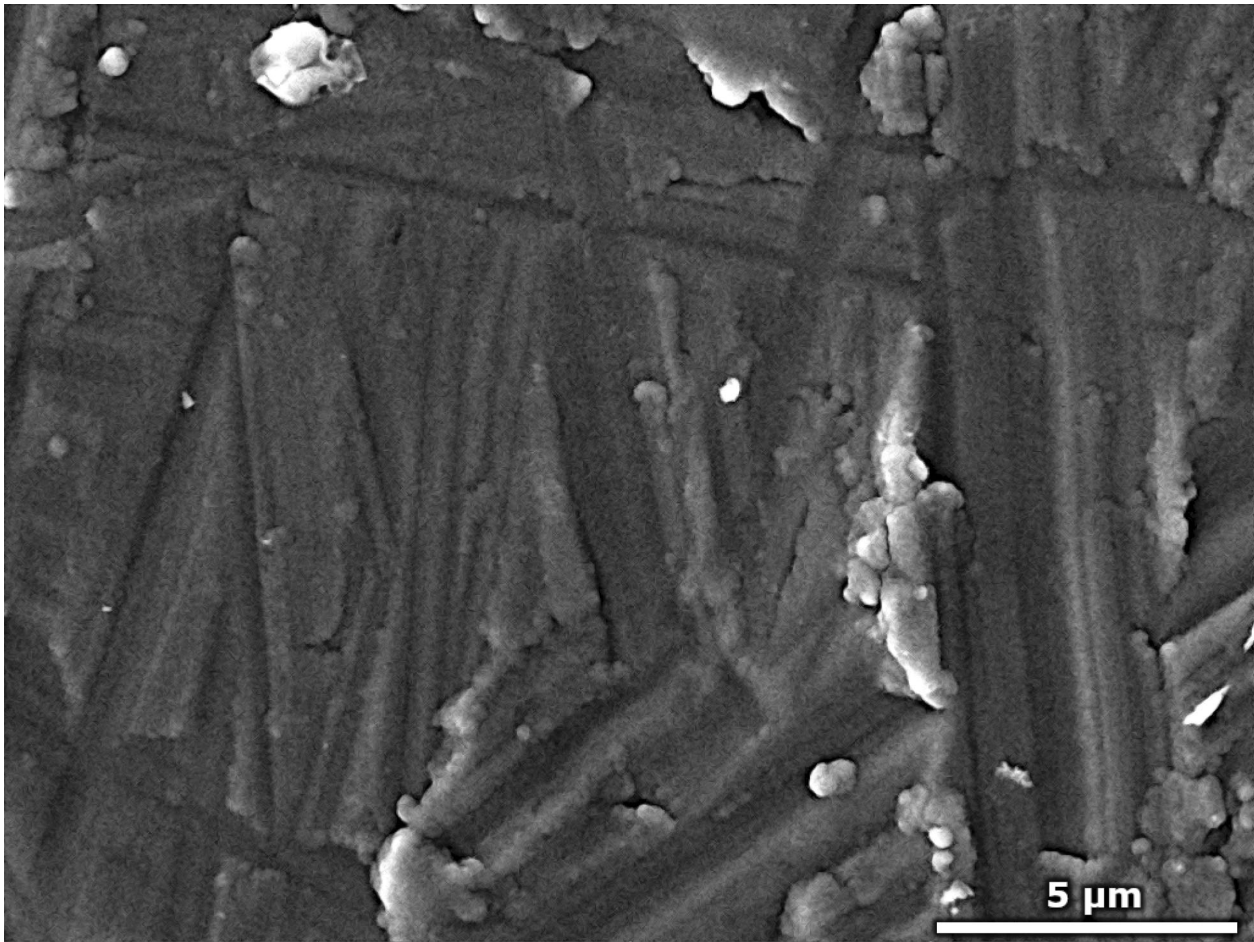

Fig. 7 SEM micrograph of the surface of a Ti-coated coupon after exposure to a liquid Galinstan droplet for 250 cycles from ambient to 150 °C

thickness showed protection under all test conditions. After 250 cycles from room temperature to 150 °C, no changes are evident in Ti barrier films and no deposition of the Galinstan material occurs. When the temperature of cycling is increased to 300 °C, nanoscale cracking and deposition of nanosized domains of Ga, In, Sn, and O occurs, but the underlying Al remains free of Ga. This work creates a direct path to the use of Ga-based TIMs to improve heat transfer on current IC devices through the addition of only a thin inexpensive barrier layer. This opens an immediate opportunity for substantial improvements in device-level power density and performance.

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Author Contributions

SS, GB, and JN collaborated to develop the concept and experimental protocol. SS and NB did the experiments and characterization. All authors contributed to the analysis of characterization results. All authors participated in the preparation of the manuscript. Funding Sources

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