# The Effects of Glass-Substrate's Surface-Treatment on the Characteristics of N-Channel Polycrystalline Silicon Thin Film Transistors

Y.Z. WANG and O.O. AWADELKARIM

Electronic Materials and Processing Research Laboratory, The Pennsylvania State University, University Park, PA 16802

We have examined the performance and hot-carrier stress reliability of n-channel polycrystalline silicon (poly-Si) thin film transistors (TFTs) on RCA-leached glass. We have found out that the TFT's performance and reliability are improved by RCA-leaching of the glass when compared to TFTs on bare glass due to the formation of a silica-rich layer on the glass surface by the RCA-leaching. The silica-rich layer acts as a barrier for impurity diffusion from glass as well as it modifies the poly-Si/glass interface which determines the physical structure of the active poly-Si.

**Key words:** Polycrystalline silicon, RCA leaching, thin film transistor

## INTRODUCTION

The use of glass as substrates for the fabrication of polycrystalline silicon (poly-Si) thin film transistors (TFTs) has enabled active matrix-liquid crystal displays to achieve widespread use in flat panel display technology.[1,2] However, the impurities in glass and the diffusion of these impurities into poly-Si during the TFT processing affect the quality of TFTs.[3,4] The introduction of a dielectric barrier layer, such as silicon oxide or silicon nitride, between poly-Si and glass is an effective way of inhibiting impurity diffusion from the glass substrate into the active poly-Si layer in the poly-Si TFT.[5,6] Nonetheless, an RCA-cleaned glass substrate was recently found to have a silica-rich surface region formed by chemical leaching, which may be able to function as a diffusion barrier-layer.[7] In this letter, we report and compare the effects of RCA-leaching glass substrates and thin silicon oxide-coating glass substrates on the performance and hot carrier stress (HCS) reliability of n-channel poly-Si TFTs (n-TFTs). The performance and HCS reliability of the TFTs on these two substrates are also contrasted to those of TFTs on bare glass substrates.

## RESULTS AND DISCUSSION

Corning Code 1737 glass substrates were employed in this study. For RCA-leached glass, the glass substrates were immersed in warm (75°C) baths of $NH_4$/$H_2O_2$/$H_2O$ and HCl/$H_2O_2$/$H_2O$ for 10 min each, and then rinsed in high-resistivity deionized water. For thin silicon oxide-coated glass, low-pressure chemical vapor deposition (LPCVD) was employed to deposit a $SiO_2$ coating layer with a thickness of 120Å atop the glass substrate. Thereafter, top-gated poly-Si TFTs were fabricated on these RCA-leached glass, $SiO_2$-coated glass, and bare (no surface treatment except for HF cleaning of the surface) 1737 glass substrates. The nominal channel width and length of the TFT are 15 μm each. LPCVD was also used to deposit 1000Å of base poly-Si at 620°C on these substrates. The poly-Si channel layer was patterned using photolithography and wet chemical etching. This was followed by a LPCVD deposition of 1000Å thick $SiO_2$ gate oxide at 450°C and another 620°C LPCVD of 3500Å thick gate poly-Si. Upon the completion of the gate poly-Si definition wet etching, the devices were ion implanted (self-aligned) for drain and source with $1 \times 10^{15}$ cm$^{-2}$ of P at 105 keV. The implanted devices were then capped with 4000Å of LPCVD $SiO_2$ at 450°C, and annealed at 600°C for four hours to activate the P dopants. The TFT fabrication was then completed by a lift-off process that was used to define aluminum contacts, and by a contact annealing for 30 min at 400°C in $H_2$ gas. The TFTs were subsequently hydrogenated in an electron cyclotron resonance (ECR) plasma source using hydrogen gas for 2 h. Each substrate carried an

(Received June 18, 1998; accepted September 9, 1998)

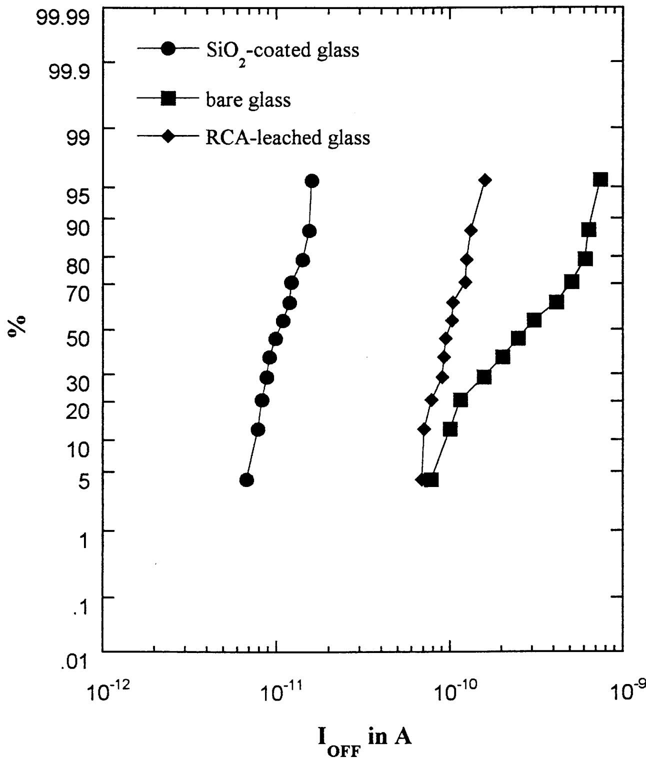


Fig. 1. Cumulative probability plots of $I_{OFF}$ of n-TFTs fabricated on RCA-leached glass, $SiO_2$-coated glass and bare glass substrates. $I_{OFF}$ was extracted from $I_d$ vs $V_g$ plots measured at $V_{ds}$ = +10V directly after fabrication.

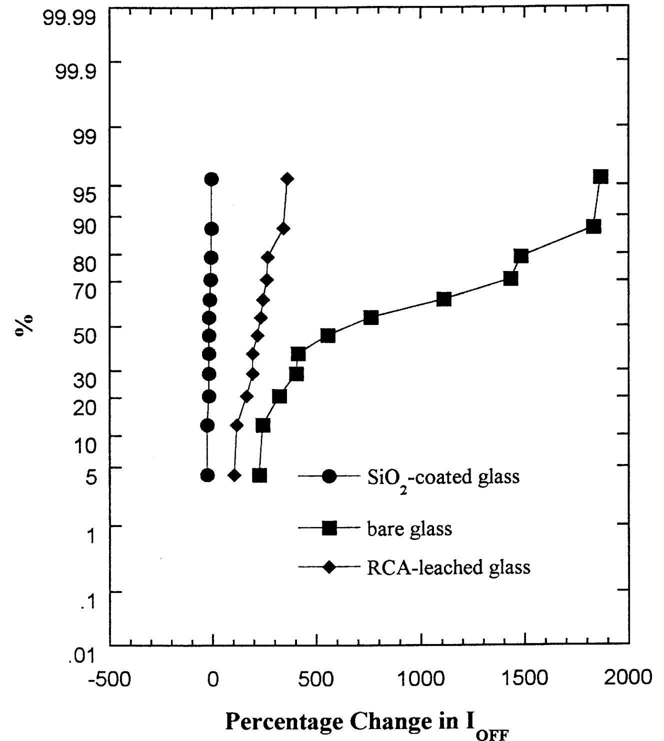


Fig. 2. Cumulative probability plots of percentage changes in $I_{OFF}$ of n-TFTs fabricated on RCA-leached glass, $SiO_2$-coated glass and bare glass substrates after the application of HCS. The data were extracted from $I_d$ vs $V_g$ plots measured at $V_{ds}$ = +10V.

array of 11 × 11 identical TFTs.

The n-TFTs were characterized, using a computer controlled HP 4142B semiconductor parameter analyzer, directly after fabrication and after the application of HCS which was performed at a gate voltage $V_g$ = +20 V and a drain to source voltage $V_{ds}$ = +40 V applied for 5 min. The transistor parameters were extracted from drain current vs gate voltage characteristics ($I_d$ vs $V_g$) measured at $V_{ds}$ of +10 V and for $-10 \text{ V} \leq Vg \leq +20 \text{ V}$. The measured parameters are the OFF current, $I_{OFF}$, defined as the minimum of $I_d$ measured at $V_{ds}$ = +10 V, the threshold voltage, $V_{th}$, defined as $V_g$ which gives 1% of the maximum $I_d$; and the subthreshold swing, S, obtained as the reciprocal slope of the linear region in the semi-log transfer characteristics before the transistor is turned on. For each set of TFTs, more than 12 devices were measured in order to generate cumulative plots.

Figure 1 shows cumulative probability plots of $I_{OFF}$ in the n-TFTs. One can see from this figure that $I_{OFF}$ ~$10^{-10}$ to $10^{-9}$ A is highest in TFTs on bare glass, and one to two orders of magnitude lower in TFTs on $SiO_2$-coated glass. $I_{OFF}$ in TFTs on RCA-leached glass lies in between at ~$10^{-10}$ A. We also examined other parameters such as $V_{th}$ and S for these same TFTs of Fig. 1. $V_{th}$, varied between 0 and 1 V in TFTs on $SiO_2$-coated glass to ~2 V in TFTs on bare glass and ~3 V in TFTs on RCA-leached glass. These ranges and signs of $V_{th}$ indicate that an overall negative charge buildup takes place in the bulk gate oxide and interface of the n-TFTs, and this charge buildup is lowest in n-TFTs on $SiO_2$-coated glass. S also exhibited a dependence on the substrate's treatment; S is highest in TFTs on bare glass and lowest in TFTs on $SiO_2$-coated glass. S in TFTs on RCA-leached glass is found to be close to that in TFTs on $SiO_2$-coated glass. This suggests that the gate oxide/poly-Si interface is of a relatively better quality in a TFT on RCA-leached glass or in a TFT on $SiO_2$-coated glass than in a TFT on bare glass. The data presented in Fig. 1 and the effects in $V_{th}$ and S, reported above, establish a clear dependence of TFT's performance on the treatment of the glass substrate. In summary, n-TFTs on bare glass substrates exhibit degraded transistor parameters which are markedly improved by the inclusion of a deposited $SiO_2$ layer between the substrate and the poly-Si. More importantly, however, the n-TFT's performance may be significantly enhanced by RCA-leaching the glass substrate.

Figure 2 shows cumulative probability plots of the percentage change in $I_{OFF}$ produced by the application to the n-TFTs of our HCS described above. Percentage change in $I_{OFF}$ is estimated relative to the pre-stress $I_{OFF}$. It is clear in Fig. 2 that TFTs on bare glass undergo the largest HCS-induced degradation in $I_{OFF}$, with the maximum increase in $I_{OFF}$ of ~1850%. On the other hand, n-TFTs on $SiO_2$-coated glass are, apparently, resistant to HCS and the induced degradation in $I_{OFF}$ of these TFTs is negligibly small. The increase in $I_{OFF}$ generated by the HCS in the n-TFTs on RCA-leached glass is ~200%. Even though this increase in

$I_{OFF}$ is large, it is still a significant improvement over that in TFTs on bare glass substrates. Figure 3 shows cumulative plots of the shift in $V_{th}$ with HCS. Very little or no shifts in $V_{th}$ with HCS are observed in TFTs on the $SiO_2$-coated glass, and $V_{th}$ shifted with HCS to more negative values in the rest of the n-TFTs. This negative shift in $V_{th}$ is less than 0.4 V in magnitude in n-TFTs on RCA-leached glass, whereas it is larger than 1.0 V in magnitude in n-TFTs on bare glass substrates. The negative shift in $V_{th}$ suggests that a positive charge accumulation and/or a negative charge neutralization has taken place in the gate oxide of the device during the HCS. Similarly, our results on S as shown in Fig. 4 for these same transistors indicate that the n-TFTs on $SiO_2$-coated glass and on RCA-leached glass are more HCS reliable as can be seen by the very small changes in S arising from the application of HCS. In contrast, a ~60% increase in S is produced by HCS in TFTs on the bare glass substrates.

In Fig. 1 through Fig. 4, we have shown that RCA-leaching the glass substrate improves the quality of the n-TFTs with regard to transistor performance and transistor immunity to HCS. In spite of our observation that the quality of TFTs on the RCA-leached glass substrates is not as good as that of TFTs on $SiO_2$-coated glass substrates, nonetheless, our results clearly demonstrate the impact of the RCA-leaching of glass in enhancing TFT performance and HCS reliability.

We have recently shown that poly-Si deposited on bare glass has higher content of electrically active traps compared to poly-Si deposited on $SiO_2$-coated glass substrates.[6] These traps are associated with grain boundaries, isolated impurities, or impurity complexes in poly-Si on bare glass which has smaller grains and higher contents of impurities such as Al and Ba.[5,6] Impurity diffusion from glass into poly-Si is apparently inhibited by the $SiO_2$ coating; this is why impurity content in $SiO_2$-coated glass is low.[6] On the other hand, the difference in grain size of the poly-Si is, presumably, due to the impurity content of the poly-Si as well as the difference in stress and/or structure at the poly-Si/glass interface in poly-Si on bare glass and at poly-Si/$SiO_2$ interface in poly-Si on $SiO_2$-coated glass since these interfaces control grain growth.[8]

Higher concentration of trapping states near the drain in the n-TFT on bare glass is responsible for the higher level of $I_{OFF}$ observed in these TFTs.[9,10] After HCS the increase in $I_{OFF}$ is attributed to the generation of electron traps in the channel edge adjacent to the drain. These traps when populated by electrons give rise to a negative charge that enhances the electric field for the trap-assisted tunneling, which is the mechanism responsible for $I_{OFF}$ generation.[10] The increase in $I_{OFF}$ is largest in n-TFTs on bare glass, which suggests that HCS-induced electron traps are denser in these TFTs. This is because the largest concentrations of grain boundary and impurity traps are in these TFTs on bare glass; the traps are passivated by hydrogenation and subsequently electrically de-passivated by HCS.[11]

Leaching glass substrate using RCA clean is expected to result in the formation of a silica-rich layer

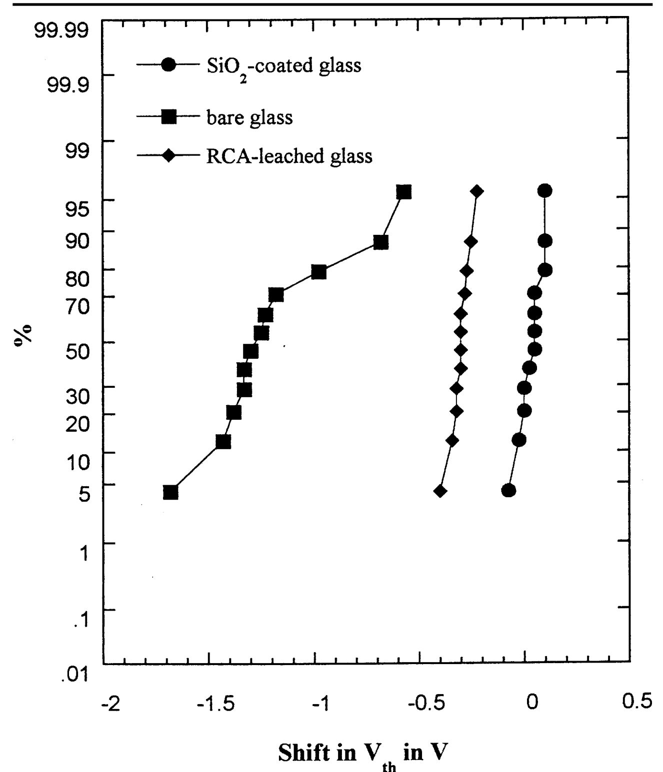


Fig. 3. Cumulative probability plots of shifts in $V_{th}$ associated with the n-TFTs in Fig. 2 after the application of HCS.

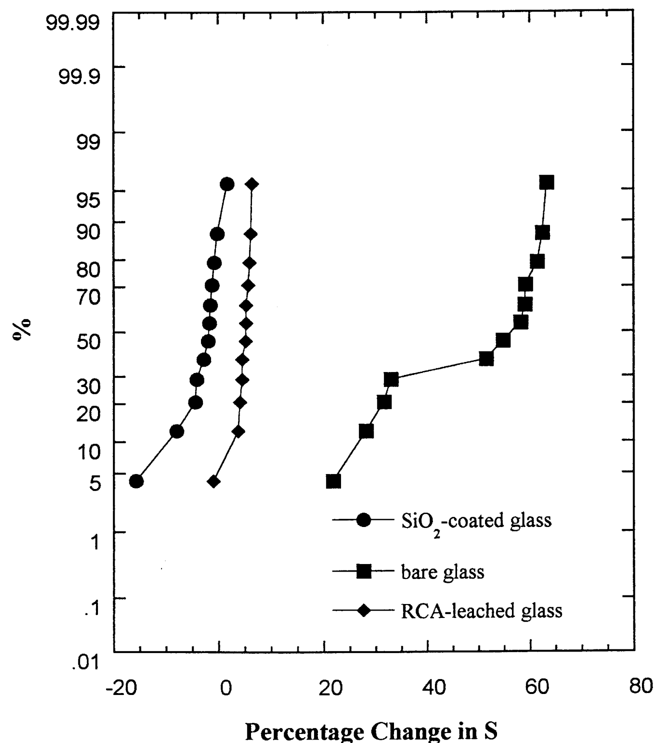


Fig. 4. Cumulative probability plots of percentage changes in S associated with the n-TFTs in Fig. 2 after the application of HCS.

on the glass surface, and this layer can be used as an impurity diffusion barrier instead of a deposited silicon oxide or silicon nitride. From transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS), and electron spectroscopy for chemical analysis (ESCA) measurements, it has been found that a thin amorphized silica-rich layer does indeed form on the glass surface after the glass is immersed in RCA bath for 10 min.[7] Cross-sectional TEM micrographs reveal that the silica-rich surface layer is ~ 30Å thick after a 10 min RCA clean, such as the one used here, and that the layer thickness increases with the RCA clean time.[7] This amorphized surface layer comprises silicon and oxygen network, and the atomic concentrations of glass components such as Al, B, and Ba in the layer are greatly reduced. The silica-rich surface layer is, seemingly, able to mimic the $SiO_2$ coating in that it inhibits impurity diffusion from glass into the poly-Si and in that it modifies the poly-Si interface with the substrate. However, the silica-rich layer does not enhance TFT characteristics as efficiently as the $SiO_2$ coating does as witnessed by the significantly superior qualities of the n-TFTs on the $SiO_2$-coated glass. This can be attributed to the much thinner silica-rich layer as compared to the $SiO_2$ coating. Moreover, the composition and porosity of the silica-rich layer may also be a contributing factor.

## SUMMARY

We have examined the performance and HCS reliability of n-TFTs on RCA-leached glass, and compared them to TFTs on $SiO_2$-coated glass and on bare glass substrates. It is found that the TFT performance and HCS reliability are improved by RCA-leaching of the glass as compared to TFTs on bare glass. This is because of the formation of a silica-rich surface layer on the aluminoborosilicate glass substrate by the RCA leaching. However, the improvement in the n-TFT's performance and HCS reliability brought about by RCA-leaching of the glass does not match that brought about by the deposition of a thicker $SiO_2$ layer atop the glass surface.

## ACKNOWLEDGMENT

The authors are grateful to Dr. J.G. Couillard at Cornell University for TFT fabrication.

## REFERENCES

1. Aiguo Yin and S.J. Fonash, *J. Vac. Sci. Technol. A* 12, 1237 (1994).
2. I.-W. Wu, *Solid State Phenomena* 37-38, 553 (1994).
3. Y.Z. Wang, O.O. Awadelkarim, J.G. Couillard and D.G. Ast, *Solid State Electron*. 42, 1689 (1998).
4. Y.Z. Wang, O.O. Awadelkarim, J.G. Couillard and D.G. Ast, *Semicond. Sci. Technol.* 13, 532 (1998).
5. Y.Z. Wang, S.J. Fonash, O.O. Awadelkarim and T. Gu, submitted to *J. Electrochemi. Soc.* (1998).
6. Y.Z. Wang and O.O. Awadelkarim, submitted to *Microelectronics and Reliability*, (1998).
7. J.G. Couillard, D.G. Ast, and F.P. Fehlner, *J. Non-Crystal. Solids* 222, 429 (1997).
8. R. Kingi, Y.Z. Wang, S.J. Fonash, O.O. Awadelkarim, J. Mehlhaff and H. Hovagimian, *Mater. Res. Soc. Symp. Proc.,* 424, (Pittsburgh, PA: Mater. Res. Soc., 1997), p. 237.
9. A.W. DeGroot, G.C. McGonigal, D.J. Thomson and H.C. Card, *J. Appl. Phys.* 55, 312 (1984).
10. S. Banerjee, R. Sundaresan, H. Shichijo and S. Malhi, *IEEE Trans. Electron Dev.* 35, 152 (1988).
11. V. Suntharalingam and S.J. Fonash, *Appl. Phys. Lett.* 68, 1400 (1996).