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Optimization of the Base Electrode for InGaAs/InP DHBT Structures With a Buried Emitter-Base Junction

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We have optimized the base electrode for InGaAs/InP based double heterojunction bipolar transistors with a buried emitter-base junction. For the buried emitter-base structure, the base metal is diffused through a thin graded quaternary region, which is doped lightly n-type, to make ohmic contact to the p^+InGaAs base region. The metal diffusion depth must be controlled, or contact will also be made to the collector region. Several metal schemes were evaluated. An alloy of Pd/Pt/Au was the best choice for the base metal, since it had the lowest contact resistance and a sufficient diffusion depth after annealing. The Pd diffusion depth was easily controlled by limiting the thickness to 50Å, and using ample Pt, at least 350Å, as a barrier metal to the top layer of Au. Devices with a 500Å base region show no degradation in dc characteristics after operation at an emitter current density of 90 kA/cm^2 and a collector bias, V_{CE}, of 2V at room temperature for over 500 h. Typical common emitter current gain was 120. An f_t of 95 GHz and f_{max}, of 131 GHz were achieved for 2×4 µm^2 emitter size devices.

Key words: Base electrode, double heterojunction bipolar transistors (DHBTs), InGaAs/InP

INTRODUCTION

We use a buried extrinsic emitter-base junction for improved device reliability in our InGaAs/InP double heterojunction bipolar transistors (DHBT).[1] For our buried emitter-base structure, the base metal is diffused through a thin graded quaternary region, which is doped lightly n-type, to make ohmic contact to the p^+InGaAs base region. The diffusion depth is critical. If the metal does not diffuse far enough, the base electrode will have a high contact resistance or be non-ohmic. If the metal diffuses too far into the semiconductor, it will also contact the collector region and cause base-collector junction leakage or shorts. Several metal schemes were evaluated, including Pd/Pt/Au, Pt/Ti/Pt/Au, Pd/Ti/Pt/Au, Ti/Pt/Au, and AuBe/Pt/Au. These particular metals were chosen, since they are commonly used for ohmic contacts in III-V materials.[2–6] Pt and Ti tend to have a fairly smooth diffusion profile when annealed at our maximum processing temperature of 300°C.[2–4] Although Pd and Au have rougher diffusion profiles, some work has indicated that if they are thin enough, they may also be used.[5] Furthermore, Pt is an excellent diffusion barrier to Au at our processing temperature of 300°C, provided it is thick enough to avoid pinholes or other defects, so Au can be used as the top metal for all of the subsequent interconnects.[6,7]

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The metals were evaluated in the DHBT structure using transmission line measurements (TLMs) on the base region to determine the contact resistance (Rc) and sheet resistance (Rs) after annealing. Any nonlinearity in the TLM data indicated that the metal had also contacted the collector region of the device. Base-collector diode measurements were also performed on these structures for comparison. Rutherford backscattering (RBS) was performed on InGaAs samples to determine the diffusion depth profile of the metals after annealing. The RBS depth profiles and TLM data agreed well with device results to determine the optimum base metal scheme. The alloys that had the appropriate depth profile and lowest contact resistance were evaluated in DHBT devices. Both large-area non-self-aligned and small self-aligned devices were fabricated for dc and rf measurements.

EXPERIMENTAL

The DHBT structure, grown by metalorganic molecular beam epitaxy (MOMBE), is shown in Fig 1. Wafers with a base thickness ranging from 200 to 500Å were evaluated. A small-area self-aligned processed device is shown in Fig. 2. The fabrication procedure is as follows. The emitter contact, defined by liftoff, 50Å Pd + 350Å Pt + 1000Å Au, was also used as the etch mask. The n^+InGaAs was selectively wet etched to the n InP. An additional overetch was performed to obtain an undercut of 5000Å under the metal contact. This n^+InGaAs acts as a mask for the

Composition	Thickness(Å)	Doping(cm^{-3})
n+$In_{0.53}Ga_{0.47}As$	2500	$3x10^{19}$
n InP	500	$5x10^{17}$
InGaAsP (1.13eV)	70	$1x10^{17}$
InGaAsP (0.95eV)	70	$1x10^{17}$
p+$In_{0.53}Ga_{0.47}As$	500	$3x10^{19}$
$In_{0.53}Ga_{0.47}As$	200	-
n $In_{0.53}Ga_{0.47}As$	300	$1x10^{17}$
InGaAsP (0.95eV)	130	$1x10^{17}$
InGaAsP (1.13eV)	130	$1x10^{17}$
n InP	4000	$3x10^{16}$
n+$In_{0.53}Ga_{0.47}As$	4000	$3x10^{19}$

Fig. 1. MOMBE grown DHBT structure.

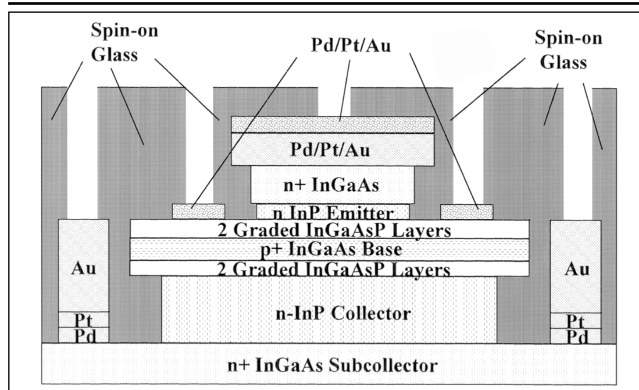

Fig. 2. Processed InGaAs/InP self-aligned DHBT device.

subsequent selective n InP wet etch. The emitter metal was then used as a shadow mask for the self-aligned base contact, deposited at this step. The structure was then encapsulated in spin-on glass (SOG). The base mesa was patterned and etched as follows. The p^+InGaAs base, quaternary layers, and n-InP collector were electron cyclotron resonance (ECR) plasma etched in BCl_3/N_2 to 2000Å before the n^+InGaAs collector contact. The remaining n-InP was selectively wet etched to the n^+InGaAs, the n-InP collector was then selectively undercut about 2 μm to reduce the collector-base capacitance of the device. The collector mesa was wet etched, 50Å Pd + 350Å Pt + 6000Å Au collector contacts were deposited, and the entire structure was encapsulated in SOG. Via holes were plasma etched in the SOG for subsequent contacts. The wet and dry etch conditions have been described previously.[8] Note that the extrinsic emitter-base junction is buried and the self-aligned base metal is diffused through the thin quaternary layers, which are doped lightly n-type, to make ohmic contact to the base region. Several base metal schemes were evaluated, including Pd/Pt/Au, Pt/Ti/Pt/Au, Pd/Ti/Pt/Au, Ti/Pt/Au, and AuBe/Pt/Au, in terms of diffusion depth into the semiconductor after annealing and minimum contact resistance. During processing, the wafers were annealed during each SOG curing cycle of 300°C for 10 min. Fabricated wafers were coated two to three times with SOG during normal processing, and thus, were annealed at 300°C for 20 to 30 min.

TLMs were performed on samples which had the metal layers deposited on the graded quaternary layers on top of the p^+InGaAs region in our DHBT structure with a 500Å base. TLM data were obtained by plotting resistance vs a gap width of 4 to 300 μm for pads of 200 μm in width by 75 μm length. Large-area devices were fabricated on structures with a base layer thickness varying from 200 to 500Å, with some of the metal schemes to determine base-collector leakage before and after annealing. Small devices were fabricated with the optimum base electrode for radio frequency (rf) measurements. All of the metal films were deposited in an Airco-Temescal e-beam evaporator at a gun bias of 10 KeV, a base pressure of 1×10^{-7} Torr, and a deposition rate of 2 to 6Å/s. The deposited metal thickness was controlled during evaporation using an in-situ crystal monitor.

RBS measurements were performed on samples with the metal layers deposited on InGaAs both before and after annealing at 300°C for 30 min. InGaAs was used instead of the actual base layer structure, since the most of the base layer is InGaAs with only a thin graded quaternary region. This simplifies the RBS data analysis. RBS was performed using a National Electrostatics Corporation 3SDH1MV tandem accelerator with a Charles Evans and Associates 400 end station. Data acquisition and reduction was performed using HYPRA™ software. RBS spectra were acquired at a backscattering angle of 160° with the sample perpendicular to the incident ion beam using a He^{++} ion beam energy of 2.275 MeV. Spectra were acquired with the sample in a "rotating random." In this orientation, inadvertent channeling of the incident ions in the III-V substrate is avoided and the signal from the substrate can be used as an internal reference. A sample is described by fitting a theoretical RBS spectrum to the experimental spectrum. A density is assumed for each layer of the model in order to present the results in units of atomic concentration vs depth. For single element films, where the density of the material typically matches that of the bulk density, thickness accuracy is quite good. For multi-element films, HYPRA™ calculates a composite density for a given layer using the bulk densities and normalizing each density by the concentration of the corresponding element. The RBS spectra are fit by applying a theoretical model and iteratively adjusting elemental concentrations until good agreement is found between the theoretical curve and experimental spectrum. Depth accuracy was estimated to be ± 50Å. Since Pt and Au are indistinguishable with RBS, the initial Pt thickness and its resulting depth profile were assumed from the as-deposited thickness of both the Au and Pt layers.

RESULTS AND DISCUSSION

The metallization schemes listed in Table I were evaluated for optimization of the base electrode in terms of metal diffusion into the semiconductor and

Rc to the base region. TLM data were obtained for the metal schemes deposited on the base layer of a DHBT structure with a 500Å base. RBS measurements were performed on structures with the metals deposited on InGaAs both before and after annealing at 300°C for 30 min, the maximum annealing time during wafer processing. Several DHBT structures with a base thickness of 200 to 500Å were then evaluated with the optimum base electrode for dc and rf measurements.

TLM data were obtained after annealing the samples at 300°C in increments of 10 min each to simulate the SOG curing cycles. Rc and Rs were determined from these measurements for all of the alloys. As an example, some of the TLM plots are shown in Fig. 3. This is the data obtained for the alloys A, B, C, G, H, and K, after annealing the samples at 300°C for 30 min. Any deviation from linearity indicates that the metal has penetrated into the collector region. When the metal has made contact to the collector region, as with alloys A, B, and K, the line is not linear, and Rs is lower than with the other alloys. Alloys C, G, and J, on the other hand, did not contact the collector region. These lines are linear, therefore, Rs and Rc can be accurately calculated. Figure 4 shows the minimum Rc obtained for each metal scheme. The high Rc obtained for alloys G, H, I, and J indicate that they did not diffuse far enough to penetrate the graded quaternary layers sufficiently and make a low resistance contact to the base region. Therefore, the diffusion depth for these latter alloys was between 0 and 140Å.

The RBS measurements were evaluated next. RBS measurements were performed on samples which had the metal deposited on InGaAs, both before and after annealing at 300°C/30 min. The RBS measurements on the samples before annealing were used as controls to determine the initial metal thickness. The initial metal thickness was also compared with the data from the crystal monitor used during evaporation and agreed within 10%. Figure 5 shows the total diffusion depth obtained into the InGaAs for the various metals after annealing at 300°C/30 min. The RBS data agreed well with the TLM data. Alloys G, H, I, and J did not diffuse far enough to penetrate the 140Å graded quaternary layers to make a low resistance ohmic contact to the p^+InGaAs base region. Alloys B and K diffused too far, more than 500Å, and made contact to the collector region. The RBS data is not accurate enough to differentiate between alloys A and C. However, the TLM data indicates that alloy A has penetrated into the collector region, and alloy C has not. For alloys A and B, the Au top layer has most likely penetrated the Pt barrier layer and spiked through to the collector region. Thus, the 200Å Pt layer was not enough of a diffusion barrier to the Au. Alloy C, with a 350Å Pt barrier, did not contact the collector region. Interestingly, for the Pd/Pt alloys, the two metals were always found at the same depth after annealing, so there may be some interaction between them.

An alloy of Pd/Pt/Au was the best choice for the base electrode. The lowest Rc obtained for this alloy was in the low $10^{-7}\Omega cm^2$ range. The diffusion depth for this alloy system goes through a minimum around 25 to 50Å of Pd, and then starts to increase. This is most likely due to competing alloys formed with the Pd, Pt, and InGaAsP system. At 300°C, there are several alloys formed between the Pd, Pt, and InGaAsP, such as $PtAs_2$, PtGa, PtIn, PtP_2, $Pd_5(InP)_2$, and $Pd_5(GaAs)_2$.[2,5] If there is sufficient Pd to alloy with the Pt, the Pt alloys may be avoided, resulting in a smoother diffusion profile. As noted from the RBS data, the Pd and Pt were always found at the same depth after anneal-

Table I. Base Contact Metals Evaluated

Sample	Metal Schemes (Thickness in Å)
A	100Pd/200Pt/1000Au
B	50Pd/200Pt/1000Au
C	50Pd/350Pt/1000Au
D	50Pd/500Pt/1000Au
E	25Pd/500Pt/1000Au
F	10Pd/500Pt/ 1000Au
G	65Pd/500Ti/500Pt/500Au
H	50Pd/500Ti/500Pt/500Au
I	25Pd/25Pt/500Ti/500Pt/500Au
J	50Ti/500Pt/1000Au
K	50AuBe(10%)/500Pt/1000Au

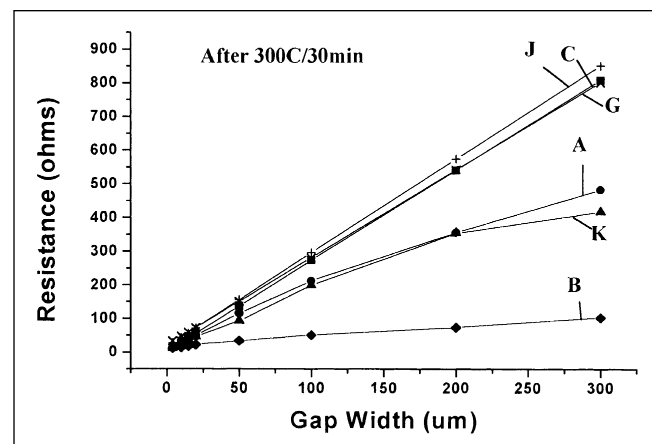

Fig. 3. Transmission line measurements for several metallization schemes on the base.

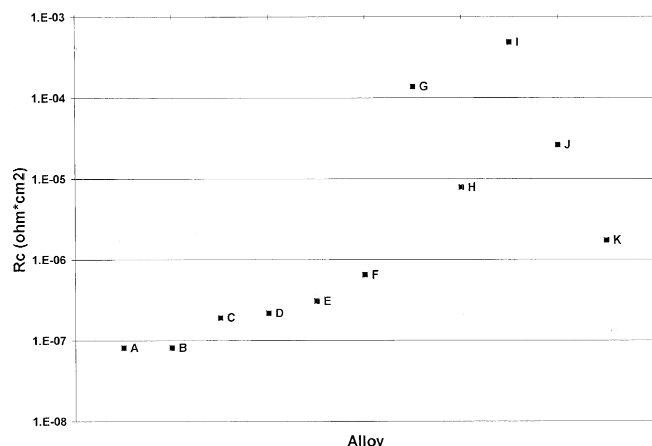

Fig. 4. Contact resistance obtained for the base metals in listed in Table I, after 300°C anneal.

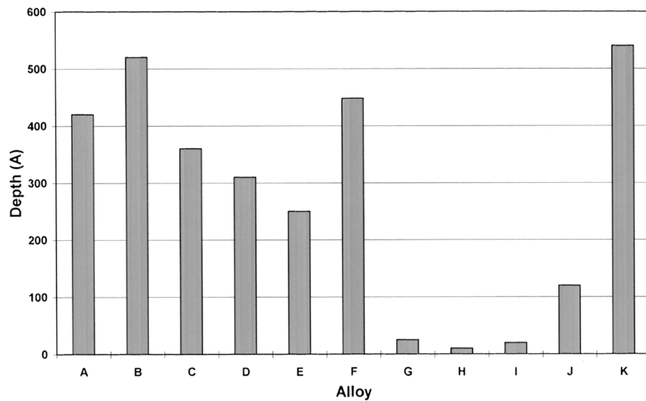

Fig. 5. Metal diffusion depth after 300°C/30 min anneal, determined using RBS.

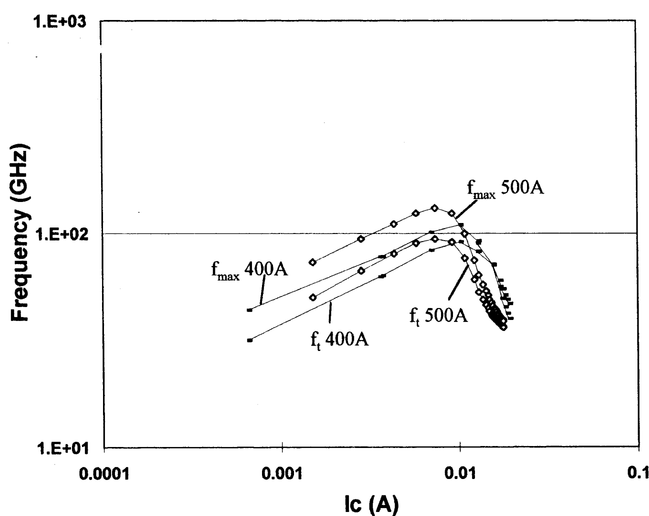

Fig. 6. Microwave characteristics for DHBT devices fabricated with thin base regions.

ing. Finally, thick Pt, at least 350Å, was a sufficient diffusion barrier metal to the Au top layer.

Several DHBT structures with a base thickness of 200 to 500Å were evaluated with the optimum base electrode. TLM test patterns on the base region and large-area devices were fabricated and measured both before and after annealing. The 400 and 500Å base DHBTs were fabricated using 50Pd/500Pt/1000Au base electrodes. The 200 and 300Å base DHBTs were fabricated with 50Pd/500Ti/500Pt/500Au electrodes, since the diffusion depth for this alloy should be fairly shallow. Table II shows the dc gain and base Rs obtained for these structures. Small devices were then fabricated. Figure 6 shows the microwave data for the 400 and 500Å base DHBTs, peak f_t = 89 and f_{max} = 109, and f_t = 91, and f_{max} = 131 GHz were obtained, respectively, at a V_{CE} of 2V. Devices with a 500Å base region were stressed at an emitter current density of 90kA/cm^2 and a collector bias, V_{CE}, of 2V at room temperature for over 500 h and

Table II. Current Gain and Rs for Thin Base DHBTs

Thick. (Å)	Gain	Rs (Ω/□)
200	1100	1950
300	500	1160
400	200	700
500	120	500

show no degradation in dc characteristics. Unfortunately, the small devices with 200 and 300Å base DHBTs of did not perform well, since the base Rc was rather high, around $8 \times 10^{-6}\Omega cm^2$.

CONCLUSION

We have optimized the base contact metal for InGaAs/InP based DHBTs with buried emitter-base junctions. The base metal is diffused through a thin graded quaternary region, which is doped lightly n-type, to make ohmic contact to the base region without diffusing into the collector region. Several base metal schemes were evaluated, in terms of diffusion depth into the semiconductor after annealing and minimum contact resistance. An alloy of Pd/Pt/Au produced the lowest Rc. The Pd diffusion depth was easily controlled by using a thickness of 25 to 50Å, and using sufficient Pt, at least 350Å, as a barrier metal to the top layer of Au. Devices with a 500Å base region show no degradation in dc characteristics after operation at an emitter current density of 90kA/cm^2 and a collector bias, V_{CE}, of 2V at room temperature for over 500 h. Typical common emitter current gain was 120. f_t of 95 and f_{max}, of 131 GHz were achieved for 2×4 μm^2 emitter size devices.

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