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ORIGINAL RESEARCH ARTICLE

Analysis of Negative Capacitance Source Pocket Double-Gate TFET with Steep Subthreshold and High ON–OFF Ratio

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Abstract

This article presents a study on the subthreshold swing (SS) and the ON–OFF current ratio of a negative capacitance source pocket double-gate tunnel field-effect transistor (NC-SP-DGTFET). In this analysis, a novel device is developed that integrates gate and channel engineering techniques. The combination of the ferroelectric material hafnium zirconium oxide (HZO) with the dielectric material SiO_2 generates a negative capacitance (NC) effect. Additionally, the incorporation of a totally depleted source pocket into the DGTFET reduces the tunneling width. The addition of NC has the potential to improve the SS through the amplification of the electric field at the tunnel junction. Moreover, it has been observed that a fully depleted source pocket within the source/channel region significantly enhances the I_{ON} current when compared to the double-gate tunnel field-effect transistor (DGTFET). Following thorough device optimization, there has been a notable enhancement in the I_{ON}/I_{OFF} current ratio, SS, and transconductance (g_m) by a factor of 1.54×10^{13}, 20.8 mV/dec, and 5.102×10^{-4} S/μm, respectively. These improvements signify superior energy efficiency and enhanced performance when compared to both DGTFET and source pocket based DGTFET (SP-DGTFET) configurations. Furthermore, substantial research has been conducted on the variation in electrical properties in relation to the thickness of ferroelectric materials. The findings indicate that the proposed device exhibits considerable potential as a viable option for applications requiring both low power consumption and high operational speed.

Keywords DC performance · ferroelectric material · negative capacitance · source pocket · subthreshold swing · tunneling width

Introduction

The scaling of metal–oxide–semiconductor field-effect transistor (MOSFET) devices has been driven by the growing demand for smaller and more efficient integrated circuits (ICs) due to advancements in technology.[1] The enhancement of switching speed and MOSFET density in an IC leads to a diminution in device performance as a result of short-channel effects (SCEs).[2–4] These SCEs include drain-induced barrier lowering (DIBL), threshold voltage roll-off, subthreshold leakage current, subthreshold swing (SS), punch through, and hot carrier effect. The tunnel field-effect transistor (TFET) is emerging as a highly promising and energy-efficient alternative to conventional MOSFETs for low-power applications.[5–7] The band-to-band tunneling (BTBT) mechanism[8] has become increasingly popular because of its advantageous characteristics, including minimal OFF-state leakage current, an SS value of less than 60 mV/decade at ambient temperature,[9] and reduced SCEs. Nevertheless, it is important to acknowledge that there are several limits associated with TFET design. One of the primary challenges faced by TFET designers is the relatively low on-state current. Furthermore, it has been observed that TFETs exhibit ambipolar behavior.[10] By incorporating the tunneling width and barrier engineering techniques, the ON current can be increased in TFETs. Barrier height may decrease by using III–V material compounds, whereas barrier width can increase by integrating pocket doping engineering in multi-gate TFET structures. The double-gate structure is highly effective in mitigating SCEs due to its superior gate control and drain current characteristics. To enhance the ON-state current of the device, it is necessary to introduce a pocket at the source/

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channel junction.[11] Simultaneously, it should be noted that the asymmetry of the device suppresses ambipolar conduction, which distinguishes it from conventional TFET architectures.[12] Further, to enhance the device characteristics a ferroelectric (FE) layer[13] is added to the TFET structure. The FE layer has shown an internal voltage amplification with steeper subthreshold characteristics and improved I_{ON}/I_{OFF} ratio without necessitating any alterations to the fundamental physics of the transistor.[14] The study conducted by Guha et al.[15] examined a TFET including a heterojunction negative capacitance. It was observed that the utilization of this technology was feasible in inverters, ring oscillators, and entire adder circuits, with an SS of 27 mV/dec. Singh et al.[16] introduced a source overlapped negative capacitance tunnel field-effect transistor (NCTFET). The SS was measured to be 34.7 mV/dec, while the ON current was determined to be 1.45 µA/µm. In their study, Kim and Kwon[17] conducted an analysis on an NCTFET with channel engineering where the tunneling direction is normal to the gate. By refining the doping concentration in the channel the SS is improved by 43.9 mV/decade and the ON current is increased by 3.5 times as compared with that of the conventional TFET. The utilization of an FE layer represents a feasible alternative for enhancing the device's characteristics, resulting in improved performance characterized by reduced power consumption and enhanced switching speed. In order to enhance the drain current and SS of TFETs,[18] an FE insulator layer is integrated within the gate stack. In this particular scenario, the TFETs hold the negative capacitance (NC) property exhibited by FE materials in order to enhance the ON current.[19] Consequently, the width of tunneling will decrease as a result of the amplified band bending, and a narrower tunneling width leads to an increased probability of tunneling with higher ON current. The studies published in the literature have looked at the gate-length-dependent SCEs of the double-gate tunnel field-effect transistor (DGTFETs) with different channel engineering techniques.[20,21] However, to the best of our knowledge, there is no existing literature on DGTFETs utilizing the NC as a gate stack along with the source pocket (SP) as a channel engineering technique. The remaining part of this paper is organized as follows: The proposed device parameters, along with the simulation models, are described in the "Device Simulation Setup and Models" section. The results and discussions are discussed in the "Results and Discussion" section, and the conclusions are drawn in the final section.

Device Simulation Setup and Models

Figure 1 depicts a schematic illustration of an NC-SP-DGTFET. The source and drain are asymmetrically doped with doping concentrations of 1×10^{20} cm^{-3} and 1×10^{18} cm^{-3}, respectively. The proposed device has a silicon channel with a length of 25 nm and it is doped with acceptor concentration of 1×10^{15} cm^{-3}. The thickness of the gate oxide (T_{OX}) is 1 nm, while the active silicon body (T_{Si}) has a thickness of 10 nm.[22–24] The decrease in channel length has minimal impact on the tunneling current due to the dominant influence of the electric field and band configuration in the vicinity of the tunneling junction on the drain current. The optimization of the I_{ON}/I_{OFF} ratio is achieved through the incorporation of a source-side *n*-type pocket layer with a high doping concentration of 1×10^{19} cm^{-3} and a pocket length (L_P) of 3 nm.

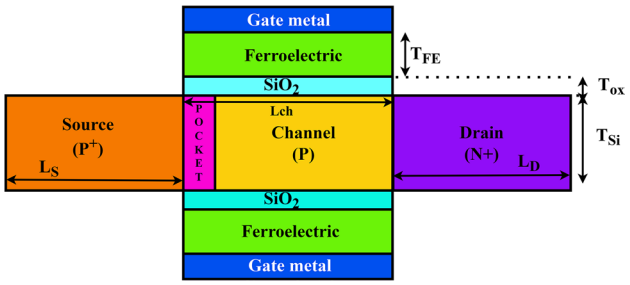

Fig. 1 Schematic cross-sectional view of an NC-SP-DGTFET.

The fabrication process for the proposed NC-SP-DGTFET closely resembles that of conventional double-gate MOSFETs,[25] as illustrated in Fig. 2. Initially, precise mask patterning and selection of photoresist facilitate the creation of p-type source, n-type drain, and channel regions on a silicon wafer via ion-implantation. An n-type pocket at the source/channel junction is introduced through an in-situ doping process. Subsequently, a SiO_2 layer is grown utilizing chemical vapor deposition (CVD), followed by the deposition of FE material via atomic layer deposition (ALD). Finally, appropriate gate metals are deposited to complete the fabrication process.

Numerical simulations were performed with the Sentaurus TCAD (technology computer-aided design) simulator[26] using the nonlocal BTBT model to include tunneling of electrons from source to drain. Generation and recombination models were used to include the charge carrier effects, and Fermi–Dirac statistics and bandgap narrowing models were activated for highly doped source and drain regions. The TCAD simulation models were meticulously calibrated with experimental data, as demonstrated by Biswas et al.[8] and shown in Fig. 3, where the BTBT model tunneling mass has been tuned as $0.037\times m_0$ and the tunneling constants are calculated as $A = 2.84\times10^{14}$ and $B = 1.73\times10^{7}$. Notably, the simulation results closely align with the experimental findings, indicating a strong agreement between the two.

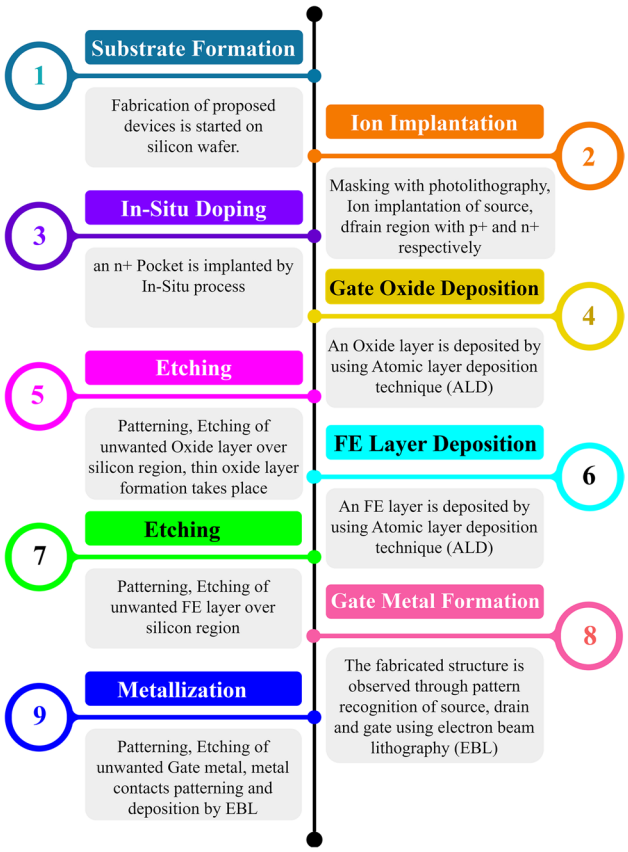

Fig. 2 Fabrication process of the proposed device.

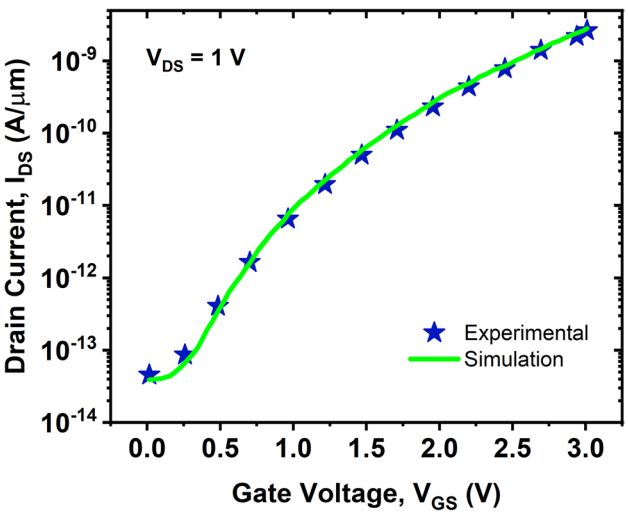

Fig. 3 Calibration of simulation model with the reported data (Ref. 8).

Existence of Negative Capacitance in Proposed Device

The use of NC[27] in the gate oxide stack of TFETs can enhance drain current and SS. The use of FE material in its NC mode leads to an increase in the surface potential and an enhancement of the electric field in TFETs. Negative capacitance may be seen when an FE capacitor is connected in series with a normal capacitor in metal–ferroelectric–insulator–semiconductor (MFIS) and metal–ferroelectric–metal–insulator–semiconductor (MFMIS) configurations. The MFMIS exhibits an increased leakage current under equivalent applied voltages, largely influenced by the presence of an internal electrode. This electrode leads to polarization screening and destabilizes the NC effect. Conversely, the absence of such an electrode in the MFIS structure reduces the leakage current, minimizes charge exchange between domains, mitigates polarization compensation, and consequently diminishes hysteresis behavior.[28] However, in the MFIS configuration, the NC effect is observed across a broader range of electric field and polarization. This broader range facilitates the provision of differential bias amplification within the necessary bias range for achieving the desired transfer characteristics of conventional FETs. Additionally, the FE parameters utilized in this study are derived from MFIS capacitor characteristics, rather than the polarization-electric field (PE) loop of the metal-ferroelectric-metal (MFM) configuration. These extracted FE parameters are experimentally obtainable and suitable for MFIS NC-SP-DGTFET implementation.

Ferroelectric materials like barium titanate ($BaTiO_3$) and lead zirconate titanate (PZT) have long been utilized for their NC effect. However, their compatibility issues with CMOS fabrication and limited scalability pose challenges.[29,30] Recently, doped hafnium oxide (HfO_2) has emerged as a promising alternative, boasting strong FE properties. Doped HfO_2, especially Zr-doped HfO_2 (HZO), offers significant advantages over traditional perovskites, such as excellent scalability and seamless integration with CMOS processes.[31] Additionally, HZO requires low annealing temperatures, further enhancing its appeal for advanced electronic applications. When comparing with PZT, HZO exhibits, we see a more pronounced NC effect, resulting in a higher electrical potential for thinner FE layers. The MFIS[32] structure exhibits a stable state in total energy when a gate bias is applied, resulting in negative curvature in the Landau energy of the FE. The analytical description of the polarization charge density and electric field in a FE film is provided by the Landau equation. The NC-SP-DGTFET is simulated by activating the Landau–Khalatnikov (LK model) model[33] to represent the polarization behavior of the FE material, and the poisons equation are calculated. The device parameters used for the simulation are shown in Table I.

The electric field of an FE material is given by the LK equation (Eq. 1)

Table I Simulation parameters of the proposed device

Parameter	Value
Body thickness (T_{si})	10 nm
Oxide thickness (T_{ox})	1 nm
Pocket length (L_p)	3 nm
Channel length (L_{ch})	25 nm
Source doping (N_s)	1×10^{20} cm^{-3}
Drain doping (N_d)	1×10^{18} cm^{-3}
Channel doping (N_{ch})	1×10^{16} cm^{-3}
Pocket doping (N_p)	1×10^{19} cm^{-3}
Ferroelectric thickness (T_{FE})	4 nm
Coercive field (E_c)	1MV/cm
Remanent polarization (P_r)	11.1 C/cm^2
α	-1.35×10^{11} cm/F
β	5.50×10^{20} cm^5/FC^2
γ	0

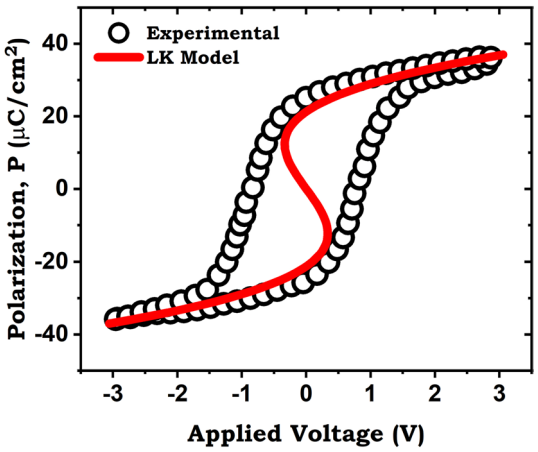

Fig. 4 Calibration of LK model with the experimental data (Ref. 34).

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5, \quad (1)$$

where α, β and γ are Landau parameters. According to the Landau–Khalatnikov equation, the relationship between FE polarization and electric field properties exhibits an area with an unstable negative slope ($dP/dE<0$), as depicted in Fig. 4. This instability in FE materials can be mitigated in a heterogeneous system, such as a ferroelectric-dielectric (FE-DE) stack, where polarization suppression ($P=0$) can be achieved by minimizing depolarization energy. To achieve this, the LK model is calibrated with the fabricated TIN/HZO/TIN capacitor[34] as illustrated in Fig. 4. The parameters of HZO material $\alpha=-1.35\times10^{-11}$ cm/F, $\beta=5.509\times10^{20}$ cm^5/FC^2 and $\gamma=0$ cm^9/FC^4 are extracted with corresponding coercive filed (E_C) 1 MV/cm and remanent polarization (P_r) 11.1 C/cm^2.

Results and Discussion

Energy profiles of NC-SP-DGTFET, SP-DGTFET and DGTFET are shown in Fig. 5a and b for the OFF and ON states, respectively. It is noticed that at $V_{GS}=0$ V, the tunneling probability from the source's valence band to the channel's conduction band is virtually insignificant due to the greater tunneling barrier width at the source-channel junction. In the ON state ($V_{GS}=1$ V), the gate voltage lowers the channel's conduction band below the source's valence band, allowing electrons to tunnel from source to channel and record a BTBT current. The tunneling width of the NC-SP-DGTFET is very small compared to SP-DGTFET and DGTFET due to the presence of pocket and FE material as gate dielectric. In the ON state (i.e at $V_{GS}=1$ V) of the NC-SP-DGTFET, polarization gets induced in the FE material, which results in the reduction in gate capacitance value. This amplifies the voltage across the gate oxide, leading to an enhancement in the electric field of the channel region and promoting BTBT.

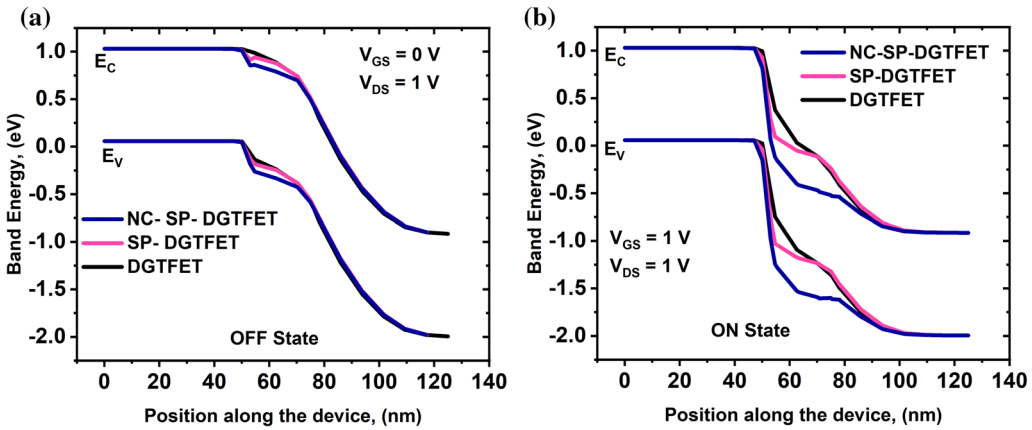

Fig. 5 Energy band diagram of the NC-SP-DGTFET, SP-DGTFET, and DGTFET in (a) OFF state (b) ON state.

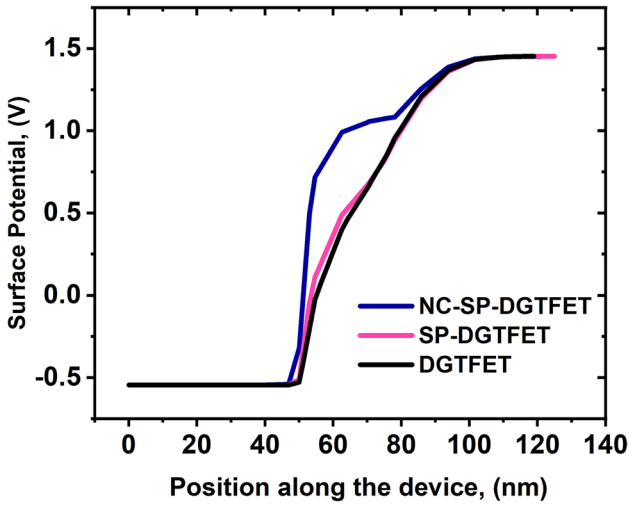

Fig. 6 The surface potential of NC-SP-DGTFET, SP-DGTFET and DGTFET.

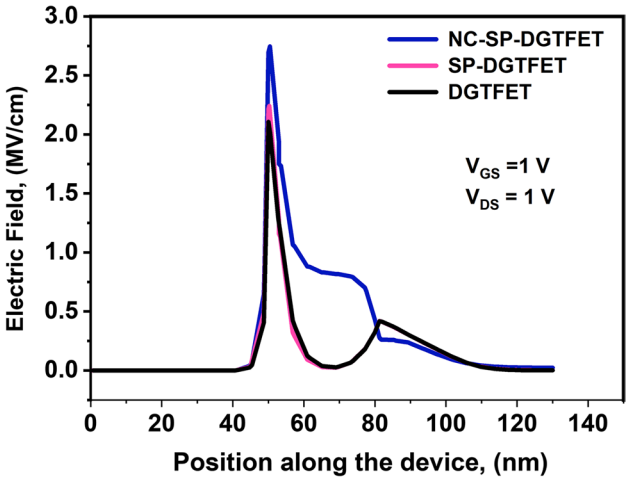

Fig. 7 Electric field of conventional and proposed devices.

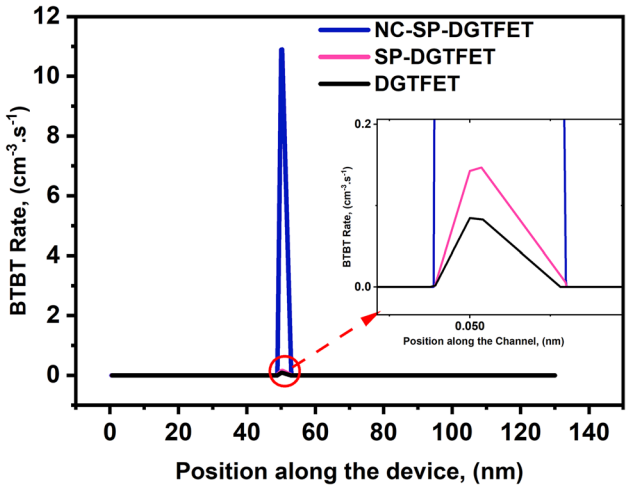

Fig. 8 BTBT rate of conventional and proposed devices.

Further, the amplification effectively reduces the tunneling barrier width, facilitating electron tunneling from the source to the channel. Additionally, integrating a n^+ pocket near source/channel region reduces the energy barrier height, causes increase in carrier concentration and enhances tunneling probability, which leads to higher ON-state current and improved device performance.

A comparison of the surface potential of the NC-SP-DGTFET, SP-DGTFET, and DGTFET is shown in Fig. 6. The surface potential is increased for the proposed device as compared to the SP-DGTFET and DGTFET owing to the existence of the NC effect attributable to the FE material. The NC leads to an internal voltage amplification and an enhancement of the electric field in the proposed device.

In addition, a comparison of the electric fields produced by the three distinct devices, NC-SP-DGTFET, SP-DGTFET, and DGTFET, is shown in Fig. 7. The proposed structure has the largest spike at the channel/source contact, indicating the greatest amount of tunneling of carriers. It is possible that the NC material utilized as the gate stack in the proposed device is responsible for the largest spike. The total gate capacitance will be increased beyond its standard value by incorporating NC material in the gate stack, resulting in a lower gate voltage being needed to achieve the same surface potential. As a result, the proposed device has a greater electric field.

Figure 8 shows the BTBT rate for the proposed device as a function of channel location. The tunneling width has a significant impact on the BTBT rate. When compared to a DGTFET, SP-DGTFET, the tunneling width of the NC-SP-DGTFET is much smaller. As a result, the electrons will tunnel very rapidly from source valance band to channel conduction band, which increases the BTBT rate.

DC Analysis

Figure 9 shows a comparison of the I_{DS}–V_{GS} characteristics of the three different structures (NC-SP-DGTFET, SP-DGTFET, and DGTFET). The effect of NC caused by the FE material is supported by the fact that NC-SP-DGTFET generates lower OFF current than the other two configurations. When comparing the NC-SP-DGTFET to the other two designs, a considerable drop in V_{th} is shown, along with an improvement in I_{ON} because of the higher drain current caused by the voltage amplification due to NC effect in the FE material used as a gate stack. SS and I_{ON}/I_{OFF} ratio are both significantly enhanced in the NC-SP-DGTFET, which significantly influences the device performance. As can be seen in Fig. 10, the NC-SP-DGTFET has an impressive I_{ON}/I_{OFF} ratio of 10^{13} while maintaining an SS of 20.8 mV/decade, while DGTFET and SP-DGTFET

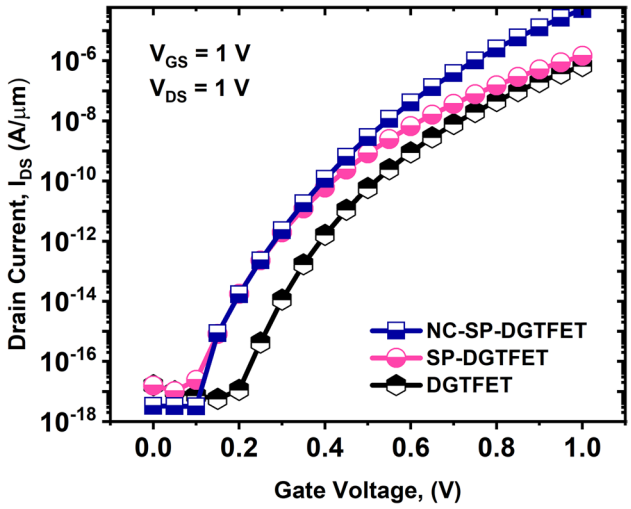

Fig. 9 I_{DS}–V_{GS} characteristics of conventional and proposed devices.

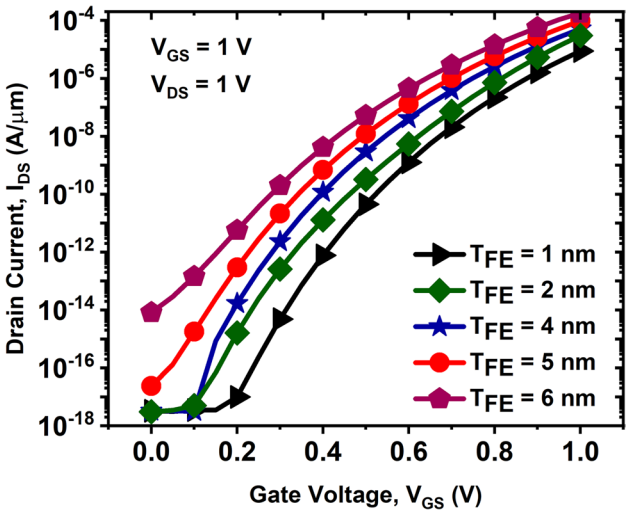

Fig. 11 I_{DS}–V_{GS} characteristics with various ferroelectric thickness (T_{FE}).

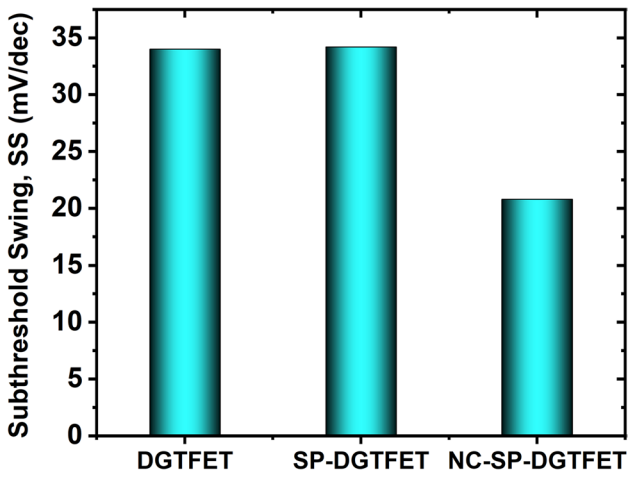

Fig. 10 Subthreshold swing for conventional and proposed devices.

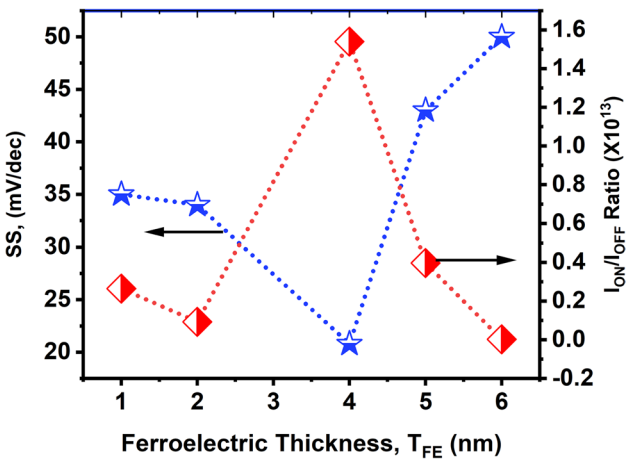

Fig. 12 Subthreshold swing and I_{ON}/I_{OFF} ratio of NC-SP-DGTFET at various T_{FE}.

have I_{ON}/I_{OFF} ratio and SS values of 4.17×10^{10}, 0.622×10^{11}, 34 mV/dec and 35 mV/dec, respectively.

Impact of Ferroelectric Thickness on Proposed Device

A large quantity of polarized charge with the smallest feasible T_{FE} is needed to increase the device's ON current. Because of the NC effect, the device's positive capacitance (baseline device capacitance, $C_{device}>0$) becomes smaller by increasing the gate capacitance, which is the inverse of the FE's differential capacitance (C_{FE}).

$$C_T = \left\{ \left(C_{FE}\right)^{-1} + \left(C_{device}\right)^{-1} \right\}^{-1}. \quad (2)$$

C_{FE} can be varied by adjusting the FE thickness (T_{FE}) and it should be matched to C_{device} ($|C_{FE}| \geq C_{device}$) to ensure maximal capacitance enhancement. Thus, at optimal T_{FE}, there is a rise in drain current because total gate capacitance (C_T) is maximized. The I_{DS}–V_{GS} curve of the NC-SP-DGTFET is shown in Fig. 11, plotted against varying T_{FE}. As T_{FE} rises, the drain current for NC-SP-DGTFET does as well, and the resulting steepening of the SS can be seen.

When the T_{FE} increases, NC effects come into play, causing the voltage of the underlying SP-DGTFET to surpass the applied gate voltage. Additionally, hysteresis occurs when the FE thickness exceeds a critical value. This critical thickness is the point at which the FE capacitance equals the total gate capacitance connected with the underlying SP-DGFET. Therefore, it's advisable to maintain T_{FE} below

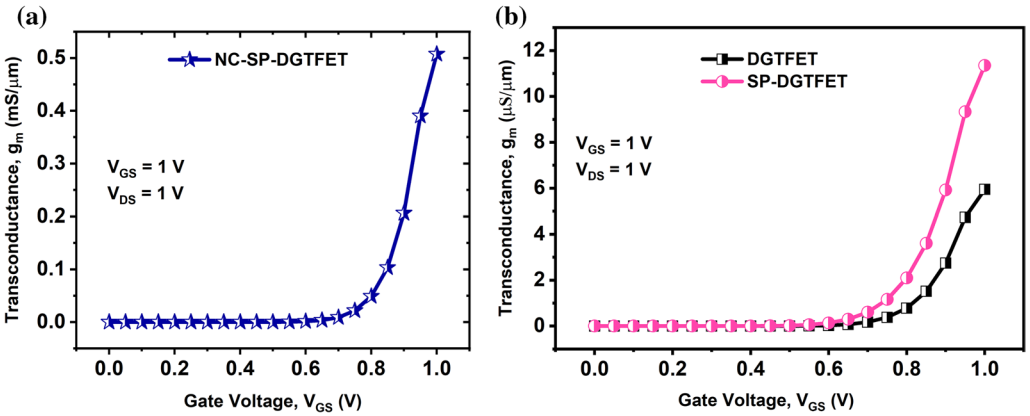

Fig. 13 Transconductance of (a) NC-SP-DGTFET, (b) DGTFET and SP-DGTFET.

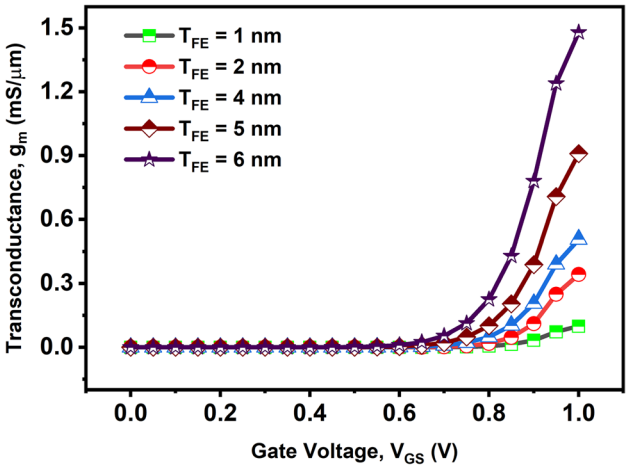

Fig. 14 Transconductance of NC-SP-DGTFET at various T_{FE}.

this critical value. As the thickness increases, the drain current abruptly transitions from the OFF state to the ON state due to improved capacitance matching. This is evident from Fig. 11, which shows that increasing T_{FE} enhances the ON current. It has also been determined that the "4 nm" T_{FE}, where the maximum drain current and steep slope of the device has been attained, is the optimal T_{FE}.

For NC-SP-DGTFET, Fig. 12 plots the SS and I_{ON}/I_{OFF} ratio versus T_{FE} variation. It can be observed that the ratio of I_{ON} to I_{OFF} (I_{ON}/I_{OFF}) reaches its maximum at $T_{FE}=4$ nm. Our device design benefits from the assumption, supported by the increase in I_{ON}/I_{OFF} with T_{FE}, that the effect of NC at I_{OFF} is negligible. For the device to function at low power, the SS is crucial. The device's speed is also determined by SS. Further, SS should be lower to facilitate quicker changeover from the OFF to ON state. Variation in SS versus T_{FE} is shown in Fig. 12. It is clear that with a T_{FE} of 4 nm, SS is 20.8 mV/dec. This means that the surface potential is amplified by including the FE layer as the gate stack, which in turn causes the value of SS to drop below the 60 mV/dec.

Figure 13 depicts the transconductance (g_m) curve as a function of gate voltage with and without the influence of NC. Transconductance is an electrical property related to both the output current and the input voltage.

Increasing the current results in a higher transconductance, revealing the device's gain, since transconductance is proportional to current. From Fig. 13a, the g_m of the NC-SP-DGTFET is 5.102×10^{-4} S/μm, which is much higher than the g_m of SP-DGTFET (1.13×10^{-5} S/μm) and DGTFET (5.94×10^{-6} S/μm) as shown in Fig. 13b. The variation in transconductance versus gate voltage with different T_{FE} is depicted in Fig. 14. The gain of the MOSFET is directly proportional to g_m.[35] From Fig. 14, it can be visualized that the increase in gate voltage improves the transconductance, further leading to higher gain. Since the proposed NC-SP-DGTFET is optimized at $T_{FE}=4$ nm, the g_m is also noticed maximum at the same T_{FE} as shown in Fig. 14.

A comparison of the obtained results with those available in the existing literature is illustrated in Table II. It is observed that the proposed device demonstrates superior performance over the other devices, which indicates that the proposed device is a promising candidate for high-speed applications.

Conclusion

This work analyses three tunnel field-effect transistor (TFET) structures: DGTFET, SP-DGTFET, and NC-SP-DGTFET. The I_{ON}/I_{OFF} and SS are improved in NC-SP-DGTFET as compared with SP-DGTFET and DGTFET by 96%, 99% and 64%, 63% respectively. These enhancements are noticed due to the incorporation of SP and FE material in DGTFET. The pocket at the junction of the source and

Table II Comparison of device characteristics of NC-SP-DGTFET with existing literature

Reference	I_{ON} (A/μm)	I_{ON}/I_{OFF}	SS (mV/decade)
36	5.1×10^{-6}	3.033×10^{7}	43
37	1.4×10^{-5}	0.81×10^{10}	36.1
38	18×10^{-6}	10^{6}	34
39	2.3×10^{-6}	4.5×10^{11}	32
This work	5.03×10^{-5}	1.54×10^{13}	20.8

channel has been used to enhance the ON current as well as the FE material exhibits the improved electric field within the channel. The impact of varying the thickness of the FE material on the transfer characteristics, g_m, and SS are also examined. The proposed device has lower SS, higher g_m and better I_{ON}/I_{OFF} ratio at $T_{FE}=4$ nm, rendering it an optimal selection for applications that prioritize both high speed and low power consumption.

Conflict of interest The authors declare that they have no conflict of interest.

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