Journal of Electronic Materials (2024) 53:2562–2572
https://doi.org/10.1007/s11664-024-10987-0

ORIGINAL RESEARCH ARTICLE

Investigation of Double RESURF P-GaN Gate AlGaN/GaN Heterostructure Field-Effect Transistors with Partial N-GaN Channels

Huan Li[1] · Zhiyuan Bai[1,2] · Lian Yang[1]

Received: 25 October 2023 / Accepted: 7 February 2024 / Published online: 14 March 2024

Abstract

In this paper, a double REduced SURface Field (RESURF) P-GaN gate AlGaN/GaN heterostructure field-effect transistor with a partial N-GaN channel (DR-HFET) is proposed to improve the on-state performance in the high-voltage P-GaN gate AlGaN/GaN heterostructure field-effect transistor (PG-HFET). The partial N-GaN channel between the gate and the drain increases the carrier density in the channel layer, and markedly reduces the on-resistance (R_{on}). The P-top layer and the P-buffer layer modulate the distribution of the electric field along the GaN channel to achieve a high breakdown voltage. After validation of the simulation models and parameters, the DR-HFETs are optimized using the charge balance principle. The optimum DR-HFET with a gate-to-drain distance of $L_{gd}=6$ µm shows a BV of 1100 V and R_{on} of 5.5 Ω mm, which is 50.9% of the R_{on} in PG-HFET. The highest Baliga figure of merit (BFOM) of 2.3 GW/cm^2 is obtained when the channel charge density Q_{ch} is 3.2×10^{13} cm^{-2} and the ratio of the P-top charge density Q_{pt} to the buffer charge density Q_{buf} is 1.625. We also examine the influence of the AlGaN/GaN quality on the performance of the DR-HFETs. The simulation results indicate that the double RESURF structure may be less effective in the high-quality AlGaN/GaN epitaxial layer. Overall, the DR-HFET shows a good balance between off-state blocking capability and on-state performance.

Keywords AlGaN/GaN · heterostructure field-effect transistors · normally off · double RESURF · low on-resistance

Introduction

In recent years, AlGaN/GaN heterostructure-based power devices have attracted considerable attention due to the wide band gap and high critical field of GaN,[1] its high electron mobility in the two-dimensional electron gas (2DEG) channel,[2–4] and the low-cost fabrication of III-N epitaxy on silicon substrate.[5] Therefore, AlGaN/GaN heterostructure field-effect transistors (HFETs) can operate at a high switching frequency (>1 MHz),[6] to reduce the volume of energy storage devices such as inductors and capacitors,[7,8] and miniaturize the power supply modules.[9] AlGaN/GaN HFETs are already widely used in power supplies, electric vehicles, and fast chargers in consumer electronics.[10–12] The P-GaN gate AlGaN/GaN HFET (PG-HFET) is a typical commercial GaN power device, which can realize enhanced-mode operation by a simple and controllable fabrication process.[8] However, PG-HFETs often suffer from the concentration of the electric field (E-field) at the gate edge, which may cause a premature breakdown.[13]

Many recent research efforts have focused on improving the breakdown voltage (BV) of the PG-HFET using various approaches, including metal field plates,[14,15] junction or P-type field plates,[16] stripe array gates, and[17] alternate-island drains.[18] All these methods can smooth the E-field distribution along the channel and significantly improve the BV. However, these device structures often have a long drift region between the gate and the drain to withstand high voltages, resulting in relatively high on-resistance (R_{on}). Therefore, improving the on-state performance of the high-voltage PG-HFET is essential.

The double REduced SURface Field (RESURF) structure is a widely used technology in high-voltage lateral diffusion metal–oxide–semiconductor field-effect transistors (LDMOSFET).[19] The double RESURF structure has a lateral N drift region that defines the R_{on} of the device and a vertical PNP structure which supports a space-charge

✉ Zhiyuan Bai
baizhy321@126.com

1 School of Information and Communication Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China

2 Southwest Minzu University, Chengdu 610225, China

depletion region enabling high breakdown voltage.[20] Compared to the single RESURF structure with a vertical PN junction, the double RESURF structure with a more highly doped N-drift region shows lower on-resistance under the same breakdown voltage.

In this work, we propose a double RESURF P-GaN gate AlGaN/GaN HFET with a partial N-GaN (DR-HFET) channel to improve the BV and the R_{on} of the PG-HFETs. The partial N-GaN channel between the gate and the drain results in a remarkable reduction in the R_{on} by increasing the electron density in the channel layer. The P-top layer and the P-buffer layer modulate the distribution of the E-field along the N-type GaN channel to achieve a high breakdown voltage. After validation of the simulation models and parameters, the optimum DR-HFET achieves a BV of 1100 V and R_{on} of 5.5 Ω mm, while the PG-HFETs produce a BV of 600 V and R_{on} of 10.8 Ω mm under the same gate-to-drain distance of 6 µm. We then discuss the influence of the AlGaN/GaN quality on the performance of the DR-HFETs. When the quality of the AlGaN/GaN epitaxial layer is improved, the relative reduction of R_{on} decreases from 53% to 40%, and the relative increase in BFOM decreases from 6.1 times to 4.6 times. The simulation results indicate that the double RESURF structure may be less effective in the high-quality AlGaN/GaN epitaxial layer. Finally, we propose a series of fabrication steps for the DR-HFET, in which the fabrication of DR-HFETs may have more steps than that of PG-HFETs.

Device Structures, Simulation Models and Mechanism

Device Structures

The structures of the PG-HFET and the proposed DR-HFET are shown schematically in Fig. 1. The structure parameters of the PG-HFET are consistent with reported results.[21] For vertical epitaxial layers, both structures are composed of a 2.6-µm-thick GaN buffer layer, a 300-nm GaN channel layer, and a 12.5-nm AlGaN barrier layer with 25% Al content. The gate stack is formed by an 80-nm-thick P-type GaN layer with a hole concentration of 1×10^{18} cm^{-3}. The Si_3N_4 passivation layer with a thickness of 500 nm is located on the top of the devices.

For the lateral structure parameters, both HFETs have a source and drain length (L_C) of 1 µm. The gate length (L_G) is set as 0.8 µm. The gate-to-source distance (L_{GS}) and gate-to-drain distance (L_{GD}) of the devices are defined as 0.75 and 6 µm, respectively. As shown in Fig. 1b, the proposed DR-HFETs have a P-AlGaN top layer, a partially doped N-GaN channel layer between the gate and the drain, and a P-type GaN buffer layer to form a double RESURF structure. All the structure parameters are given in Table I.

Simulation Models and Validation

The technology computer-aided design (TCAD) simulation was conducted using the Shockley–Read–Hall (SRH) model to calculate the carrier generation and recombination, and the carrier in the simulated devices obey Fermi–Dirac statistics. The high field mobility and the polarization model of the III-N materials was adopted with default parameter values from the Silvaco ATLAS TCAD tool.[22,23] Acceptor-like traps of 0.59 eV under the conduction band were added into the buffer layer of the PG-HFET with density of 1×10^{16} cm^{-3}.[24]

The Selberherr impact ionization model was used to emulate the breakdown characteristics of the GaN-based electronic devices.[25] The impact ionization coefficients for electrons (α_n) and holes (α_p) are based upon the following expressions.

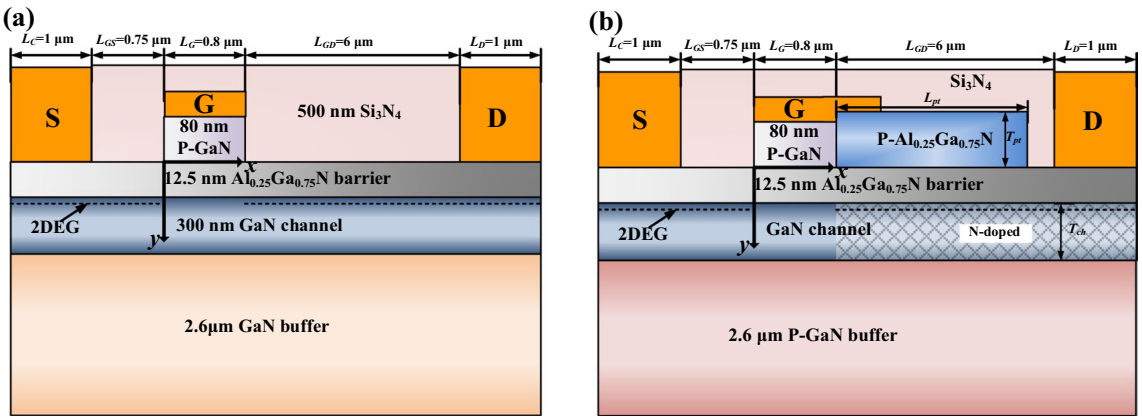

Fig. 1 Device structures of (a) PG-HFETs, (b) DR-HFETs.

Table I Simulated device specifications

Parameters	Values	Parameter captions
L_G	0.8 μm	Gate length
L_{GS}	0.75 μm	Distance from gate to source
L_{GD}	6 μm	Distance from gate to drain
T_{barr}	12.5 nm	Thickness of $Al_{0.25}Ga_{0.75}N$ barrier layer
T_{buf}	2.6 μm	Thickness of GaN buffer layer
T_{GaN}	80 nm	Thickness of P-GaN gate
N_{pGaN}	1×10^{18} cm^{-3}	Density of holes in the P-GaN gate
N_{pt}	$3.6–6.8\times10^{17}$ cm^{-3}	Density of holes in the P-top layer
T_{pt}	500 nm	Thickness of the P-top layer
L_{pt}	1–5.6 μm	Length of the P-top layer
T_{ch}	100–500 nm	Thickness of the channel layer
N_{ch}	$0.01–100\times10^{18}$ cm^{-3}	Density of electrons in the N-GaN channel
N_{buf}	$3.1–9.2\times10^{16}$ cm^{-3}	Density of holes in the buffer layer

$$\alpha_n = a_n \exp\left[-\left(\frac{b_n}{E}\right)^m\right], \tag{1}$$

$$\alpha_p = a_p \exp\left[-\left(\frac{b_p}{E}\right)^m\right], \tag{2}$$

where E is the electric field in the direction of current flow at a particular position in the structure, and a_n, a_p, b_n, b_p, m are parameters. The parameters were set as $a_n = a_p = 1.1438\times10^7$ cm^{-1}, $b_n = b_p = 23.8933$ MV/cm and $m = 1$.[26]

The Lombardi mobility model was conducted as the low field mobility model in the simulation.[27] In the Lombardi mobility model, the electron mobility is limited by the surface acoustic phonon scattering mobility μ_{ac}, doping-dependent bulk carrier mobility μ_b and interface roughness scattering μ_{int}. The total electron mobility μ_n was calculated using Matthiessen's rule.

$$\frac{1}{\mu_n} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{int}}, \tag{3}$$

$$\mu_{ac} = \left(B\frac{T}{E_\perp} + C\frac{1}{E_\perp^{1/3}}\right)\frac{1}{T}, \tag{4}$$

$$\mu_b = \mu_0 + \frac{\mu_{max} - \mu_0}{1 + \left(N/C_r\right)^{\alpha 1}}, \tag{5}$$

$$\mu_{int} = \frac{\delta}{E_\perp^2}, \tag{6}$$

where $E_\perp$ is the transverse field, T is the temperature, μ_{max} is the Hall mobility at room temperature, N is the impurity concentration of the semiconductor, and B, C, μ_0, C_r, $\alpha1$, δ are fitting parameters. The values of μ_0, C_r and μ_{max} are defined based upon other research results.[28–30] We tuned the parameters of B, C, $\alpha1$ and δ to fit the experimental results reported by Li et al.[21]. The parameters used in the Lombardi mobility model are listed in Table II.

Table II Parameters for μ_{ac}, μ_b, and μ_{int} in the mobility model

Parameters	Units	Values
B	cm/s	2.6×10^7
C	K cm/s	3.3×10^2
μ_{max}	cm^2/V s	1600
μ_0	cm^2/V s	100
C_r	cm^{-3}	9.68×10^{16}
$\alpha1$		0.7
δ	V/s	4.6×10^{14}

The validation of our simulation was conducted by comparison of the simulation curve and the experimental data for PG-HFETs reported by Li et al.[21] The validation results are illustrated in Fig. 2. The PG-HFET has a threshold voltage V_{TH} of 1.6 V, a linear area current I_{dlin} of 9.3 mA/mm and a BV of 600 V. The method for calculating R_{on} is to divide the V_{DS} by the I_{dlin} current. During the transfer curves simulation, the V_{DS} was set as 0.1 V, and the R_{on} was obtained as 10.8 Ω mm. These simulation results match the characteristics of the experimental results reported by Li et al.[21] As shown in Fig. 2, the output (Fig. 2a), transfer (Fig. 2b), and off-state (Fig. 2c) characteristics of the PG-HFET are basically consistent with the experimental results.

Device Mechanism

The electron density and band diagram at $x = 4$ μm for the PG-HFETs, the PG-HFETs with only N-GaN channels (NC-HFET) and the DR-HFETs are compared and discussed in

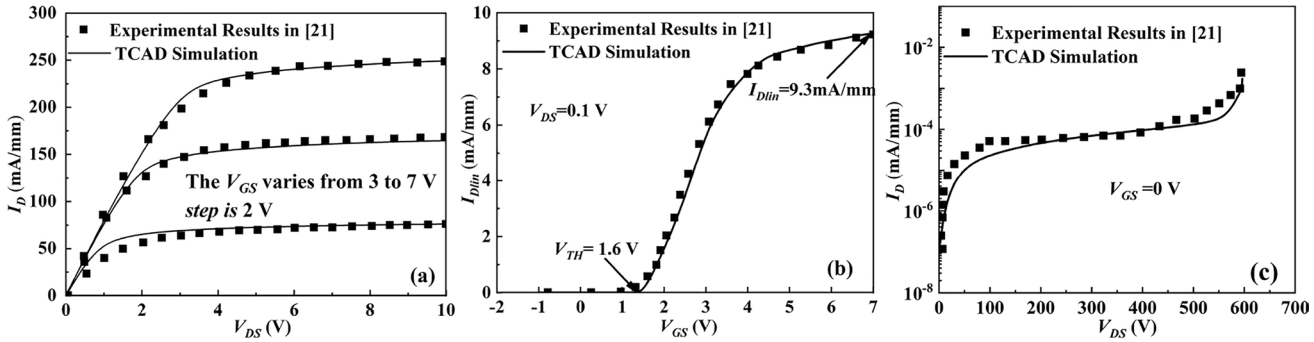

Fig. 2 Simulation validation by comparison of the experimental curves of (a) output (b) transfer (c) off-state characteristics.

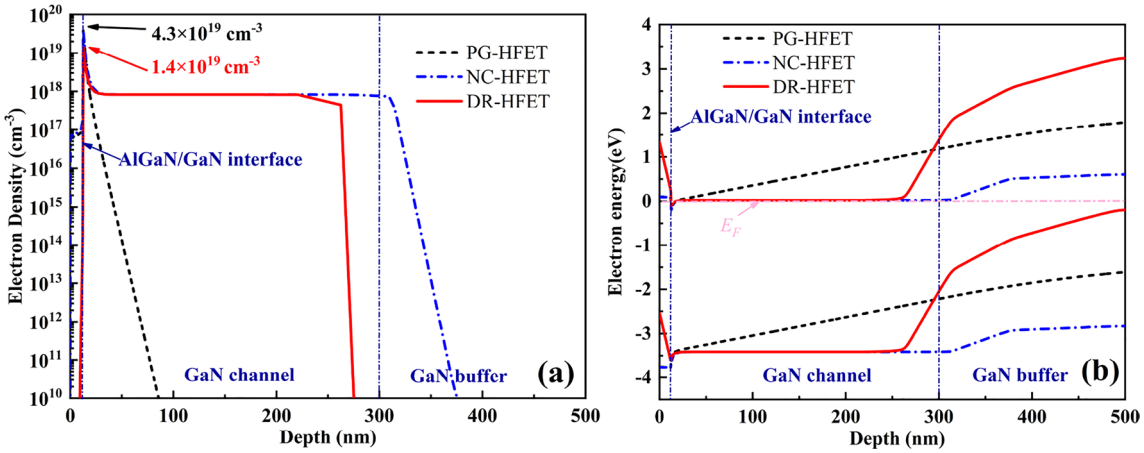

Fig. 3 (a) Electron density and (b) band diagram of the PG-HFET, NC-HFET and DR-HFET with a T_{ch} of 300 nm in thermal equilibrium.

Fig. 3 under thermal equilibrium conditions. As shown in Fig. 3a, the NC-HFET and DR-HFET have partial N-GaN channels with an electron concentration N_{ch} of 8×10^{17} cm^{-3}, which is placed between the gate and the drain; thus the channel electron density in the NC-HFET and DR-HFET become much higher than that of the PG-HFET. For the DR-HFET, the P-top layer induces a decrease in 2DEG density, and the P-buffer layer can extend the depletion region in the channel layer. Therefore, DR-HFETs may have a lower R_{on} than PG-HFET but a higher R_{on} than NC-HFET. In Fig. 3b, it is obvious that the DR-HFETs have the highest electron barrier in the buffer layer due to a concentration of 6.2×10^{16} cm^{-3} acceptors in the P-GaN buffer, and thus DR-HFETs may show low leakage current.

Figure 4 illustrates the results of our in-depth research on the relationship between the structural parameters of the N-GaN channel and R_{on} in the NC-HFETs. When the N_{ch} and the T_{ch} of the N-GaN channel increase, the R_{on} decreases monotonically. When R_{on} is lower than ~ 4 Ω mm, a larger change in N_{ch} or T_{ch} has a relatively smaller impact on the R_{on}, and it is inefficient to reduce R_{on} by increasing the N_{ch} or T_{ch} of the N-GaN channel. Therefore, the benefit threshold

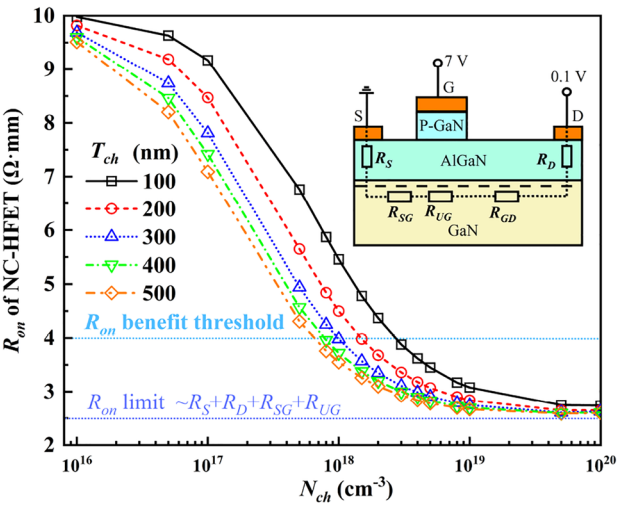

Fig. 4 The T_{ch} and N_{ch} dependence of the R_{on} in the NC-HFET.

of R_{on} is obtained as 4 Ω mm, and we choose T_{ch} = 400 nm, $N_{ch}=8\times10^{17}$ cm^{-3} as the optimum value of the N-GaN channel.

In Fig. 4, the R_{on} of the PG-HFET can be expressed as

$$R_{on} = R_S + R_D + R_{SG} + R_{UG} + R_{GD}, \quad (7)$$

where R_S and R_D are the resistance between the metal contacts and the 2DEG channel, R_{SG} and R_{GD} are the access region resistance, and R_{UG} is the channel resistance under the gate. Although increasing T_{ch} and N_{ch} can reduce the R_{GD}, R_{on} is limited to ~ 2.5 Ω mm, where the sum of R_S, R_D, R_{SG} and R_{UG} become the main part of the R_{on} in the NC-HFETs.

Results and Discussion

Device Characteristics and Optimization

The DC characteristics of the PG-HFETs, NC-HFETs and DR-HFETs are illustrated in Fig. 5. DR-HFETs and PG-HFETs have a T_{ch} of 400 nm, a N_{ch} of 8×10^{17} cm^{-3}. According to the charge balance principle of the RESURF structure, the DR-HFETs are optimized and have a total charge density in P-top layer Q_{tp} of 2.6×10^{13} cm^{-2} ($N_{pt}=5.2\times10^{17}$ cm^{-3}, $T_{pt}=500$ nm), and a total charge density in P-GaN buffer layer Q_{buf} of 1.6×10^{13} cm^{-2} ($N_{buf}=6.2\times10^{16}$ cm^{-3}, $T_{buf}=2.6$ μm).

Facilitated by the high electron density in the N-GaN channel, the NC-HFET and DR-HFET show a higher saturation current I_{dsat} and a lower R_{on} than that of PG-HFET. As shown in Fig. 5a, owing to the electron depletion caused by the P-top and P-buffer layer, a degradation of on-state performance can be observed in the DR-HFET. In Fig. 5b, the R_{on} is extracted by the transfer characteristic at $V_{DS}=0.1$ V. The R_{on} of the NC-HFET is achieved as ~ 4 Ω mm, which is the benefit threshold value mentioned in above section. Then, the DR-HFET have a R_{on} of 5.5 Ω mm, which is 50.9% that of PG-HFET, indicated that double RESURF structure can significantly reduce the R_{on}. As shown in Fig. 5b, the threshold voltage V_{TH} of the PG-HFET and NC-HFET is 1.6 V with non-doped GaN buffers, while the V_{TH} of the DR-HFET becomes 1.7 V due to the P-type doping in the buffer layer.

The off-state breakdown characteristics of PG-HFETs, NC-HFETs and DR-HFETs are compared at $V_{GS}=0$ V in Fig. 6. The BV is extracted when the reverse leakage current reaches 1 μA/mm. The on-state and off-state simulations have identical structural parameters. As shown in Fig. 6a, the DR-HFETs show a BV of 1100 V, while the PG-HFETs have a BV of 600 V. Compared to the PG-HFETs and NC-HFETs, the DR-HFETs display reverse leakage current of ~ 10^{-6} mA/mm at $V_{DS}=600$ V, which indicates that the P-GaN buffer can effectively suppress the leakage currents. The E-field distribution along the channel at $y=13$ nm is shown in Fig. 6b. When breakdown occurs, all devices have the maximum E-field strength of ~ 3.4 MV/cm. It is clearly shown that the E-field distribution of the DR-HFET spread more uniformly than that of the PG-HFETs and the NC-HFETs; thus, the DR-HFETs have the highest BV of 1100 V among all three kinds of HFETs.

The potential distributions of PG-HFET and the proposed DR-HFET at $V_{DS}=600$ V are shown in Fig. 7. For the PG-HFET in Fig. 7a, the potential contours are closely packed at the gate edge due to the incomplete depletion of the gate-to-drain access region, which suggests the crowding of the electric field lines at the gate edge. As shown in Fig. 7b, the potential distribution of the DR-HFETs is more uniform than that of the PG-HFETs. It can be observed that the potential contours are relatively concentrated at the gate edge and the P-top edge. Therefore, two electric field peaks at these edges can also be found in the E-field distribution of the DR-HFETs in Fig. 6b.

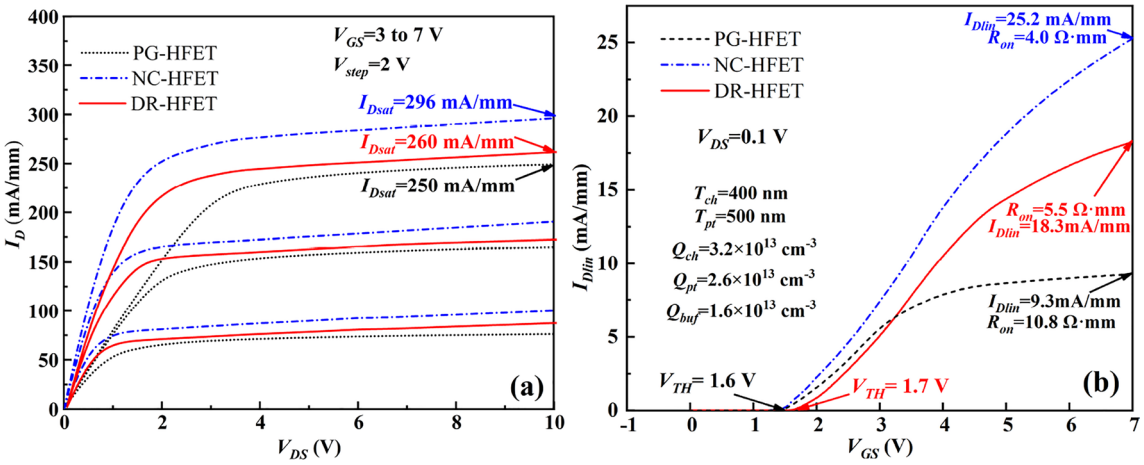

Fig. 5 The DC characteristics of PG-HFETs, NC-HFETs and DR-HFETs: (a) output curves, (b) transfer curves.

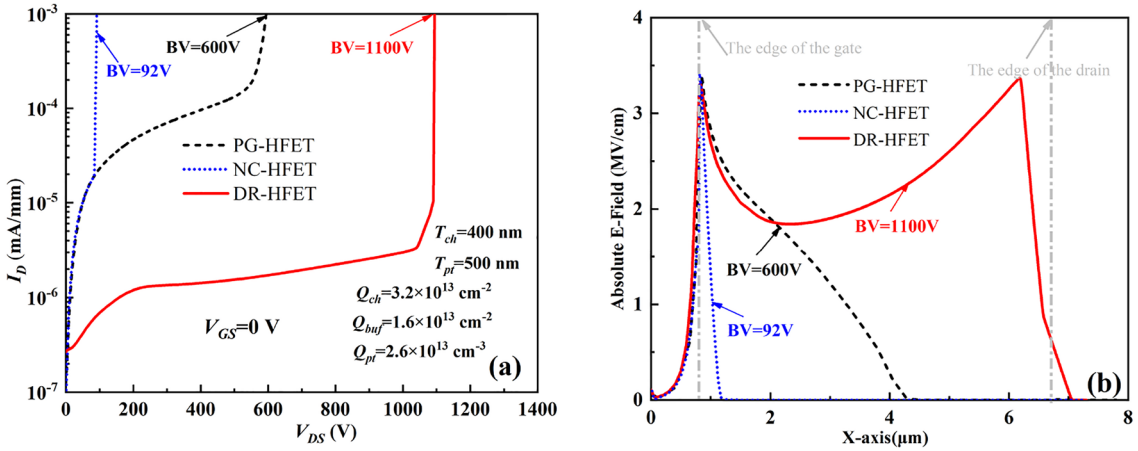

Fig. 6 (a) The BV curves, (b) the E-field distribution along the channel of the PG-HFETs, NC-HFETs and DR-HFETs at the BV.

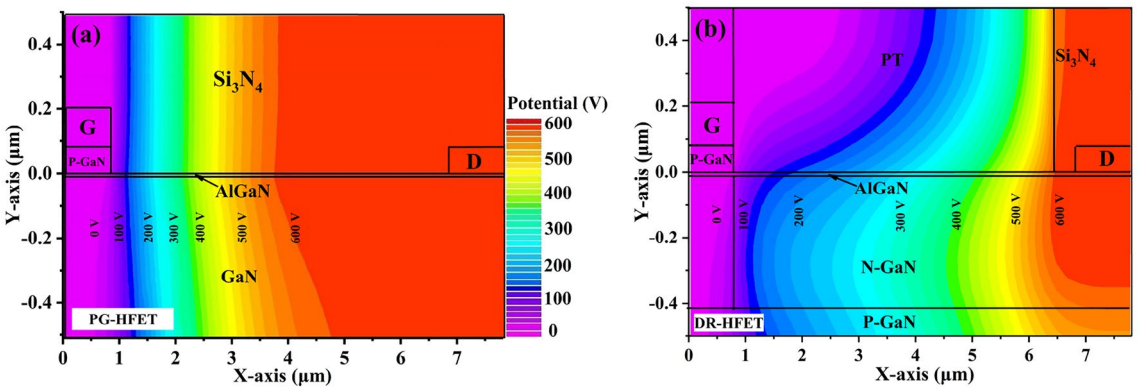

Fig. 7 Potential distribution at V_{DS} = 600 V: (a) PG-HFETs, (b) DR-HFETs.

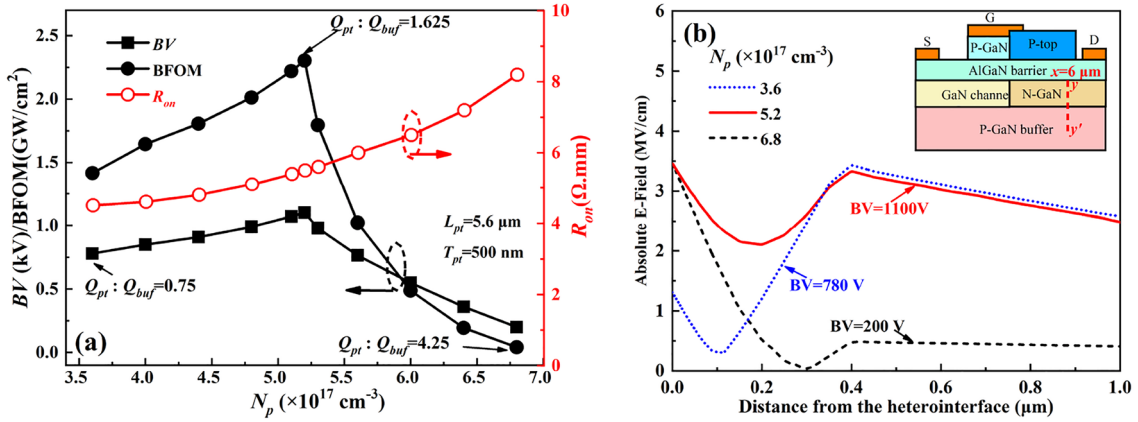

Fig. 8 (a) The N_p dependence of the BV, R_{on} and BFOM with charge balance at T_{pt} = 500 nm, and (b) the E-field distribution at x = 6 μm with different N_p.

In Figs. 8 and 9, we optimize the structure parameters of the DR-HFETs. The optimization of hole concentration N_p in the P-top layer is shown in Fig. 8a. It should be noted that the optimization of N_p is in accordance with the charge balance principle. Once a value of N_p is defined, the hole concentration of the P-buffer layer N_{buf} can be expressed as

$$N_{buf} = \frac{N_{ch} \cdot T_{ch} - N_p \cdot T_{pt}}{T_{buff}}, \quad (8)$$

where $N_{ch} = 8 \times 10^{17}$ cm^{-3}, $T_{ch} = 400$ nm, and T_{pt} is the thickness of the P-top layer. The T_{pt} has no influence on R_{on}. When a thick P-top layer is grown, the N_p can be smaller upon the same Q_{pt}. When the value of N_p is relatively small, the depletion effect of the P-top layer on the N-GaN channel is decreased, and the DR-HFET will show a low R_{on}. Therefore, the T_{pt} is set as 500 nm, which was the highest value in our previous work.[16] The T_{buff} is the thickness of the P-GaN buffer layer, which is defined as 2.6 μm in the compared experimental PG-HFETs.

When the charge balance principle is followed during the optimization, the proportion of Q_{pt} to Q_{buf} has an optimum value of 1.625 (2.6:1.6). According to the double RESURF theory, the selection of the charge density in P-top and P-sub should maintain the full depletion in the N-drift region under the breakdown voltage. For a uniformly doped drift region, the charge in the P-top layer is usually half of that in the drift region.[20] However, there is a 2DEG channel in the N-GaN drift region of the DR-HFET in our simulation, so the determination of Q_{tp} should ensure the depletion of both the 2DEG channel and the half of the N-GaN drift region. The charge density in the 2DEG channel Q_{2DEG} is calculated as ~ 1×10^{13} cm^{-2} in our simulation.[16] Thus, the optimum value of Q_{pt} should be the sum of Q_{2DEG} and $1/2Q_{ch}$, and is calculated as 2.6×10^{13} cm^{-2}. The above results can also be confirmed in the vertical E-field distribution between y–y' under the heterointerface at $x = 6$ μm in Fig. 7b. When $N_p = 3.6$ or 6.8×10^{17} cm^{-3}, high E-field strength can be observed only at the N-GaN/P-buffer interface or only at the AlGaN/GaN heterointerface. When the $N_p = 5.2 \times 10^{17}$ cm^{-3}, two E-field peaks can be found, at both the N-GaN/P-buffer interface and AlGaN/GaN heterointerface; thus the DR-HFET with $N_p = 5.2 \times 10^{17}$ cm^{-3} shows a relatively uniform distribution of the E-field in the vertical direction.

The L_{pt} dependence of the BV, R_{on} and BFOM is shown in Fig. 9a. When the L_{pt} increases from 1 μm to 5.8 μm, the value of the BV, R_{on} and BFOM increase monotonically. The reason for the increase in BV can be found in Fig. 9b. When the L_{pt} increases, the depletion region under the P-top also extends several microns in the lateral direction, so the E-field along the channel can spread more uniformly, thus improving the BV. Therefore, the optimum L_{pt} is obtained as 5.8 μm in our simulation.

In comparison with other experimental P-GaN gate AlGaN/GaN HFETs in the literature (Fig. 10),[14,15,17,18,21,31–35] our device shows a high BV of 1100 V with a remarkably low $R_{on,sp}$ of 0.53 mΩ cm^2, leading to a BFOM of 2.3 GW/cm^2, which suggests a good balance between the off-state blocking capability and on-state performance.

The Influence of the AlGaN/GaN Quality

Epitaxial growth methods and fabrication process parameters may influence the quality of the AlGaN/GaN heterostructure. Typical growth methods for AlGaN/GaN include molecular-beam epitaxy (MBE) and metal–organic vapor-phase epitaxy (MOVPE), and the low field mobility is most affected by different growth methods.[36] According to experimental results, the electron mobility may vary from

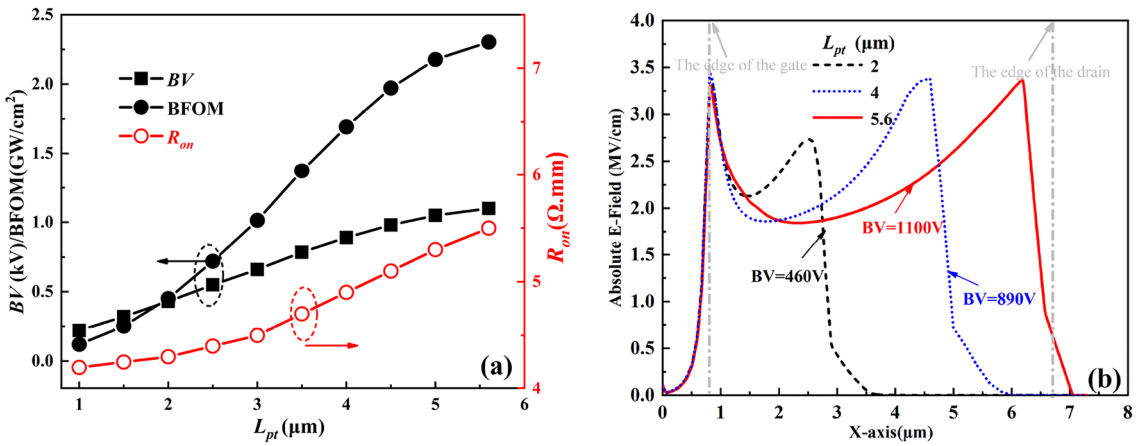

Fig. 9 (a) The L_{pt} dependence of the BV, R_{on} and BFOM, and (b) the E-field distribution at $y = 13$ nm with different L_{pt}.

2000 $cm^2/(V\ s)$ to 500 $cm^2/(V\ s)$ under different growth conditions.

In our simulation, we use the Lombardi model to calculate the mobility under low electric field conditions. As described in the Lombardi model, the electron mobility is limited by surface acoustic phonon scattering, doping-dependent scattering and interface roughness scattering, while surface acoustic phonon scattering and interface roughness scattering are related to the quality of the AlGaN/GaN heterostructure.[36] Therefore, we tune the parameters of B, C and δ in the Lombardi model to simulate the impact of the AlGaN/GaN material quality. Otherwise, we make no changes to the μ_{max}, μ_0, C_r or $\alpha 1$ values in the doping-dependent scattering part of the Lombardi model during the low field mobility simulation. Finally, the low field electron mobility μ_n varies from 500 $cm^2/(V\ s)$ to 2000 $cm^2/(V\ s)$ when we tune the parameters in the simulation.

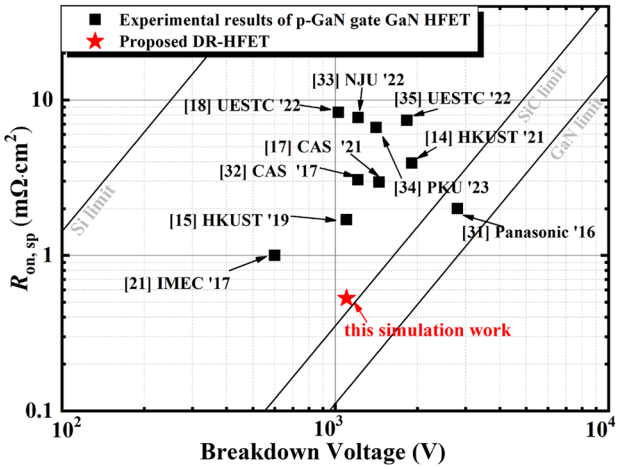

Fig. 10 Comparison plots of BV versus $R_{on,sp}$ for the P-GaN gate HFET.

Figure 11a shows the relationships between the R_{on} and the N_{ch} and T_{ch} of the NC-HFETs with varied μ_n. The μ_n in the previous simulation results is 700 $cm^2/(V\ s)$. When the growth quality of the AlGaN/GaN is improved, the μ_n will increase while the R_{on} of PG-HFET will decrease. When the mobility is higher, the R_{on} of the PG-HFET is lower, and thus the impact of the N_{ch} and the T_{ch} on the R_{on} is decreased. When $\mu_n = 2000$ $cm^2/(V\ s)$, the R_{on} of the PG-HFET is 14.2 Ω mm, and when $\mu_n = 500$ $cm^2/(V\ s)$, the R_{on} of the PG-HFET is 3.5 Ω mm. After considering the benefit threshold of R_{on}, by increasing the channel doping concentration, the R_{on} of the NC-HFET with $\mu_n = 500$ $cm^2/(V\ s)$ can be reduced by 8.4 Ω mm, while for the NC-HFET with $\mu_n = 2000$ $cm^2/(V\ s)$, the R_{on} can be reduced from 3.5 Ω mm to 1.5 Ω mm. When $T_{ch} = 400$ nm, the optimum N_{ch} is around $\sim 8 \times 10^{17}$ cm^{-3}, while the R_{on} for each NC-HFET with different μ_n reaches the benefit threshold. Therefore, when the quality of the material is improved, the effects of the R_{on} reduction by increasing N_{ch} or T_{ch} become weak.

As shown in Fig. 11b, when the μ_n increases to 2000 $cm^2/(V\ s)$, the I_{dlin} of the DR-HFET reaches 47.6 mA/mm, while the R_{on} of the devices is as low as 2.1 Ω mm. The reduction in R_{on} with the double RESURF structure is 1.4 Ω mm, which is the lowest R_{on} improvement among the emulated DR-HFETs.

The graph inset in Fig. 11b shows the dependence of the relative increase in the R_{on} and BFOM on the μ_n. It should be noted that the relationship between the BV and the material quality is unclear. If the GaN buffer is of poor quality, the buffer leakage current may increase, causing a premature breakdown.[37] Otherwise, in our simulation case, we add acceptor traps into the GaN buffer of the PG-HFETs, and we

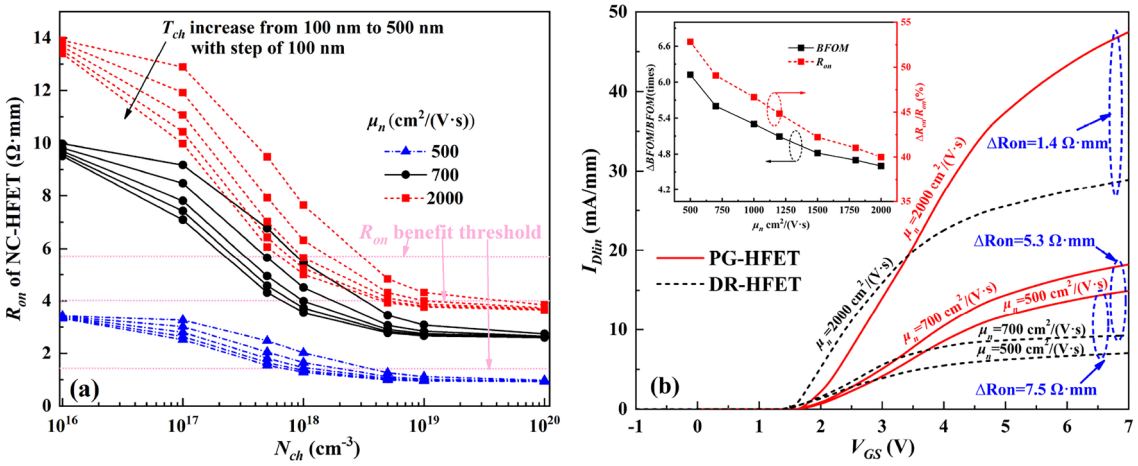

Fig. 11 (a) The relationships between the R_{on} and the N_{ch} and T_{ch} of the NC-HFETs with varied electron mobility μ_n, and (b) the dependence of PG-HFETs and transfer curves, the relative variation of the R_{on} and the BFOM on the μ_n.

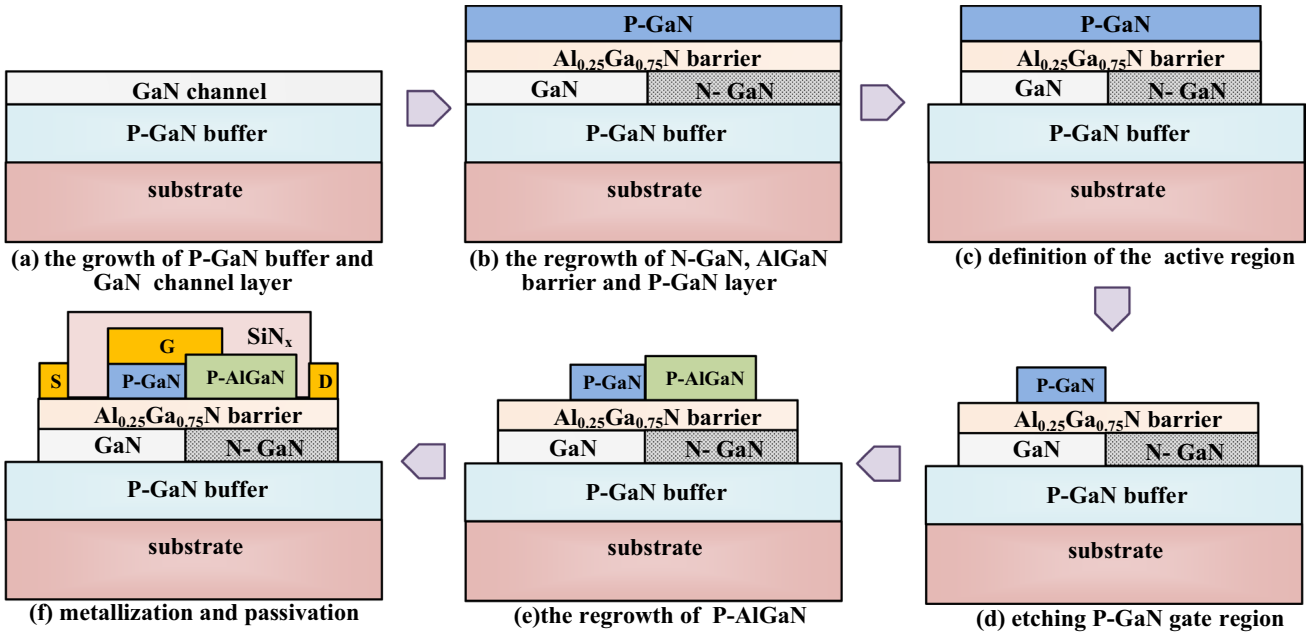

Fig. 12 Schematic for the fabrication steps of the DR-HFET: (a) the growth of P-GaN buffer and GaN channel layer, (b) the regrowth of N-GaN, AlGaN barrier and P-GaN layer, (c) the definition of the active region, (d) etching P-GaN gate region, (e) the regrowth of P-AlGaN, (f) metallization and passivation.

use P-GaN as a buffer layer in the DR-HFETs. The P-GaN buffer or acceptor trap-doped buffer shows low leakage current, and avoids premature breakdown.[38,39] Thus, in our simulation case, the BV of the PG-HFETs remains 600 V, while the BV of the DR-HFETs remains 1100 V. When the μ_n increases from 500 $cm^2/(V\ s)$ to 2000 $cm^2/(V\ s)$, the relative reduction of the R_{on} decreases from 53% to 40%, while the relative increase in the BFOM decreases from 6.1 times to 4.6 times. Therefore, the enhancement of forward characteristics and BFOM of the DR-HFETs would gradually weaken when the quality of the AlGaN/GaN is improved.

Key Fabrication Steps

Figure 12 shows the main fabrication steps for the DR-HFET. After growth of the P-GaN buffer/GaN channel epitaxy by metal–organic chemical vapor deposition (MOCVD) (Fig. 12a), the Si-doped GaN channel, the AlGaN barrier and the P-GaN are regrown on the dielectric patterned wafer after selective etching of the GaN channel (Fig. 12b). Then, mesa isolation is conducted to define the active region of the devices (Fig. 12c). The P-GaN gate region is formatted after selective etching of the P-GaN layer (Fig. 12d). Then, a patterned dielectric is deposited after a surface treatment, and the patterned dielectric is used to perform selective area growth of P-AlGaN (Fig. 12e). Finally, a passivation layer is deposited and patterned after the formation of metal contacts (Fig. 12f).

Conclusion

A method for improving on-state performance utilizing double RESURF technology is presented for a P-GaN gate GaN HFET by TCAD simulation. With the simulation validation and the optimization of the Q_{ch}, Q_{pt} and Q_{buf} in the double RESURF structure, a BV of 1100 V and BFOM of 2.3 GW/cm^2 can be achieved, which indicates a good balance between off-state blocking capability and on-state performance.

Acknowledgments This work was financially supported by the Key RD foundation of Sichuan Province (Grant No. 2022YFG0338) and Natural Science Foundation of Sichuan Province Project (Grant No. 2022NSFSC0965).

Conflict of interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

1. A.I. Emon, M. Hassan, A.B. Mirza, J. Kaplun, S.S. Vala, and F. Luo, A review of high-speed GaN power modules: state of the art, challenges, and solutions. *IEEE J. Emerg. Sel. Top. Power Electron.* 11, 2707 (2023).
2. Y. Zhang, F. Udrea, and H. Wang, Multidimensional device architectures for efficient power electronics. *Nat. Electron.* 5, 723 (2022).

3. B.N. Pushpakaran, A.S. Subburaj, and S.B. Bayne, Commercial GaN-based power electronic systems: a review. *J. Electron. Mater.* 49, 6247 (2020).
4. C. Bryan, P. Faucherand, M. Charles, M. Plissonnier, and G. Savelli, Thermoelectric properties of n-type GaN and 2D electron gas in AlGaN-GaN heterostructure. *J. Electron. Mater.* 50, 1301 (2021).
5. J. Ajayan, D. Nirmal, P. Mohankumar, B. Mounika, S. Bhattacharya, S. Tayal, and A.S.A. Fletcher, Challenges in material processing and reliability issues in AlGaN/GaN HEMTs on silicon wafers for future RF power electronics & switching applications: a critical review. *Mater. Sci. Semicond. Process.* 151, 106982 (2022).
6. A. Udabe, I. Baraia-Etxaburu, and D.G. Diez, Gallium nitride power devices: a state of the art review. *IEEE Access* 11, 48628 (2023).
7. Y.-C. Lai, Y.-N. Zhong, M.-Y. Tsai, and Y.-M. Hsin, Gate capacitance and off-state characteristics of E-mode p-GaN gate AlGaN/GaN high-electron-mobility transistors after gate stress bias. *J. Electron. Mater.* 50, 1162 (2021).
8. N. Kim, J. Yu, W. Zhang, R. Li, M. Wang, and W.T. Ng, Current trends in the development of normally-OFF GaN-on-Si power transistors and power modules: a review. *J. Electron. Mater.* 49, 6829 (2020).
9. E.A. Jones, F.F. Wang, and D. Costinett, Review of commercial GaN power devices and GaN-based converter design challenges. *IEEE J. Emerg. Sel. Top. Power Electron.* 4, 707 (2016).
10. Y. Zhang, C. Yao, X. Zhang, H. Chen, H. Li, and J. Wang, Power loss model for GaN-based MHz critical conduction mode power factor correction circuits. *IEEE J. Emerg. Sel. Top. Power Electron.* 8, 141 (2020).
11. K. Kumar and R.K. Behera, Loss assessment of a 3.3 kW integrated charger for electric vehicles using GaN semiconductor devices, in *IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy* (Cochin, India), 2020 (2020), p. 19535095.
12. J. Lu, L. Zhu, G. Liu, and H. Bai, Device and system-level transient analysis in a modular designed sub-MW EV fast charging station using hybrid GaN HEMTs + Si MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* 7, 143 (2019). https://doi.org/10.1109/JESTPE.2018.2834483.
13. Z. Bai, J. Du, H. Wang, X. Li, and Q. Yu, Simulation design of high Baliga's figure of merit normally-off P-GaN gate AlGaN/GaN heterostructure field effect transistors with junction field plates. *Superlattice Microstruct.* 123, 257 (2018).
14. H. Jiang, Q. Lyu, R. Zhu, P. Xiang, K. Cheng, and K.M. Lau, 1300 V normally-OFF p-GaN gate HEMTs on Si with high ON-state drain current. *IEEE Trans. Electron Devices* 68, 653 (2021).
15. H. Jiang, R. Zhu, Q. Lyu, and K.M. Lau, High-voltage p-GaN HEMTs with off-state blocking capability after gate breakdown. *IEEE Electron Device Lett.* 40, 530 (2019).
16. Z. Bai, S. Chai, C. Zhao, and L. Wang, Design of high Baliga's figure-of-merit P-GaN gate AlGaN/GaN heterostructure field-effect transistors with P-AlGaN field plates. *J. Electron. Mater.* 52, 3892 (2023).
17. X. Wei, X. Zhang, C. Sun, W. Tang, C. Zeng, F. Chen, T. He, G. Yu, L. Song, W. Lin, X. Zhang, D. Zhao, W. Huang, Y. Cai, and B. Zhang, Improvement of breakdown voltage and ON-resistance in normally-off AlGaN/GaN HEMTs using etching-free p-GaN stripe array gate. *IEEE Trans. Electron Devices* 68, 5041 (2021).
18. R. Sun, P. Luo, F. Wang, C. Liu, W. Xu, Y. Wang, G. Ding, H. Yang, Q. Feng, W. Chen, and B. Zhang, Reverse blocking p-GaN gate HEMTs with multicolumn p-GaN/Schottky alternate-island drain. *IEEE Electron Device Lett.* 43, 850 (2022).
19. X. Zhou, L. Geng, Y. Li, X. Fang, Z. Wang, S. Zhu, J. Wu, M. Qiao, and B. Zhang, Investigation on total-ionizing-dose radiation response for 700 V double-RESURF SOI LDMOS. *IEEE Trans. Nucl. Sci.* 69, 1134 (2022).
20. M. Imam, Z. Hossain, M. Quddus, J. Adams, C. Hoggatt, T. Ishiguro, and R. Nair, Design and optimization of double-RESURF high-voltage lateral devices for a manufacturable process. *IEEE Trans. Electron Devices* 50, 1697 (2003).
21. X. Li, M.V. Hove, M. Zhao, K. Geens, V. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, 200 V enhancement-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI with trench isolation for monolithic integration. *IEEE Electron Device Lett.* 38, 918 (2017).
22. ATLAS User's Manual (Silvaco Int. Santa Clara, 2018), pp. 541–557.
23. Y. Liu, Q. Yu, and J. Du, Simulation design of a high-breakdown-voltage p-GaN-gate GaN HEMT with a hybrid AlGaN buffer layer for power electronics applications. *J. Comput. Electron.* 19, 1527 (2020).
24. S. Gustafsson, J.T. Chen, J. Bergsten, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, Dispersive effects in microwave AlGaN/AlN/GaN HEMTs with carbon doped buffer. *IEEE Trans. Electron. Dev.* 62, 2162 (2015).
25. Z. Bai, J. Du, Q. Xin, R. Li, and Q. Yu, Numerical analysis of the reverse blocking enhancement in High-K passivation AlGaN/GaN Schottky barrier diodes with gated edge termination. *Superlattices Microstruct.* 114, 143 (2018).
26. C. Bulutay, Electron initiated impact ionization in AlGaN alloys. *Semicond. Sci. Technol.* 17, L59 (2002).
27. J. Du, H. Yan, C. Yin, Z. Feng, S. Dun, and Q. Yu, Simulation and characterization of millimeter-wave InAlN/GaN high electron mobility transistors using Lombardi mobility model. *J. Appl. Phys.* 115, 164510 (2014).
28. I. Hwang, H. Choi, J.W. Lee, H. S. Choi, J. Kim, J. Ha, C.-Y. Um, S.-K. Hwang, J. Oh, J.-Y. Kim, J. K. Shin, Y. Park, U. Chung, I.-K. Yoo, and K. Kim, 1.6kV, 2.9 mΩcm2 normally-off p-GaN HEMT device, in *Proceedings of International Symposium on Power Semiconductor* (2012), pp. 44–41.
29. A. Perez-Tomas, M. Placidi, X. Perpina, A. Constant, P. Godignon, X. Jordà, P. Brosselard, and J. Millán, GaN metal-oxide-semiconductor field-effect transistor inversion channel mobility modeling. *J. Appl. Phys.* 105, 114510 (2009).
30. C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, A physically based mobility model for numerical simulation of nonplanar devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* 11, 1164 (1988).
31. H. Handa, S. Ujita, D. Shibata, R. Kajitani, N. Shiozaki, M. Ogawa, H. Umeda, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, High-speed switching and current-collapse-free operation by GaN gate injection transistors with thick GaN buffer on bulk GaN substrates, in *IEEE International Electron Devices Meeting (IEDM)* (2016), pp. 10.3.1–10.3.4.
32. R. Hao, W. Li, K. Fu, G. Yu, L. Song, J. Yuan, J. Li, X. Deng, X. Zhang, Q. Zhou, Y. Fan, W. Shi, Y. Cai, X. Zhang, and B. Zhang, Breakdown enhancement and current collapse suppression by high-resistivity GaN cap layer in normally-off AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* 38, 1567 (2017).
33. F. Zhou, W. Xu, F. Ren, Y. Xia, L. Wu, T. Zhu, D. Chen, R. Zhang, Y. Zheng, and H. Lu, 1.2 kV/25 a normally off P-N junction/AlGaN/GaN HEMTs with nanosecond switching characteristics and robust overvoltage capability. *IEEE Trans. Power Electron.* 37, 26 (2022).
34. J. Cui, Y. Wu, J. Yang, J. Yu, T. Li, X. Yang, B. Shen, M. Wang, and J. Wei, Method to study dynamic depletion behaviors in High-Voltage (BV=1.4 kV) p-GaN Gate HEMT on Sapphire Substrate, in *International Symposium on Power Semiconductor Devices & ICs,* (Hong Kong, China), 2023 (2023), p. 127.

35. C. Yu, F. Wang, J. He, Y. Zhang, R. Sun, W. Xu, G. Ding, Q. Feng, X. Wang, Y. Wang, M. He, W. Chen, H. Jia, and H. Chen, High voltage normally-off p-GaN gate HEMT with the compatible high threshold and drain current. *ECS J. Solid State Sci. Technol.* 11, 085009 (2022).
36. S. Kotzea, W. Witte, B.-J. Godejohann, M. Marx, M. Heuken, H. Kalisch, R. Aidam, and A. Vescan, Comparison of MOCVD and MBE regrowth for CAVET fabrication. *Electronics* 8, 377 (2019).
37. W. Zhang, J. Zhang, M. Xiao, L. Zhang, and Y. Hao, $Al_{0.3}Ga_{0.7}N$/GaN (10 nm)/$Al_{0.1}Ga_{0.9}N$ HEMTs with low leakage current and high three-terminal breakdown voltage. *IEEE Electron Device Lett.* 39, 1370 (2018).
38. N. Remesh, N. Mohan, S. Raghavan, R. Muralidharan, and D.N. Nath, Optimum carbon concentration in GaN-on-silicon for breakdown enhancement in AlGaN/GaN HEMTs. *IEEE Trans. Electron. Dev.* 67, 2311 (2020).
39. D.-S. Kim, J.-B. Ha, S.-N. Kim, E.-H. Kwak, S.-G. Lee, H.-S. Kang, J.-S. Lee, K.-S. Im, K.-W. Kim, and J.-H. Lee, Normally-off operation of Al_2O_3/GaN MOSFET based on AlGaN/GaN heterostructure with p-GaN buffer layer, *in Proceedings of International Symposium on Power Semiconductor*, Hiroshima, Japan (2010), pp. 256–260.