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ORIGINAL RESEARCH ARTICLE

Effect of Thickness and Thermal Treatment on the Electrical Performance of 2D MoS_2 Monolayer and Multilayer Field-Effect Transistors

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Abstract
We deposited high-quality molybdenum disulfide (MoS_2) monolayer and multilayer crystals on SiO_2/Si substrates, by means of a chemical vapor deposition (CVD) process at atmospheric pressure. Notably, NaCl salt was used as component of the precursors to assist the growth of MoS_2 crystals, which were intended for use as the active channel layer in the fabrication of field-effect transistors (FETs). The resulting MoS_2 crystals from this CVD process were analyzed by optical, scanning electron, and atomic force microscopies, and by Raman and photoluminescence spectroscopies. The optical images and the micrographs obtained by SEM revealed the formation of dispersed MoS_2 crystals with a triangular shape all over the SiO_2 surface. The thickness of the MoS_2 crystals, analyzed by atomic force microscopy, showed minimum values of around 0.7 nm, confirming the formation of monolayers. Additionally, multilayers with larger thickness were also identified. The Raman and photoluminescence spectra of the MoS_2 crystals corroborated the formation of single and multiple layers. The fabrication of the FET back-SiO_2 -gate configuration was made by depositing patterned source and drain Ti contacts on the dispersed MoS_2 crystals to achieve the Ti/MoS_2/SiO_2/Si layer stacks. MoS_2-based FETs with one and three layers were assembled and their electrical response analyzed by I–V output and transfer curves showing the typical characteristics of an *n*-type semiconductor channel operating in depletion mode. The electrical performance parameters of the devices, such as mobility and threshold voltage, were also determined from this analysis. Finally, to enhance their electrical response, the MoS_2-based devices were thermally annealed at 200 °C for 30 min in Ar atmosphere. The increase in the mobility of the device was 176% compared to the device before the treatment.

Keywords Chemical vapor deposition · 2D materials · FETs · MoS_2

Introduction

Two-dimensional (2D) layered semiconductor materials, specifically transition metal dichalcogenides (TMDs), have garnered significant interest for their potential applications in numerous electronic and optoelectronic devices.[1,2] These materials possess unique properties, including atomic thinness, a surface free of dangling bonds, a direct energy band in monolayer form, and relatively high carrier mobility.[3–5] Among 2D TMDs, layered molybdenum disulfide (MoS_2) has recently been considered of special importance, and it has emerged as a promising semiconductor material in the application of next-generation electronic devices due to its unique electrical and optical properties.[6,7] For example, 2D MoS_2 field-effect transistors (FETs) have attracted considerable attention as potential building blocks for high-performance, low-power, next-generation electronics devices, and a variety of potential applications in the field of sensors and RF switching devices have been explored.[8–11] The understanding of the electrical response and performance characteristics of 2D MoS_2-based FETs is crucial for their successful integration into practical applications. Several techniques have been employed to achieve the 2D MoS_2 semiconductor layers in FETs, CVD being one of the most convenient for this purpose.[12–14] Other techniques, such as atomic layer

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deposition,[15] mechanical exfoliation,[16] and liquid-phase exfoliation[17] have also been widely explored to obtain 2D MoS_2 layers with controlled thickness and quality. However, mechanical exfoliation or layer transfer methods are not ideal for large-scale manufacturing due to their complex processes and uncertain control over size and layer number of the 2D layers. Chemical vapor deposition (CVD) has emerged as a reliable and promising synthesis method for 2D TMDs, enabling the deposition of monolayers, discrete triangular islands, and continuous thin-to-thick-layer films, offering precise control over film thickness and interface quality.[18] This is why CVD is a widely adopted technique for the growing of high-quality 2D TMDs, including MoS_2. Recently, it has been demonstrated that assisted synthesis using alkali metal halides (AMH), like NaCl, KBr, KCl, etc., plays a crucial role in the growth of different TMDs.[19,20] This process induces the formation of volatile compounds that interact more effectively with the sources of the transition metal and chalcogen, thereby enhancing the characteristics of the deposit, such as size and crystalline quality. It even influences the growth of specific TMDs like ReS_2, $MoSe_2$, and WSe_2.

2D MoS_2-based FETs have shown several advantages such as good thermal stability, high carrier mobility, excellent on/off ratio, and great compatibility with flexible substrates.[21,22] Therefore, the research in this topic is of current interest, including the efforts to advance in fabrication techniques, design of device structures, and the analysis of the performance characteristics. These devices are promising for a wide range of applications. They can be utilized in integrated circuits for digital and analogic electronics, as well as in flexible and wearable devices due to their mechanical flexibility.[23,24] Furthermore, the strong light–matter interaction of 2D MoS_2, due to its direct energy band gap is excellent for potential application in optoelectronic devices, including photodetectors and light-emitting transistors.[25–28] The typical device structure consists of a back-gated structure, where the 2D MoS_2 layer deposited on the dielectric gate material is the semiconductor channel. The selection of the dielectric gate material is critical because it has a great influence on the device performance parameters, such as carrier mobility, threshold voltage, and on/off ratio. Some commonly reported dielectric gate materials employed to assemble 2D MoS_2-based FETs are SiO_2, HfO_2 , and Al_2O_3.[29–32]

In this paper, we report the synthesis of 2D MoS_2 semiconductor crystals by an atmospheric pressure CVD (APCVD) AMH assisted method, using NaCl as growth promoter, and its application as active layers in FETs with a SiO_2 dielectric gate. To assemble the FETs with a back-gate configuration, the 2D MoS_2 crystals were deposited on Si/SiO_2 wafers and, by means of a lift-off photolithography process, source and drain Ti contacts were evaporated on some of these dispersed crystals to complete the devices. This procedure enables the fabrication of FETs with either single or multiple layers of 2D MoS_2. The aim of the paper is to determine the effect of the MoS_2 active layer thickness on the electrical response of the assembled FETs, as well as the impact of post-deposition thermal annealing treatment. For this, we include here the description of the APCVD process and the analysis of the main characteristics of the 2D MoS_2 crystals by spectroscopic and microscopic techniques. Moreover, the electrical responses of two types of 2D MoS_2-based FETs have been investigated, with the semiconductor active layer consisting of a single layer and three layers of 2D MoS_2 crystals, respectively. The fabricated devices exhibited typical characteristics of an *n*-type channel working in the depletion mode. Finally, to enhance the performance of the 2D MoS_2-based FETs, a heat treatment at 200 °C for 30 min was conducted, which resulted in an increase of the drain current and enhanced mobility with lowering of the threshold voltage for both types of devices.

Experimental

2D MoS_2 CVD Growth

Monolayers and multilayers of MoS_2 were synthesized using the APCVD method. The 2D MoS_2 crystals were deposited on 25 × 15 mm^2 pieces of SiO_2(300 nm)/Si substrates (*p*-type, B-doped, orientation 100, 1–10 Ohm cm). Prior to the deposition, the organic and inorganic residuals on the substrates were removed through sequential ultrasonic baths in acetone and isopropyl alcohol. Figure 1a displays the experimental setup and Fig. 2b the temperature ramp of the CVD process for MoS_2 growth. An alumina boat loaded with the blend of 30 mg of molybdenum dioxide (MoO_2; 99.0%; Sigma Aldrich) precursor powder with 1 mg of NaCl (99.0%; Sigma Aldrich) was placed in the center of a tube furnace. The Si/SiO_2 substrate was positioned in the center of the boat with the polished side facing down. Another alumina boat with 150 mg of S (99.5%; Alfa Aesar) was placed upstream at the edge of the furnace. The distance between these two boats was optimized to approximately 19 cm. At the beginning of the heating process, 80 sccm of Ar was introduced into the system as a carrier gas and remained throughout the process. As shown in Fig. 1b, the temperature was gradually increased from room temperature up to 550 °C at a rate of 30 °C/min, and then, after 5 min, increased again up to 750 °C at 5 °C/min. This temperature, 750 °C, was kept for 5 min, and, finally, the furnace is naturally cooled to room temperature.

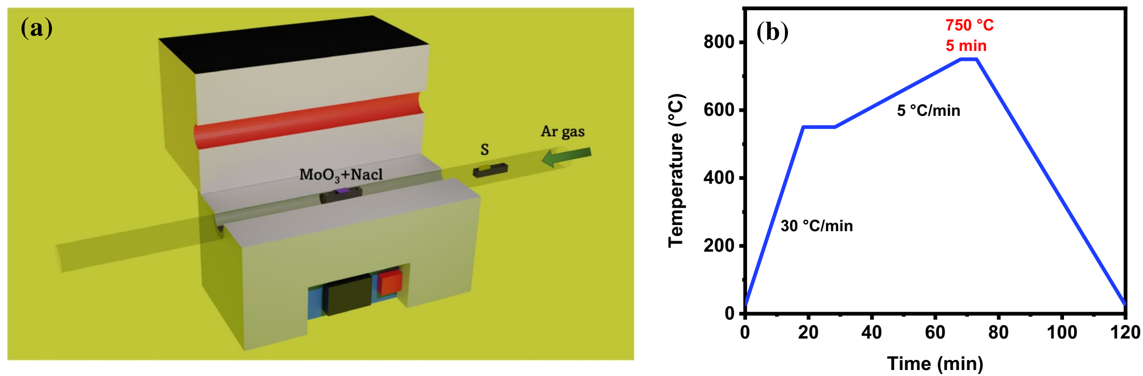

Fig. 1 (a) Schematic of the setup of the CVD process, and (b) variation of the furnace temperature during the MoS_2 growth CVD process.

MoS_2 Device Fabrication

The FETs were fabricated by covering the MoS_2 crystals deposited on the SiO_2 dielectric surface by the CVD process with a patterning of source and drain Ti contacts. For the patterning, a lift-off layer (500 nm) (LOR 5A; Micro Chemical) and a 1.9-μm-thick photoresist layer (Micropositt m S1818TM) were initially spin-coated at 1000 rpm for 10 s (step 1) and 4000 rpm for 40 s (step 2). Subsequently, the lift-off layer and the photoresist were baked on a hot plate at 170 °C and 110 °C, respectively, for 2 min. After annealing, UV light was exposed for 13 s using a photomask aligner (Mask Aligner and UV Exposure System 83210), and the photoresist layer was developed for 30 s. Then, the source (S) and drain (D) Ti (100 nm) ohmic contact electrodes were deposited using a DC magnetron sputtering system. Finally, the lift-off process removed the photoresist layers.

Materials and Devices Characterization

Scanning electron microscope (SEM; JXA-8530F; JEOL) was utilized for capturing images to determine the shape of the MoS_2 crystals. The surface morphology and thickness (number of layers) of the 2D MoS_2 crystals on the SiO_2 surface were examined by using an atomic force microscope (AFM; INNOVA; Bruker). The optical characteristics of the CVD-grown MoS_2 were evaluated through Raman spectroscopy and photoluminescence (PL) spectroscopy (Labram HR Evolution; HORIBA Scientific). The electrical response of the 2D MoS_2-based FETs was analyzed from current–voltage measurements in a dark environment at room temperature performed with a semiconductor parameter analyzer (Keithley 4200).

Results and Discussion

2D MoS_2 Single and Multilayers

Figure 2a shows an optical image of the deposited MoS_2 on the SiO_2 surface, from which it can be seen that there is a typical random distribution of triangular-shaped MoS_2 crystals dispersed throughout the substrate surface. The different dark and bright colors of the MoS_2 crystals in this image are directly related to the presence of monolayers and multilayers.[33] These features are characteristics of the CVD growth of 2D MoS_2 crystals. The SEM image in Fig. 2b is a higher-amplification image of these crystals, where two triangular MoS_2 crystals are observed. The triangles have a size of around 20 μm and not sharp corners but truncated, which is attributed to the Mo:S atomic ratio reacting on the substrate.[34] In addition, smaller triangular MoS_2 crystals with sharp corners grew on the center of both truncated triangles, evidencing the formation of multilayers in a partial area. In both cases, several triangles stack at the center of the larger triangle. A topography analysis, performed by AFM and shown in Fig. 1a, corroborated the coexistence of monolayers and multilayers among the MoS_2 crystals. The AFM image in Fig. 2c displays a large triangular MoS_2 crystal, in which two straight dotted lines are drawn, one at the center of one of the triangle sides and the other one around one corner, respectively. The height profiles along these lines are shown in Fig. 2d and e for the line at the center of the side and the corner, respectively. These profiles reveal that the height steps between the MoS_2 crystal and the SiO_2 substrate at these points are 0.78 and 2.6 nm, respectively. The height of the step at the center of the triangle of the MoS_2 crystal coincides with the reported value for the thickness of a MoS_2 monolayer.[9,10,13,35] Meanwhile, the height step around the corner, 2.6 nm, suggests the formation of a stack of three

Fig. 2 (a) Optical and (b) SEM images of MoS_2 crystals grown by CVD on SiO_2/Si at 750 °C for 5 min. (c) AFM image of the MoS_2 crystals on the SiO_2/Si substrate. Height profile of a MoS_2 (d) monolayer (*dotted line* AFM image) and (e) trilayer (*dashed line* AFM image).

MoS_2 monolayers (trilayer) in this zone. The monolayer and trilayer of MoS_2, as identified in Fig. 2c, were further analyzed by Raman and photoluminescence spectroscopy. The Raman spectra of crystals display two characteristic Raman peaks ,as shown in Fig. 3a. For the monolayer,[36] the peak related to the out-of-plane vibrations of S atoms (A_{1g}) is observed at ~ 405 cm^{-1}, and for the in-plane vibrations of S and Mo atoms (E_{12g}) at ~ 384 cm^{-1}. The difference between the positions of the A_{1g} and E_{12g} Raman peaks is related to the thickness of the MoS_2 crystals. In our case, this difference is ~ 21 cm^{-1}; this value has been reported for single layers of MoS_2 crystals, corroborating that it is a monolayer.[37] As observed in Fig. 3a, in the trilayer MoS_2 spectrum, the A_{1g} Raman peak shifts towards higher energy

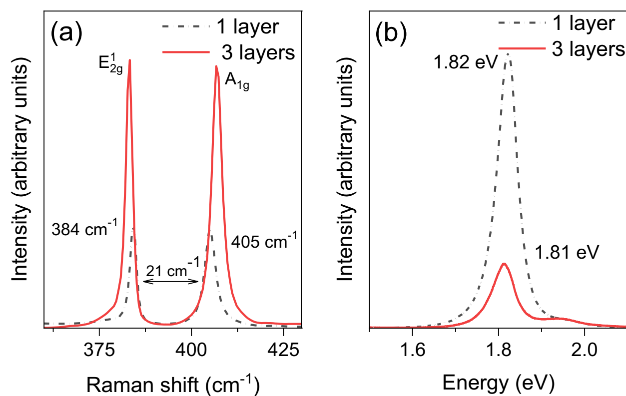

Fig. 3 (a) Raman and (b) PL spectra of the monolayer and the trilayer of MoS_2 crystals shown in Fig. 2c.

values. This is because it is associated with the out-of-plane vibration of S atoms, and the vibrational energy of the lattice decreases as the underlying layer feels the electric potential of the MoS_2 layers above. For the E_{12g} mode, the Raman peak shifts towards lower energy values, as it is associated with the in-plane vibration of the atoms. With an increasing number of layers, the electrostatic repulsion force between the atoms increases, resulting in a lower vibrational energy of the mode. As a result, the difference between the A_{1g} and E_{12g} Raman peaks increases with the number of layers of the MoS_2 crystals; for the trilayer, the measured value is 23 cm^{-1}.[38] The photoluminescence spectra of MoS_2 crystals also exhibit a strong dependence on the number of layers. Due to the two-dimensional confinement, monolayers of MoS_2 have a direct band gap of 1.82 eV, which enables a strong photoluminescence emission. On the other hand, MoS_2 in multilayers has an indirect band gap that is smaller than 1.81 eV, resulting in a much weaker emission intensity[39]. Figure 3b shows the photoluminescence spectra acquired at room temperature in the same points where the Raman measurements were performed for the monolayer and trilayer of MoS_2. Both spectra display an emission band at 1.82 eV related to exciton A.[40] As expected, the emission intensity of the monolayer is much higher than that of the trilayer in these spectra. The transition of MoS_2 from direct band gap to an indirect band gap material by the increasing the number of layers also produces a red shift of the emission band,[41] which is observed in these photoluminescence spectra. Furthermore, a second contribution to the emission can be observed at higher energies due to the spin–orbit coupling present in these semiconductors. There is a degeneracy in the valence band, allowing for another transition at the same high-symmetry point near the valence band but with higher energy. This transition is referred to as exciton B.[42,43]

2D MoS_2 thin film transistors

As described in the previous section, the CVD process resulted in the growth of MoS_2 crystals with different number of layers randomly dispersed on the SiO_2/Si substrates. The MoS_2 crystals were used as semiconductor active layers in FETs with the back-gate configuration shown in Fig. 4a, where the moderately doped *p*-type Si substrate is the gate electrode, and the SiO_2 layer is the dielectric gate.

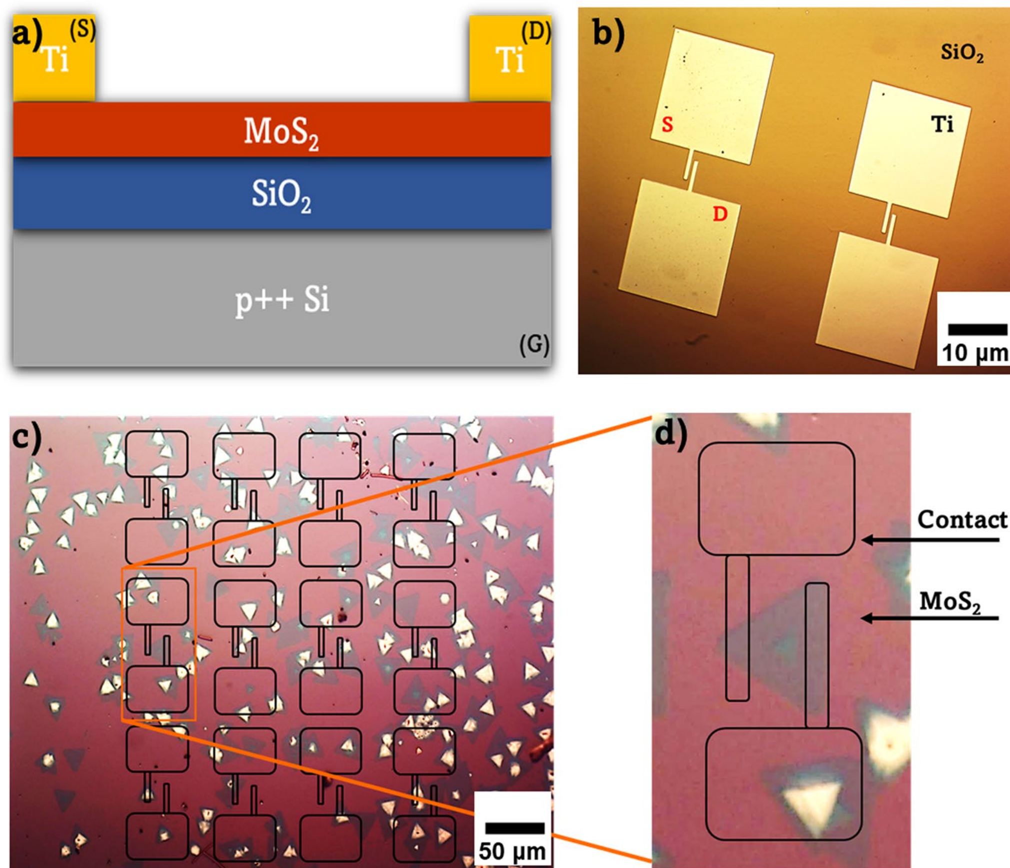

Fig. 4 (a) Schematic of the back-gate configuration of the MoS_2-based FET; *S* source, *D* drain, *G* gate. (b) Optical image of the source and drain Ti contacts. (c) Optical image of the shadow mask pattern on the MoS_2 crystals. (d) Amplified image of a complete layer stack of the FET.

The devices were completed by the patterning of source and drain Ti contacts by the lift-off photolithography process described in the experimental section.

Figure 4b shows two pairs of the Ti contacts after the lift-off process. Since the growth of the MoS_2 crystals is random on the SiO_2 surface, the alignment of the source and drain contacts, defined by the mask employed for the patterning to achieve the stack configuration in Fig. 4a, necessarily requires a successful coincidence. This situation can be seen in Fig. 4c where the patterned source and drain Ti contacts can be seen deposited mostly on the SiO_2 surface, or partially over the SiO_2 crystals. However, in some regions, like the one shown in Fig. 4d, there is a successful coincidence of both Ti contacts on a triangular MoS_2 crystal, defining a device with the stack layer in Fig. 4a. This way, we could find in different regions several complete devices with MoS_2 crystals with different number of layers as the semiconductor active layer.

The electrical response was analyzed on two types of FETs with one and three MoS_2 layers. These devices are shown in Fig. 5a and b, respectively, which include the height profiles of the MoS_2 crystals corroborating the number of MoS_2 layers in each case. The average thickness of the single- and three-layer MoS_2 crystals, measured along the gate, were 0.94 ± 0.12 nm and 2.3 ± 0.26 nm, respectively. In these devices, the length of the channel, L, is 7 μm, while, based on these images, the width, W, of the channel is 16 and 14 μm, respectively. Figure 6a and c shows the output drain current versus drain voltage (I_{DS}-V_{DS}) curves at different source-gate voltage (V_{GS}) values from − 5 V to 20 V in steps of 5 V, for the devices with MoS_2 single layer and three layers, respectively.

The output curves of both devices reveal the typical transistor response for an *n*-type semiconductor channel with drain current linear behavior at low drain voltages and saturation at higher voltages. The drain current saturation is achieved at rather low drain voltage, around 2–3 V, in both devices. The maximum values of the drain current at the different values of V_{GS} are higher for the device with three layers of MoS_2. On the other hand, the transfer drain current versus source-gate voltage (I_{DS}–V_{GS}) curves measured at 0.5 V of the source-drain voltage are shown in Fig. 6b and d for the devices with MoS_2 single layer and three layers, respectively. As can be seen, the lowest values of the drain current in both devices are of the order of 10^{-10} A which increases to values of the order of 10^{-8} A with source-gate voltage. From this, both devices have an I_{on}/I_{off} current ratio of 10^2. The field effect mobility in the linear region, μ, and threshold voltage, V_T, can be also determined from the transfer characteristics of the devices using:

$$\mu = \frac{L}{WC_G}\left(\frac{dI_{DS}}{dV_{GS}}\right)\frac{1}{V_{DS}} \tag{1}$$

where L and W are the length and width of the channel, respectively, $(dI_{DS})/(dV_{GS})$ is the slope of the transfer curve of the device, V_{DS} is the applied drain voltage, and C_G is the gate capacitance, which for SiO_2 is ~ 115 μF m^{-2}. The value of $(dI_{DS})/(dV_{GS})$ is obtained by fitting the linear region of the transfer curves, as shown in the right-axis plots of Fig. 6b and d. The drain current in these transfer curves is plotted in linear scale, unlike the left-axis drain current where the scale is logarithmic. The best linear fitting to Eq. (1) is depicted by the red dashed line in both transfer curves. In addition, the threshold voltage of the devices is determined from the

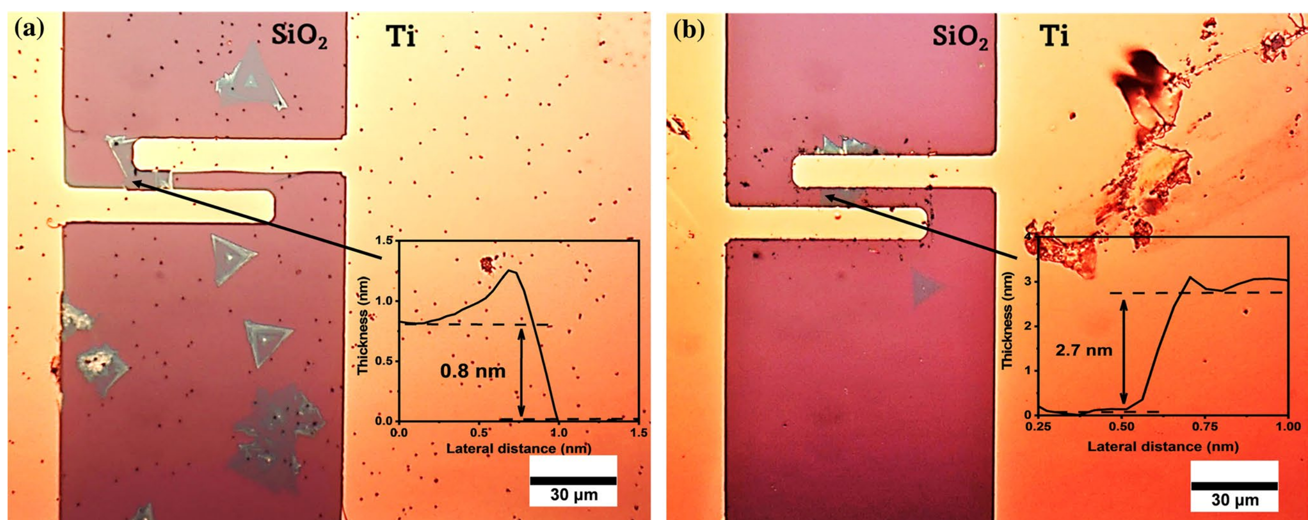

Fig. 5 Optical image of the (a) single- and (b) three-layer MoS_2-based FETs. The height profile corroborating the number of MoS_2 layers in the device is included as an *inset* in each case.

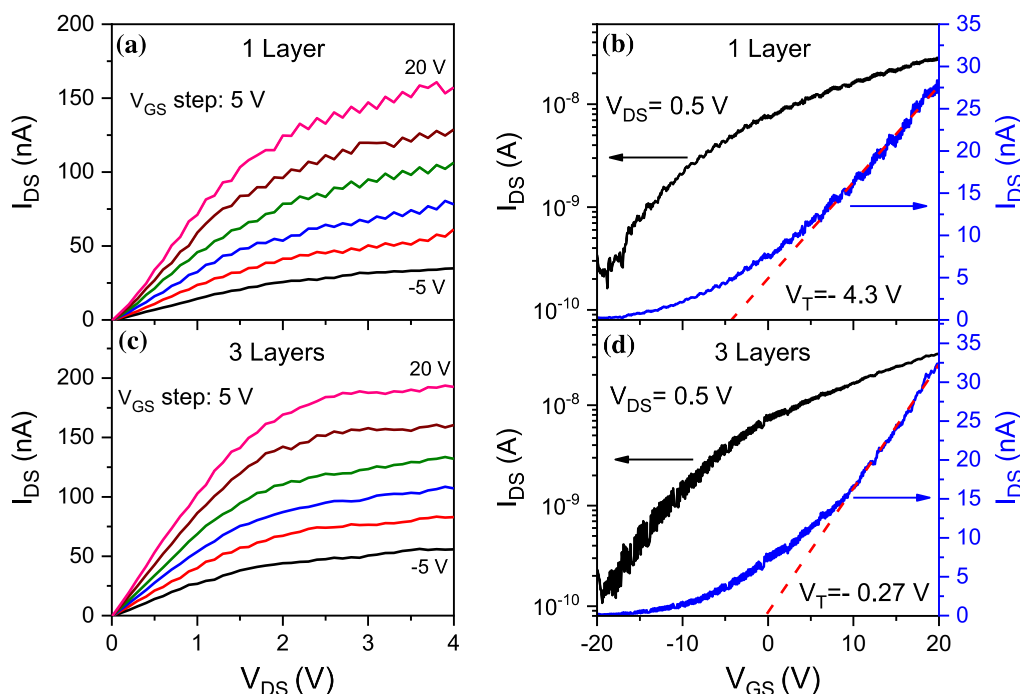

Fig. 6 (a) Output and (b) transfer curves of the single-layer MoS_2-based FET, and (c) output and (d) transfer curves of the three-layer MoS_2-based FET (Color figure online).

Table I Dimensions and electrical performance parameters of the MoS_2 -based FETs with single and three layers, before and after thermal annealing

	L, μm	W, μm	μ, cm^2V^{-1} s^{-1}	V_T, V	I_{ON}/I_{OFF}
1 layer	7	10	0.13	− 4.3	10^2
3 layers	7	12	0.16	− 0.27	10^2
1 layer 200, °C	7	10	0.36	0.53	10^2
3 layers 200, °C	7	12	0.38	− 1.86	10^3

interception of this straight line with the V_{GS} axis. The electrical performance parameters for both types of MoS_2-based FETs are summarized in Table I. The mobility, 0.38 cm^2/Vs, and threshold voltage, − 1.86 V, of the MoS_2 trilayer device are slightly better values than those corresponding to the MoS_2 monolayer device, 0.36 cm^2/Vs and 0.53 V. This difference, attributed to the number of layers of MoS_2, can be due to Coulomb scattering. The higher susceptibility of the monolayer to acquire impurities from the environment, such as water or oxygen molecules, form adsorbates on its surface causing a decrease in the mobility of the device.[44,45] In the same way, since it is a single layer, the roughness can be another important factor in the decrease of this parameter.[46]

To enhance the electrical performance parameters of the MoS_2-based FETs, they were thermally annealed at 200 °C in an Ar atmosphere during 30 min. It is known that the heat treatments improve the electronic transport reducing the resistance of the metal contacts and removing contaminants such as resin residues from the manufacturing process.[47] Likewise, it has been reported that heat treatment induces a structural rearrangement, thus affecting the electrical properties of the MoS_2 semiconductor.[48] Thermal annealing produces the removal of defects and impurities in the MoS_2 crystals, leading to the reduction of charge trapping and improving the charge carrier mobility. This is particularly important in CVD-grown MoS_2 crystals, which may contain a higher density of defects compared to highly crystalline material.[48–50] Because the devices can be damaged by the high temperature,[51] the treatment temperature was chosen as 200 °C. The electrical response of both types of devices after the heat treatment is shown in Fig. 7, where a and c correspond to the output curves and b and d to the transfer ones. The output curves of the annealed devices show the transistor behavior with increased drain current compared to the corresponding curves before annealing. The observed increase of the drain current is higher for the single-layer device, where the current saturation shifts to higher voltage, while the current saturation in the trilayer device is much better at still a low voltage. The observed slope of the output curves in the saturation region of the single-layer device can also be a consequence of the more conductive channel after thermal annealing. The drain current increases, producing

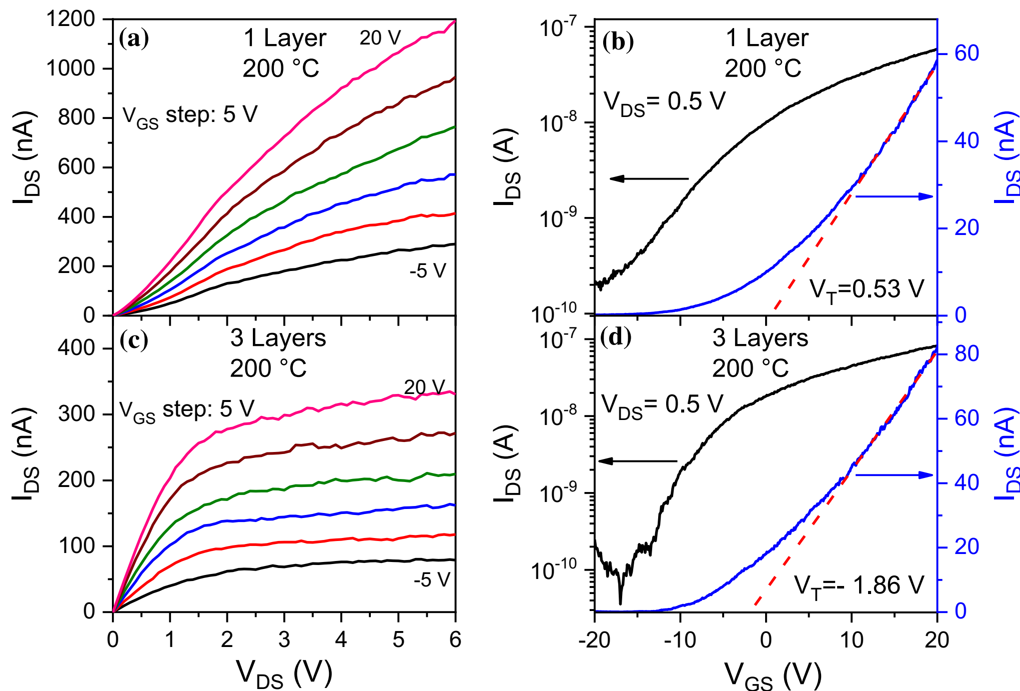

Fig. 7 (a) Output and (b) transfer curves of the single-layer MoS_2-based FET, and (c) output and (d) transfer curves of the three-layer MoS_2-based FET.

the observed slope in the curve, indicating that the polarization of the dielectric gate is not enough to modulate the drain current. The transfer curves also show the increase of the drain current in the annealed device keeping the current level of the off-state of the device. Therefore, the annealing of the devices produces an increase of their I_{on}/I_{off} current ratio, which in the case of the trilayer device is now 10^3. These curves were also fitted to Eq. (1) to determine the mobility and threshold voltage of the annealed devices, and the results are summarized in Table I. These results show that the heat treatment increased by about ~ 1.25 times the mobility of the single-layer and trilayer devices. Meanwhile, the threshold voltage of the single-layer device reduced and even became positive. The negative values of the threshold voltages of *n*-type FETs indicate their depletion operation mode, where at zero gate voltage they are turned on. Therefore, the single-layer device, with very low positive threshold voltage, 0.53 V, changed to enhancement operation mode after thermal annealing, where the device is turned off at zero gate voltage. These results demonstrate the enhancement of the electrical response of the MoS_2-based FETs produced by the thermal treatment at 200 °C.

The values of the mobility and I_{on}/I_{off} current ratio of our FETs can be fairly compared with similar CVD-MoS_2 monolayers and multilayer-based FETs with a SiO_2 dielectric gate. For these devices reported in the literature, the values of mobility and I_{on}/I_{off} current ratio also depend on the number of layers and are in the ranges from 0.003 cm^2/Vs to 45 cm^2/Vs and from 10^3 to 10^7, respectively.[37,52,53] The large difference between these values is mainly due to the CVD-MoS_2-based FETs fabrication processes. Better FET performance parameters are achieved when e-beam lithography is employed in their fabrication, while the photolithography process, like in our case, produces devices with lower values of mobility and I_{on}/I_{off} current ratio.

Conclusions

We have reported the electrical behavior of 2D MoS_2 layers, obtained from an AMH assisted APCVD process, as the active semiconductor layer in FETs with back-SiO_2 -gate configuration. The detailed microscopic and spectroscopic analysis of the 2D MoS_2 deposit on the SiO_2 surface corroborated the formation of single and multiple layers of MoS_2 crystals with a triangular shape. The size of the crystals was a few microns, and the thickness of the single layer was 0.78 nm. The assembling process of the FETs was carried out by depositing a patterning of source and drain Ti contacts on the randomly dispersed MoS_2 crystals, and selecting those where the layer stack configuration of the device was complete. This way, two types of 2D MoS_2-based devices with one and three layers were assembled and analyzed. These devices exhibited *n*-type electrical behavior

operating in the depletion mode, where the trilayer device showed slightly higher mobility, 0.16 cm^2/Vs, with very low threshold voltage, − 0.27 V, than the single-layer device, 0.13 cm^2/Vs and − 4.3 V, respectively. Furthermore, the 2D MoS_2-based FETs were thermally annealed at 200 °C for 30 min to improve their electrical response. This thermal treatment led to a improvement in the drain current for both devices, resulting in a ~ 1.25 times increase in mobility. Specifically, the mobility values increased to 0.36 and 0.38 cm^2/Vs for the single-layer and three-layer devices, respectively. An interesting observation was a change in the threshold voltage of from − 4.3 V to 0.53 V for the single-layer device after thermal annealing, indicating a transition from depletion to enhanced operation mode due to thermal annealing. Furthermore, the I_{on}/I_{off} current ratio of the three-layer device increased to 10^3 after thermal annealing, suggesting an improvement in the device's performance and its potential for practical applications.

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Author contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by BAMM. The first draft of the manuscript was written by BAMM and RRB. All authors commented on previous versions of the manuscript. All authors read an approved the final manuscript.

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Declarations

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

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