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ORIGINAL RESEARCH ARTICLE

Defect Engineering in MBE-Grown CdTe Buffer Layers on GaAs (211)B Substrates

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Abstract
Demand for high-performance HgCdTe infrared detectors with larger array size and lower cost has fuelled the heteroepitaxial growth of HgCdTe on CdTe buffer layers on lattice-mismatched alternative substrates such as Si, Ge, GaAs and GaSb. However, the resulting high threading dislocation (TD) density in HgCdTe/CdTe limits their ultimate application. Herein, strained CdZnTe/CdTe superlattice layers have been used as dislocation filtering layers (DFL) to reduce the TDs in CdTe buffer layers grown on GaAs (211)B substrates (14.4% lattice-mismatch) by molecular beam epitaxy (MBE). Cross-sectional microstructure characterization indicates that the DFLs suppress the propagation of TDs. For optimal Zn content combined with thermal annealing, the DFLs effectively reduce the defect density of the upper-most CdTe layer from low-10^7 cm^{-2} to the critical level of below 10^6 cm^{-2}. In comparison to conventional buffer CdTe layers, the in-plane lattice of the CdTe layers in/near the DFL region is compressively strained, leading to a spread in x-ray double-crystal rocking curve full-width at half-maximum values but better in-plane lattice-matching with HgCdTe. The combined advantages of lower dislocation density and better lattice-matching with HgCdTe indicate that the DFL approach is a promising path towards achieving heteroepitaxy of high-quality HgCdTe on large-area lattice-mismatched substrates for fabricating next-generation infrared detectors.

Keywords CdTe · HgCdTe · alternative substrates · dislocation filters · etch pit density

Introduction

Significant attention has recently been devoted to the epitaxial growth of CdTe layers on alternative substrates (AS), such as Si,[1,2] Ge,[3] GaAs,[4] and GaSb,[5,6] to act as buffer layers for the subsequent growth of HgCdTe infrared (IR) materials for detector devices. These studies of lattice-mismatched heteroepitaxial growth have been motivated by the potential for growing device-quality HgCdTe IR materials on large-area, cost-effective substrates for next-generation HgCdTe IR detectors and imaging focal plane arrays (FPAs).[7] This would lead to lower cost and larger array format in comparison to current state-of-the-art HgCdTe IR detectors grown on lattice-matched $Cd_{0.96}Zn_{0.04}Te$ (CZT) (211)B substrates, which are smaller-area wafers and much higher cost.[8–10] It is widely recognized that defects limit the performance of HgCdTe devices and, therefore, FPA operability. Etch pit density (EPD) analysis has been used as a screening technique to qualify HgCdTe epilayers and CdTe buffer layers.[11] For HgCdTe grown on lattice-matched CZT, the EPD is typically of the order of mid-10^4 cm^{-2}, which corresponds with the EPD of the CZT substrates.[12] Although alternative substrates have much higher crystalline quality (EPD < 10^3 cm^{-2}) than CZT, the large lattice mismatch (f_l) and difference in thermal expansion coefficient (CTE) (f_t) between HgCdTe and these AS (f_l = −19.3%, −14.3%, −14.4%, −6.1%, and f_t = −92%, 14%, 14%, 23% for Si, Ge, GaAs, and GaSb, respectively) inevitably generate misfit dislocations (> 10^8 cm^{-2}) in the vicinity of the CdTe/AS interface. These misfit dislocations form threading

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dislocations (TD) that can propagate into the CdTe buffer layer and the subsequent HgCdTe epitaxial layer.[13]

Providing thick buffer layers is unlikely to yield very high-quality material, so different approaches have been studied to reduce the threading dislocation density (TDD) in CdTe and HgCdTe epitaxial layers grown on AS. These include the use of low-temperature nucleation layers of ZnTe or CdTe,[4] and various forms of cyclic thermal annealing (CTA).[14] Substantial progress has been made, resulting in routine EPD in HgCdTe and CdTe varying between low-10^6 cm^{-2} to low-10^7 cm^{-2}.[4] Although this EPD level is acceptable for the fabrication of shortwave IR (SWIR) and mid-wave IR (MWIR) detectors, a level below mid-10^5 cm^{-2} is needed for longwave IR (LWIR) detectors, which are much more sensitive to material defects due to their narrower band gap.[15,16] Although EPD values of ~ 10^5 cm^{-2} have been achieved in both CdTe/Si and HgCdTe/CdTe/AS layers by using CTA at above 400°C to induce dislocation reduction, there are numerous issues with using this approach at such elevated temperatures. Moreover, the direct growth of HgCdTe on CdTe substrate (EPD of ~ mid-10^4 cm^{-2}) results in EPD in the range of low-10^6 cm^{-2} in HgCdTe, which suggests that reducing the HgCdTe/CdTe lattice-mismatch ($f_l = 0.25\%$) is required in order to achieve the desired HgCdTe EPD values for MWIR/LWIR/AS applications.[17,18] Therefore, improvement of the crystallinity of the HgCdTe epilayer grown on AS, requires a buffer layer with both low dislocation density as well as in-plane lattice-matching. In the past, one approach for reducing the HgCdTe/CdTe lattice-mismatch was by incorporating Zn and/or Se into the CdTe buffer.[19,20] However, due to difficulties related to the epitaxial growth of Cd(Zn, Se)Te by vapor phase methods such as molecular beam epitaxy (MBE), high-quality Cd(Zn, Se)Te ternary buffer layers were difficult to obtain.[21] Hence, there is a strong incentive to develop different buffer layer approaches that have higher efficiency in dislocation reduction and better lattice-matching with HgCdTe.

A strained-layer superlattice (SLS), consisting of alternating strained hetero-layers and generally referred to as a dislocation filtering layer (DFL), has been observed to block TD propagation and thus reduce dislocation density in the overlaying epitaxial layer.[22,23] Although the dislocation filtering efficiency varies with experimental conditions, modeling results indicate that the minimum TDD obtained in any given structure is likely to be limited by kinetic effects to approximately 10^4–10^5 cm^{-2}.[24] Movement of TDs in response to misfit strain combined with thermal energy has been shown to be the best way to enhance the annihilation probability.[25] The SLS-based DFL technology has been successfully demonstrated in the growth of III–V semiconductors on lattice-mismatched substrates for many years. For example, the TDD has been reduced from ~ 10^9 cm^{-2} to ~ 10^5 cm^{-2} for GaAs buffer layers grown on Si by incorporating 4 sets of 10-nm $In_{0.18}Ga_{0.18}As$/10-nm GaAs SLS-based DFLs, leading to high-performance InAs/GaAs quantum dot lasers.[26] In contrast to the CTA techniques used in heteroepitaxial growth, it can be anticipated that incorporating a DFL technology will allow thinner buffer layer thickness, shorter processing time, and lower processing temperature to achieve similar EPD levels due to the high dislocation filtering efficiency. Moreover, the successful application of SLS-based DFLs has been reported for a wide range of hetero-material systems in which the DFL structures are grown with a high degree of control over a range of composition and thickness by epitaxial growth techniques such as MBE.[27–29]

Historically, similar dislocation filtering effects can be found in the early growth of heteroepitaxial CdTe on GaAs (001) with the insertion of thick CdZnTe layers.[30] However, the (211)B orientation has been widely used for growing high-quality HgCdTe since it requires much lower Hg flux than either (001) or (111)A orientations to maintain the same MBE growth rate, and it is less sensitive to micro-twin formation in comparison to (111) A/B.[18] In addition, compared with bulk CdZnTe, SLS-based CdZnTe/CdTe DFLs not only provide more interfaces that increase the chance of coalescence and annihilation of dislocations, but also alleviate growth concerns such as Zn segregation in the CdTe host and the growth temperature incompatibility between ZnTe and CdTe.[31] Limited research has been reported in the open literature on the use of SLS-based CdZnTe/CdTe DFL. Although some preliminary results for CdTe SLS-based DFL buffer layers grown on GaSb (211)B substrates have been reported,[32] information is still lacking for evaluating this DFL approach on alternative substrates, especially GaAs. High-quality (211)B GaAs substrates are lower cost and more readily available in comparison with GaSb substrates of the same orientation.[33]

In comparison to non-polar group IV substrates such as Si and Ge, "epi-ready" GaAs is more readily available and has smaller f_l and f_t with respect to CdTe and HgCdTe. To date, MWIR MCT/GaAs FPAs are commercially available, whereas LWIR MCT/GaAs technology (which is of great interest to the IR industry) is hampered by low operability due to high EPD values. In addition, in the design and MBE growth of CdZnTe/CdTe SLS-based DFL layers, factors such as strain, composition/thickness, growth conditions and annealing temperatures, need to be optimized in order to achieve optimum dislocation filtering efficiency, which represents a large unexplored research space.

Motivated by these considerations, we have undertaken a study of CdTe buffer layers grown on GaAs (211)B substrates and the incorporation of CdZnTe/CdTe SLS-based DFLs. It is shown that the EPD of CdTe buffer layers on GaAs can be effectively reduced from the low-10^7 cm^{-2} to the mid-10^5 cm^{-2} level using DFLs grown with optimal

Zn content and annealing conditions. Moreover, the EPD analysis shows excellent uniformity across the entire 2-inch wafer. These results indicate that DFLs provide a promising approach towards the heteroepitaxy of HgCdTe on large lattice-mismatched substrates with lower dislocation density and smaller lattice-mismatch for application to next-generation IR detectors.

Experimental Section/Methods

Growth of CdTe Buffer Layers on GaAs (211)B Substrates

CdTe buffer layers were grown in a Riber 32P MBE system on 2-inch GaAs (211)B substrates. Elementary Zn, Te, and compound CdTe were loaded in standard Knudsen cells as sources, and the individual fluxes (beam equivalent pressures, BEP) were controlled by adjusting the cell temperatures. To evaluate the in situ oxide desorption process of GaAs substrates prior to MBE growth, reflection-high-energy electron diffraction (RHEED) was used to monitor the transition from a spotty pattern to a streaky pattern as the substrate temperature was raised to ~580°C. After oxide desorption at ~580°C for 3 min, the substrates were cooled down to 220°C, and a thin ZnTe nucleation layer (< 30 nm) was grown at this temperature for 3 min, and then processed by in situ thermal annealing with a background Te BEP of 3×10^{-6} Torr at 380°C for 15 min. Note that ZnTe has a lattice constant intermediate between those of GaAs and CdTe, contributing to better nucleation on GaAs in comparison to CdTe nucleation layer. The thin ZnTe nucleation layer was used in order to suppress three-dimensional growth and preserve a good (211)B interface for the subsequent CdTe growth.[34] After growth of a 2–5 μm thick CdTe bottom layer, several sets of CdZnTe/CdTe SLS DFL were grown, separated by 500-nm-thick CdTe spacer layers. Each set of CdZnTe/CdTe DFL consisted of five periods of ~13 nm CdZnTe (20 s MBE growth)/~11 nm CdTe (20 s MBE growth). In situ thermal annealing for 15 min was undertaken after each DFL growth. The samples were completed by the growth of a 4–20-μm-thick CdTe top layer. Both the CdZnTe and CdTe layers were grown at about 270°C under Te-rich conditions with the Te/CdTe BEP ratio of approximately 1.5. The CdTe DFL buffer layers were grown with different structural designs and annealing conditions to explore their impact on the final EPD of the top CdTe layer.

Characterization of CdTe Buffer Layers

Fourier-transform IR spectroscopy (FTIR) was used to measure the buffer layer thickness and, therefore, the CdTe growth rate. A Philips X'pert MRD high-resolution x-ray diffractometer (HRXRD) equipped with a four-crystal Ge (220) monochromator was used to obtain double-crystal rocking curve (DCRC) full-width at half-maximum (FWHM) rocking curve values for the layers as well as to determine the structural parameters of the CdZnTe/CdTe DFL, including Zn composition, thickness, and lattice strain through ω–2θ scans and/or reciprocal space mapping (RSM) measurement. Similar XRD analysis has been described in our previous work.[32] The CdTe surface morphology of the samples was evaluated using optical microscopy and scanning electron microscopy (SEM). The dislocation density in the samples was characterized via EPD measurements using a standard Everson etchant,[35] optical microscopy, and SEM imaging. Cross-sectional transmission electron microscopy (TEM) and SEM images were used to investigate the crystalline quality in more detail. Photoluminescence (PL) spectra were acquired in an unpolarized quasi-backscattering geometry with an Alpha 300 confocal Raman microscope (WITec, GmbH) using a 785 nm laser (laser spot size of ~10 μm) and a 600 g mm^{-1} diffraction grating (spectral resolution of ~0.75 meV). The CdTe buffer layers were etched to the desired thickness for depth profiling using bromine methanol in order to study the dependence of material properties such as EPD, XRD FWHM, and PL on the thickness.

Results and Discussion

CdTe Buffer Layers with Strained CdZnTe/CdTe Superlattice-Based DFL

Structure Design and MBE Growth

Figure 1a shows a typical sample structure for a CdTe buffer layer on a 2-inch GaAs (211)B substrate with five sets of $Cd_{1-x}Zn_xTe$/CdTe SLS-based DFL. The purpose of the SLS layer structure is to increase the likelihood of dislocation annihilation and inhibit dislocation multiplication and/or propagation. As discussed by Wark et al.,[24] the key to significant reduction in TDD is TD movement using misfit stress, i.e., in layers with a finite strain-thickness product (εh). Moreover, a good rule of thumb for DFL design in heteroepitaxial growth is given by $\varepsilon_c h_c < \varepsilon h < 4\varepsilon_c h_c$, where $\varepsilon_c h_c$ is a constant (experimentally, $\varepsilon_c h_c$ is ~0.24 nm in the GaInAs system). This can be understood by considering that the stress in the DFL needs to be high enough to divert TDs but not enough to generate additional TDs. In a layer of constant composition, dislocation multiplication is expected to commence when the strain thickness product exceeds ~$4\varepsilon_c h_c$, which places an upper limit on the strain and thickness of a DFL.[36]

In calculating this product, the superlattice structure of each DFL set can be considered to be equivalent to a

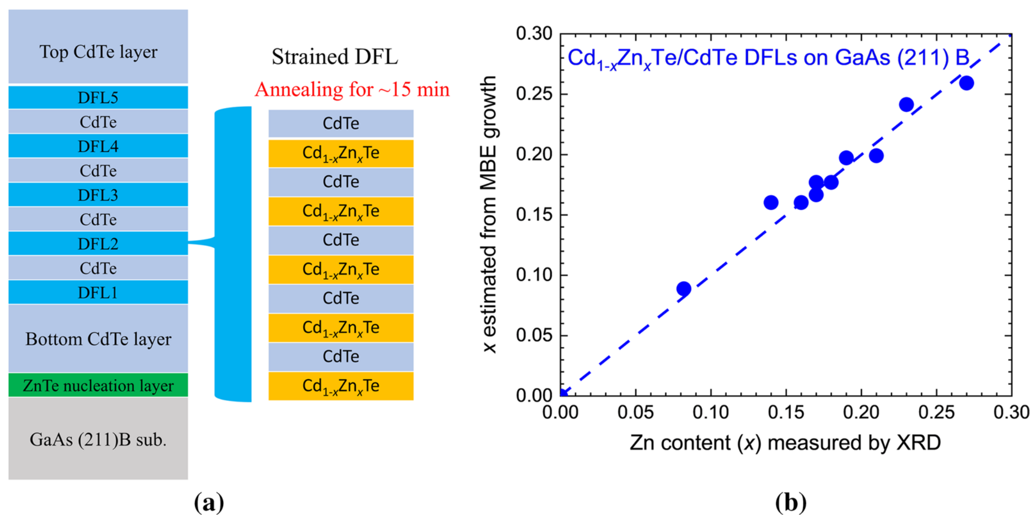

Fig. 1 (a) Schematic sample structure for MBE growth of CdTe buffer layers on GaAs (211)B, including several sets of strained CdZnTe/CdTe superlattice-based (SLS) dislocation filtering layers (DFLs). Each DFL layer consists of five periods of $Cd_{1-x}Zn_xTe$/CdTe with thicknesses of ~13 nm/~11 nm, respectively; (b) comparison of x-values as determined by XRD and estimated from the MBE growth conditions for the CdTe DFL buffer layers.

single $Cd_{1-y}Zn_yTe$ layer having a same total thickness of $h = 5d_1 + 4d_2$, and having a mean Zn content of $y = xd_1/(d_1 + d_2)$, and therefore, a mean misfit strain of $\varepsilon = yf_l$, where $d_1 = 13$ nm and $d_2 = 11$ nm are the thicknesses of the $Cd_{1-x}Zn_xTe$ layers and CdTe layers, respectively, and $f_l = -5.8\%$ is the lattice-mismatch of ZnTe/CdTe. Hence, the DFL has a strain-thickness product of $\varepsilon h = 3.1x$ nm, and the constraint condition determines a limited Zn content range of $0.08 < x < 0.30$ for our DFL design, assuming the critical strain-thickness product of $\varepsilon_c h_c = 0.24$ nm for the $Cd_{1-x}Zn_xTe$ system. As mentioned previously, a high-quality CdZnTe buffer is challenging to grow, and layers that are too thick and/or have more Zn content may increase the risk of Zn segregation. However, since the CdZnTe SLS layers here are only of the order of 10-nm thick, subsequent CdTe layers should smoothen out any irregularities in the CdZnTe surfaces before other crystal phases nucleate.

Growing a DFL with a specific x-value for the CdZnTe layers (i.e., desired strain) is essential for achieving high dislocation filtering efficiency and repeatable device performance. Under Te-rich growth conditions, the Zn content (x) in the CdZnTe layers can be estimated using the relationship $x = P_{Zn}/(P_{Zn} + k\, g_{ct})$ since $Cd_{1-x}Zn_xTe$ can be considered an alloy of CdTe and ZnTe, where P_{Zn} is the BEP of the Zn cell, g_{ct} is the growth rate of CdTe, and k is an adjustable parameter. Experimentally, the value $k = 2 \times 10^{-7}$ h μm^{-1} was obtained from calibration growths in our MBE system. During MBE growth, the BEP of the CdTe cell (P_{ct}) was fixed to be around 2×10^{-6} Torr, which corresponds to a growth rate of approximately 2 μm h^{-1}. Experimentally, we find that for growing $Cd_{1-x}Zn_xTe$ with $x < 0.2$, the Zn cell temperature (T_{Zn}) and the corresponding P_{Zn} need to be lower than ~260°C and 1×10^{-7} Torr which, however, is close to the practical background floor of the ion gauge used for BEP measurements in our Hg-containing MBE chamber. Fortunately, based on the relationship

$$P_{Zn} = 39617 e^{-14159/(T_{Zn}+273)} \tag{1}$$

fitted from the BEP data measured at higher temperatures of the Zn cell, we can extrapolate P_{Zn} for relatively low Zn cell temperatures and can thus grow $Cd_{1-x}Zn_xTe$ with specific x values < 0.2. This approach was found to be very useful, especially for growing $Cd_{1-x}Zn_xTe$ with low x value when the BEP gauge appeared to be influenced by the Hg background pressure after Hg-related growth. As evident from Fig. 1b, x-values estimated from the MBE growth conditions based on the calculated P_{Zn} and measured g_{ct} are in good agreement with x values determined by XRD measurement.

Dislocation Filtering Effect

The dislocation filtering effect in the CdTe DFL buffer layers grown on GaAs substrates has been confirmed by several characterization methods, including TEM, EPD analysis, and PL. Although TEM can visualize individual defects, it is destructive and time-consuming. Moreover, it has a lower detection limit of TDD of 10^7–10^8 cm^{-2} due to the relatively small volume being analyzed. Moreover, TEM specimen preparation of HgCdTe structures can be challenging due to the fragile nature of the material compared with other semiconductors.[37] Defect decoration based on chemical

etching, known as EPD etching, has been developed for several semiconductors, including HgCdTe.[35,38] EPD etching is also destructive but significantly extends the lower detection limit. For example, 1 min of Everson etching for CdTe (211) B surface (etching rate ~ 1.9 μm min^{-1}) decorates TDs by forming larger surface etch pits (~ 2 μm in size, as shown in Fig. 3), which can be easily detected and counted at lower magnification, thereby facilitating the inspection of larger sample areas. The surface morphology/roughness/polarity and orientation of epitaxial films may affect the validity of EPD measurements.[39] The EPD values were obtained from CdTe buffer layers with reasonable surface quality and regular (211)B orientation, as confirmed by XRD measurements. The chemical etching rate for the $Cd_{1-x}Zn_xTe$/CdTe DFL region is a factor of 2–5 times (depending on the x value) lower than that for CdTe, and the defect decoration effect appears to be less pronounced if the etching stops within the DFL region, causing difficulties in characterizing TD evolution within the CdTe layer between each DFL set. To control the depth at which the etching is terminated, most CdTe DFL buffer layers were grown with a sandwich structure of ~ 5-μm CdTe bottom layer/DFL region (~ 2.8-μm thick for five sets of DFL)/~ 5-μm CdTe top layer.

In this study, TEM was used to examine the CdTe buffer layer structure, in particular, the interactions between TD and each SLS-based DFL. Figure 2a and d present bright-field (BF) TEM images of CdTe DFL buffer layers grown on GaSb (211)B and GaAs (211)B, respectively, showing clear and sharp interfaces between the DFL and the surrounding CdTe layers. Figure 2b shows a higher-magnification TEM image of the CdTe/GaSb interface, where it can be observed that a TD starts from the interface and propagates through the 2-μm-thick CdTe bottom layer. The observation of an almost dislocation-free top CdTe layer suggests an efficient reduction of TDD by the SLS DFL regions. The dislocation filtering effect of the SLS DFL is demonstrated

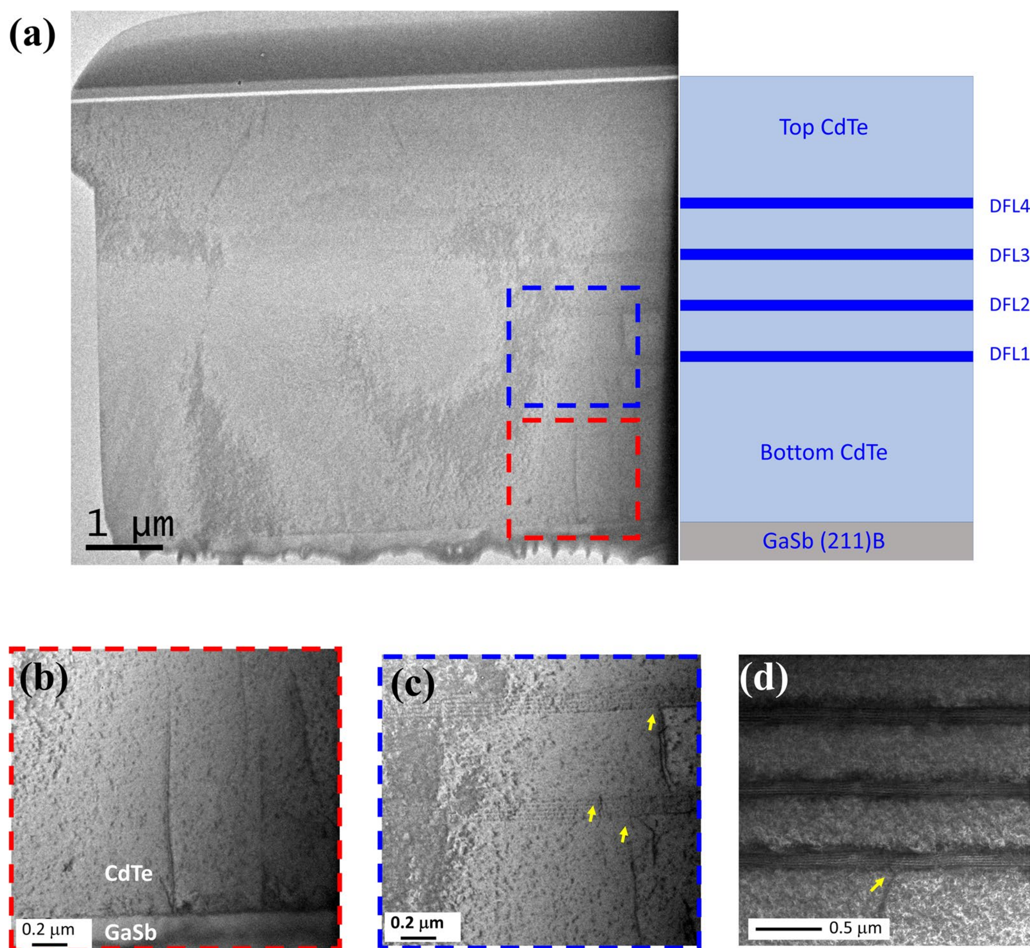

Fig. 2 (a) Cross-sectional bright-field TEM images of 5.2-μm-thick CdTe buffer layer containing four sets of CdZnTe/CdTe DFLs on GaSb (211)B substrate; (b) enlarged TEM image of the CdTe/GaSb substrate interface where threading dislocations originate from; and (c) enlarged TEM image of the DFLs, showing evidence for dislocation filtering (indicated by yellow arrows); (d) TEM image of CdTe DFL buffer layer grown on GaAs (211)B substrate (Color figure online).

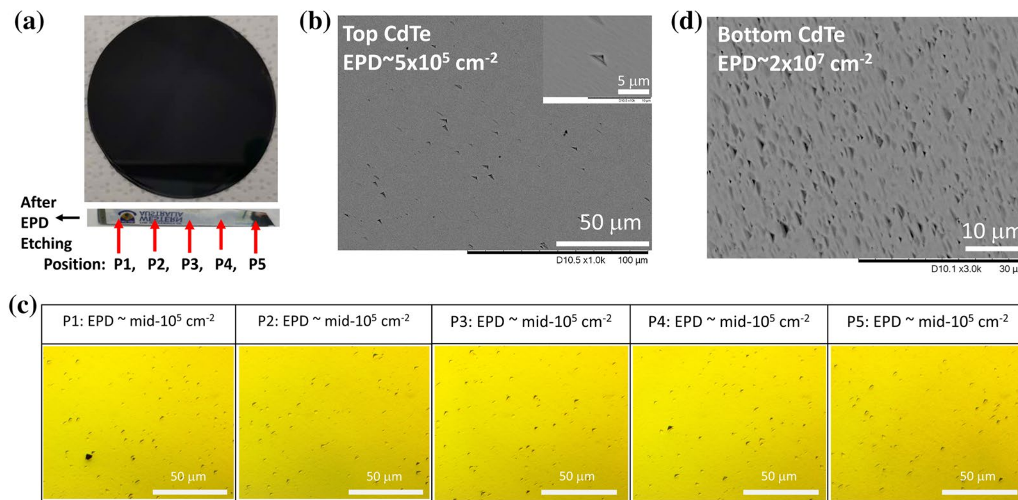

Fig. 3 (a) Photograph of 2-inch MBE-grown CdTe buffer/GaAs (211) B with DFL annealed at 320°C; (b) SEM image for EPD measurement of top CdTe layer; (c) optical images for EPD measurement across five points along the wafer diameter; (d) SEM image for EPD measurement for the bottom CdTe surface after EPD etching.

in the enlarged TEM image in Fig. 2c. In addition to sharp SLS interfaces, apparent TD re-direction and termination at the CdZnTe/CdTe hetero-interfaces are evident, as indicated by the yellow arrows. Similar dislocation filtering has been observed in a CdTe DFL buffer grown on GaAs (211)B substrate with similar DFL design (Fig. 2d).

Figure 3a shows an MBE-grown 2-inch CdTe buffer/GaAs (211)B sample, having a uniform and mirror-like surface to the naked eye. In order to examine the material quality of the top CdTe layer across the whole wafer, EPD measurements were performed for a bar cut along the diameter, which still shows a shiny surface after EPD etching, as visible in Fig. 3a. Figure 3b shows a representative SEM image for the etched surface, and the EPD is determined to be approximately 5×10^5 cm^{-2}, agreeing with values determined from optical imaging. As demonstrated in Fig. 3c, the EPD values measured along the wafer diameter are all in the range of mid-10^5 cm^{-2}, indicating excellent material uniformity across the entire 2-inch wafer. In contrast, as evident from Fig. 3d, the EPD of the bottom CdTe layer is around 2×10^7 cm^{-2}, suggesting that the DFL reduces the dislocation density by a factor of 40. The EPD level achieved for the top CdTe layer is approaching the critical EPD level required for fabricating high-performance LWIR HgCdTe detectors.[15]

Figure 4a presents a representative cross-sectional SEM image of a cleaved CdTe DFL buffer layer. After EPD etching, as shown in Fig. 4b, five etch pits in series along the growth direction are visible, which are well separated by each DFL. This result is similar to observations of GaAlAs/GaAs heterojunctions, and is presumably related both to misfit dislocations and TDs present in the vicinity of heterogeneous interfaces.[40] As evident from Fig. 4c, the number of cross-sectional etch pits appears to decrease from bottom-to-top after each DFL, suggesting that each DFL acts as a barrier to TD propagation. It is interesting that the DFLs tend to act as agents to reveal the TD propagation path. Although the precise relationship between TD and the observed cross-sectional etch pits is unclear at this stage, it would appear that etch pits form preferentially within the CdTe space layers due to the presence of Zn in the DFL region, which leads to reduced Everson etching in the DFLs. Although the cross-sectional etch pits have been observed experimentally, it remains challenging to apply this approach for characterizing the TD evolution in CdTe DFL buffer layers since there are often only a few pits visible in the cross-sectional surface after EPD etching in most CdTe buffer layers examined.

As a quick and non-destructive approach, optical techniques such as PL have been widely used in developing optoelectronic devices. However, since these methods are based on the generation/recombination and transport of charge carriers, their application for evaluating TDD present in a layer suffers from the presence of non-ideal surfaces, interfaces, and background impurities, which typically dominate the overall recombination velocity (therefore, PL intensity) and hence screen the impact of bulk TDD. Despite this drawback, a comparison of PL intensities for similar structures grown in the same batch of samples and/or within a short time interval is relevant to TDD measurements, since the MBE growth conditions in terms of background impurities and fluxes can presumably be assumed to be unchanged. To assess the material quality of the CdTe buffer layers grown, RT (room temperature) PL spectroscopy was undertaken for samples grown within the same MBE growth session. Figure 5a and b compare PL intensities of the CdTe buffer layers. Under the same excitation conditions as indicated by

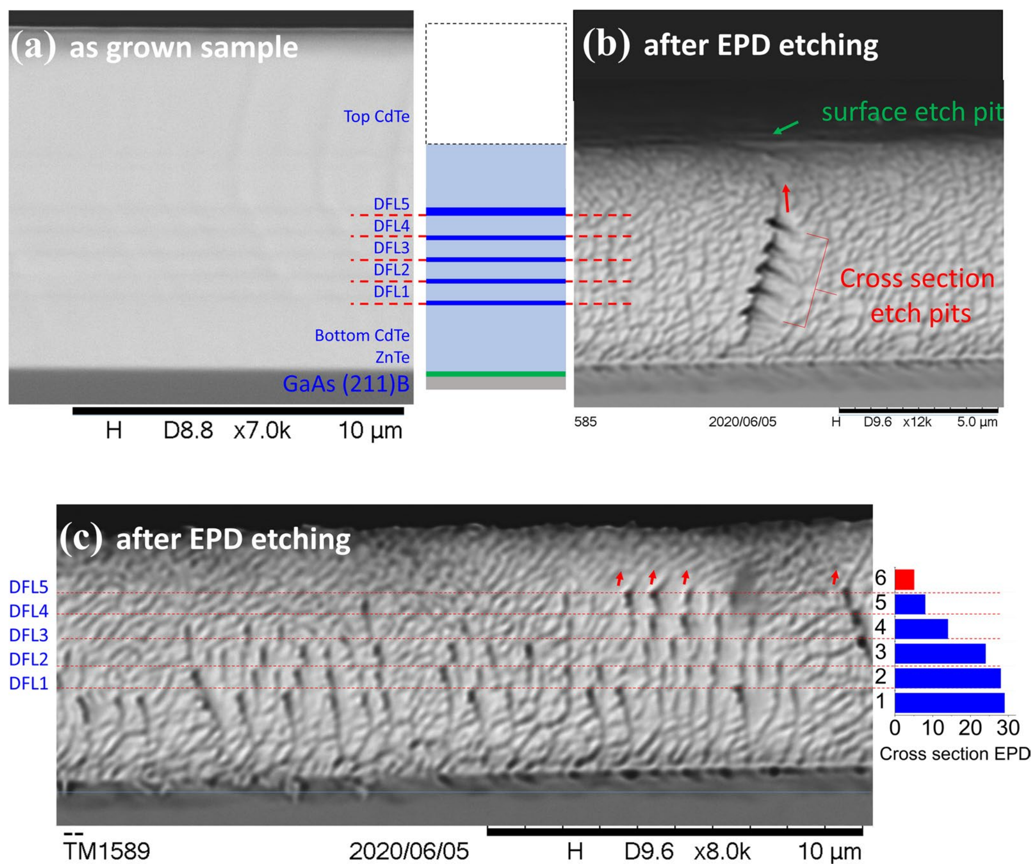

Fig. 4 (a) Cross-sectional SEM images of cleaved CdTe buffer layer with DFLs, and (b) after cross-sectional EPD etching. (c) Depth-dependence of cross-sectional EPD on the number of DFLs.

the inset in Fig. 5a, these PL intensities of the CdTe peak at around 1.5 eV are very well correlated with the EPD values in the range from low-10^7 to mid-10^5, suggesting that this optical method provides a fast and reliable non-destructive approach for evaluating the TDD for CdTe buffer layers with and without DFL. In contrast, as evident from Fig. 5b and c, a larger XRD FWHM does not necessarily imply higher TD density, as will be discussed in the "Impact of DFL Design on Material Properties of CdTe Buffer Layers" section.

Impact of DFL Design on Material Properties of CdTe Buffer Layers

Dislocation Filtering Efficiency

There are several parameters such as x value in $Cd_{1-x}Zn_xTe$ layers, CTA temperature, and the number of DFL, as summarized in Fig. 6, that affect the dislocation filtering efficiency (η) and, therefore, the final EPD value of the top CdTe layer. As shown in Fig. 6a, the EPD values of the bottom CdTe layer (EPD_b) and the top CdTe layer (EPD_t) in CdTe buffer layers with different DFL designs were measured, with the corresponding η as calculated by

$$\eta = (EPD_b - EPD_t)/EPD_b \quad (2)$$

and shown in Fig. 6b. In the case of buffer layers with five sets of DFL grown with CTA at 320°C, an optimal x range of $0.15 < x < 0.17$ is observed, which leads to a low EPD level ranging from mid-10^5 cm^{-2} to low-10^6 cm^{-2}, and the highest EPD filtering efficiency of ~98% within the Zn composition range of $0.08 < x < 0.27$ studied. When $x = 0.17$, samples with no thermal annealing as well as those that underwent annealing at the higher temperature of 360°C resulted in a relative higher EPD level of mid-10^6 cm^{-2} and corresponding η of 85% and 60%, respectively. It is generally assumed that moderate thermal annealing for DFL structures can further improve their efficiency of filtering defects due to the combined effect of increasing the mobility of defects and introducing thermal strain (ε_t) for more efficient defect annihilation.[41] The data in Fig. 6b suggests that in CdTe DFL buffer layers without CTA, the optimal x value in $Cd_{1-x}Zn_xTe$ is relatively high at around 0.23 ($\eta = 94\%$, EPD_t of 2×10^6 cm^{-2}). This is to be expected since higher x value, and therefore, more lattice-mismatch strain in the DFL, can compensate for the lack of benefits associated with CTA.

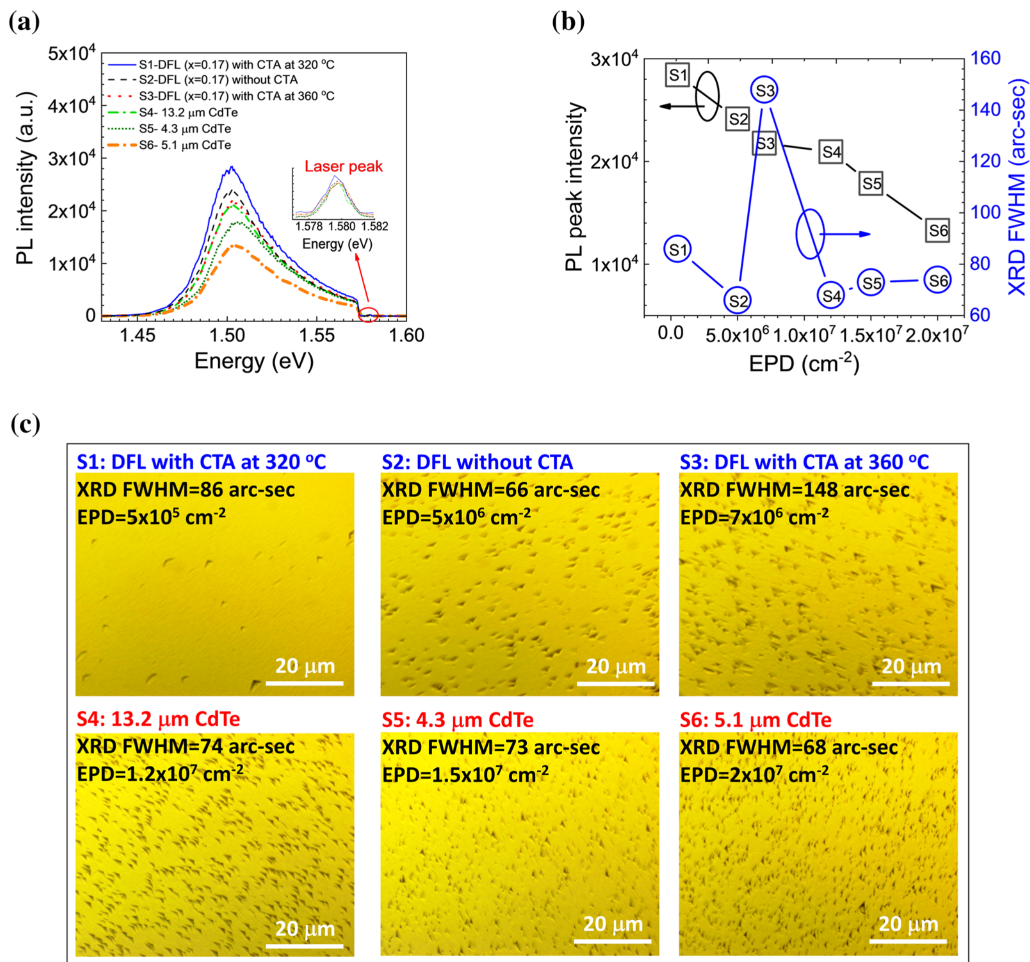

Fig. 5 (a) Room-temperature PL spectra of CdTe buffer layers with/without DFL. The inset shows that laser intensities are the same, indicating the same excitation conditions for all samples; (b) PL peak intensity and XRD FWHM plotted as a function of the measured EPD for different buffer layers; (c) optical images for EPD measurements on CdTe buffer layers after EPD etching. Sample numbers of "S1", "S2", "S3", "S4", "S5", "S6" are labeled for the CdTe buffer layers analyzed in the figure.

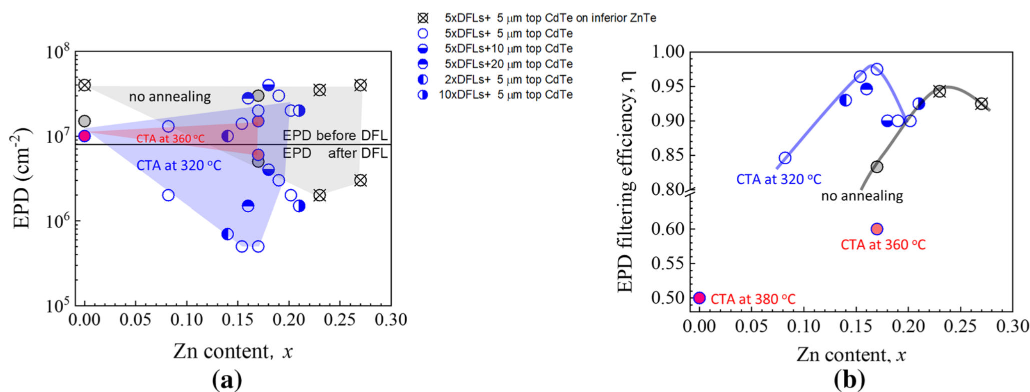

Fig. 6 (a) EPD values measured for the top CdTe and bottom CdTe layers for DFL buffer layers grown with different DFL designs and plotted as a function of Zn content (x), and (b) corresponding EPD filtering efficiency.

Excessive annealing can result in net surface evaporation of CdTe, surface roughening, Te deficiency related defects, and potential nucleation points for additional dislocations.[42] However, this is unlikely to occur for nearly relaxed CdTe when the CTA is carried out at temperatures below 400°C under Te overpressure. Experimentally, we found that the EPD of a CdTe/GaAs buffer without DFL can be reduced from 2×10^7 cm^{-2} to 1×10^7 cm^{-2} after introducing CTA at temperatures up to 380°C, corresponding to a TD reduction efficiency of ~50%. Furthermore, EPD reduction from low-10^7 cm^{-2} to mid-10^5 cm^{-2} was observed by other workers for CdTe/Si ($f_t = -92\%$) with 10 cycles of CTA at high temperatures up to ~500°C.[14] In this case, both additional Te and CdTe fluxes were supplied during the CTA process to prevent surface roughening/evaporation. Note that the EPD reported for CdTe/Ge ($f_t = 14\%$) and CdTe/GaAs ($f_t = 14\%$) with the use of CTA at ~400°C varied in the range of 10^6–10^7 cm^{-2}.[43,44] These values are relatively high compared to the best reported values for CdTe/Si, which may be explained by the differences in the thermal annealing temperature (ΔT) as well as f_t since $\varepsilon_t \propto f_t \Delta T$. Further comparisons of the effect of thermal mismatch in various HgCdTe/AS composite structures on their final EPD after CTA are worth investigating.[45]

Another factor that needs to be considered for the CTA process in CdTe DFL buffer layers is that $Cd_{1-x}Zn_xTe$ has a larger thermal expansion coefficient ($\alpha(x) = (4.7 + 3.63x) \times 10^{-6}$ K^{-1}) than CdTe ($f_t = 13\%$ for $Cd_{0.17}Zn_{0.83}Te$/CdTe).[46,47] Thus, additional tensile strain ε_t may be introduced in the CdZnTe layers when the buffer layers are cooled down from thermal annealing temperatures to room temperature (RT).[48] Between RT and typical growth/thermal annealing temperature, this difference in thermal expansion amounts to $\varepsilon_t = 1.8 \times 10^{-4}$ for DFL without annealing, $\varepsilon_t = 2.1 \times 10^{-4}$ for DFL annealed at 320°C, and $\varepsilon_t = 2.4 \times 10^{-4}$ for DFL annealed at 360°C, which are all nearly two orders of magnitude lower than the lattice-mismatch-induced strain of $\varepsilon = 1 \times 10^{-2}$ in a $Cd_{1-x}Zn_xTe$/CdTe DFL with $x = 0.17$. These results suggest that thermal mismatch plays a minor role in the dislocation reduction process for the CdTe DFL buffer layers on GaAs with CTA at the temperatures evaluated (< 380°C).

The above discussion suggests that strained CdZnTe layers in the DFL may be more sensitive to CTA, and thus the effect of excessive heating on the strained CdZnTe layers should be considered. It has been found in many lattice-mismatched systems, such as strained InGaAs/GaAs and strained SiGe/Ge, that annealing of the strained layers helps to generate misfit dislocations that relax the strain and reduce critical thickness.[49–51] Therefore, the decrease of dislocation filtering efficiency observed in the CdTe DFL buffer with CTA at 360°C could be attributed to thermal annealing-assisted misfit dislocation formation and strain relaxation/leakage in the CdZnTe layers. Further detailed control of the annealing temperature and/or annealing duration, as well as Te flux, could be effective in providing CdTe DFL buffers with EPD$_t$ < mid-10^5 cm^{-2}.[14] The CdTe DFL buffer layers demonstrate higher efficiency in TD reduction at much lower temperature CTA in comparison to conventional CdTe/AS, which may be beneficial in reducing the risk of structural damage during cooling with highly mismatched thermal expansion, such as CdTe/Si, as well as reducing the risk of Ga contamination in HgCdTe layers grown on GaAs substrates.[52]

As evident from Fig. 6b, other parameters such as thicknesses of the top and bottom CdTe layers and the number of DFLs, are also expected to affect the EPD$_t$ values. It is interesting that considerable EPD reduction can be achieved by using only two sets of DFL, providing much shorter processing times and thinner buffer layers compared with conventional CdTe buffer layers grown with complex CTA procedures. Moreover, the EPD$_t$ of CdTe DFL buffer layers with thicker top CdTe layer (> 10 μm) appears to be slightly larger than that with 5 μm, which may be related to lattice relaxation in the top CdTe layer. In principle, the thicknesses of the bottom CdTe as well as the top CdTe can be reduced for the subsequent growth of HgCdTe without affecting dislocation filtering, while improving the lattice matching for HgCdTe/CdTe, as will be discussed in the "Compressively Strained CdTe In-Plane Lattices In/Near the DFL Region" section.

DFL-Induced XRD FWHM Spread in CdTe Buffer Layers

EPD measurements are destructive, as discussed in the "Dislocation Filtering Effect" section, and therefore, have limited application as a screening technique for the manufacturing process. Simple, fast, and non-destructive techniques such as XRD have been used to screen MBE-grown HgCdTe epilayers in terms of dislocation density.[10] As evident from Fig. 7a, for previously reported MBE-grown HgCdTe data on lattice-matched CZT substrates, nearly lattice-matched CdTe substrates, and CdTe buffer/AS, all show the general trend that a decrease in EPD is associated with lower XRD FWHM.[4,18] Based on the frontier of the data (upper points of data envelope), we can establish an empirically numerical correlation

$$\rho = 10^{\left[-14.6+20.8\left(1-e^{-\frac{X_f}{11.3}}\right)+2\left(1-e^{-\frac{X_f}{104.5}}\right)\right]} \quad (3)$$

where ρ is EPD and X_f is XRD FWHM. As illustrated in Fig. 7a, the FWHM for a given value of EPD, as deduced from the empirical curve, is close to the lowest FWHM value, which is presumably dominated by the intrinsic dislocation density, while the spread in measured FWHM can

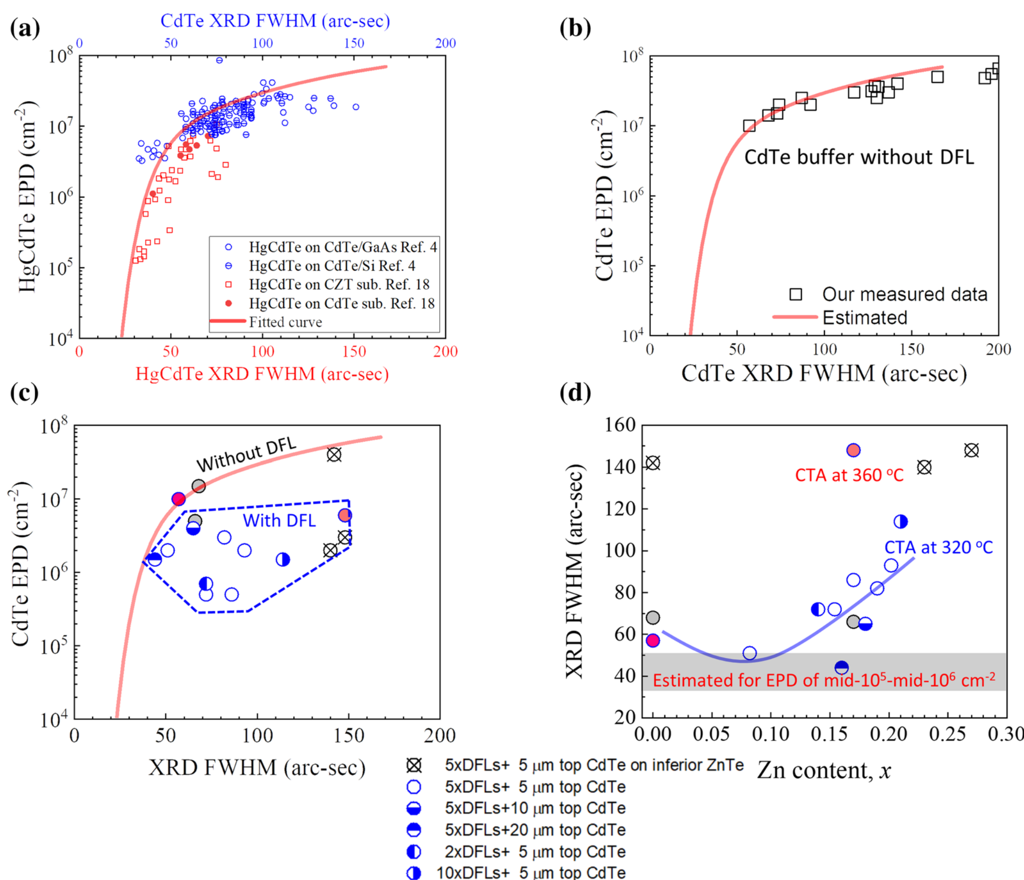

Fig. 7 (a) EPD of HgCdTe/CdTe/GaAs and HgCdTe/CdTe/Si grown at Teledyne,[4] plotted as a function of XRD FWHM of the underlying CdTe buffer layer. XRD FWHM versus EPD for MBE-grown HgCdTe epilayers on CdZnTe and CdTe substrates are also included.[18] The solid line was fitted to the frontier of these experimental data (upper envelope of data); (b) EPD of CdTe buffer layers/GaAs (211)B without DFL from the present study, plotted as a function of XRD FWHM and compared to the same fitted curve as in (a); (c) EPD of CdTe buffer layers/GaAs with DFL and some CdTe reference samples from the present study, plotted as a function of XRD FWHM and compared to the fitted curve as in (a), and (d) plotted as a function of Zn content.

be explained by other parameters such as residual strain and/or composition non-uniformity present in the HgCdTe films. From the difference between the curve and the data points in the lower envelope of the experimental data, it is evident that the spread is no larger than 15 arc-sec when the EPD value is in the low-10^6 cm^{-2} range or lower. For example, it appears that when EPD is 2×10^6 cm^{-2} or lower, the smallest FWHM estimated from the curve is 40 arc-sec, while the experimental FWHM is not larger than 55 arc-sec.

In order to examine this correlation, the experimental data from the present study are plotted in Fig. 7b, indicating that results for buffer layers without DFL are in good agreement with the fitted curve. The large FWHM and EPD (FWHM > 120 arc-sec, EPD ~ mid-10^7 cm^{-2}) are related to CdTe buffer layers grown with inferior ZnTe nucleation layers. With an optimal ZnTe, the FWHM and EPD are reduced to < 100 arc-sec and low-10^7 cm^{-2}, respectively, which can be further reduced to 57 arc-sec and ~ 1×10^7 cm^{-2} when CTA (380°C, 15 min) is applied. However, as shown in Fig. 7c, a much more extensive spread in FWHM values is observed for our CdTe DFL buffer layers. The EPD_t for the DFL buffer layers is in the range of mid-10^5 to mid-10^6, while the XRD FWHM is in the range of 42–150 arc-sec, which is much larger than the estimated range of 35–50 arc-sec based on the fitted curve from Fig. 7a. Hence, a more residual strain induced by the DFL is suspected to be present in the top CdTe layer of the DFL buffer layers compared to conventional HgCdTe layers. As discussed later, the FWHM spread originates from the compressive strain of the CdTe layers in/near the DFL region. In other words, the tensile-strained CdZnTe superlattice layers can modify the in-plane lattice of their neighboring CdTe superlattice layers and CdTe spacers such that they are compressively strained, thereby relieving their tensile strain.

The correlation between the FWHM spread and the strain related to the DFL buffer design has been investigated. Both the CdTe DFL buffer ($x = 0.16$) grown with the thickest top CdTe layer (~ 20 μm) and the CdTe DFL buffer grown

with the lowest Zn content of $x = 0.08$ (cap layer thickness ~5 μm) have small XRD FWHM that are very close to the expected range of 40–50 arc-sec predicted from the fitted curve. This result corresponds with the fact that a thick top CdTe layer will lead to a relaxed CdTe lattice, and low Zn content will result in lower strain. As evident from Fig. 7d, an FWHM broadening rate of 3 ± 1 arc-sec/Zn% is deduced for the DFL buffer layers grown with a 5-μm top CdTe layer and CTA at 320°C. Therefore, the FWHM of 86 arc-sec measured in the CdTe DFL buffer ($x = 0.17$, EPD $= 5 \times 10^5$ cm^{-2}) is expected to reduce to 35 arc-sec when the top layer thickness increases from 5 μm to 20 μm or thicker, which is consistent with the estimated value from the FWHM-EPD curve. As evident from Fig. 7b, other parameters such as the thickness of the top CdTe layer, DFL annealing temperature, the number of DFLs, and thickness of the bottom CdTe layer, are also suspected to affect the FWHM values.

Compressively Strained CdTe In-Plane Lattices In/Near the DFL Region

To further understand the abnormal spread in FWHM values for the DFL buffer layers, the thickness-dependent FWHM, EPD, and PL peak energy in the CdTe DFL buffer layers was measured. As evident from Fig. 8a, no apparent EPD ∝1/thickness behavior is observed in the bottom CdTe layer. In contrast, a continuous reduction of the number dislocations during the DFL growth is observed in the CdTe DFL buffer layers (Fig. 8a and e).

As evident from Fig. 8b, the dependence of XRD FWHM on thickness within the CdTe DFL buffer, where an "M" trend is observed near the DFL region, is quite different from that observed for the conventional CdTe buffer layer/AS in which the XRD FWHM decreases monotonically with increasing CdTe thickness.[9] Most FWHM broadening

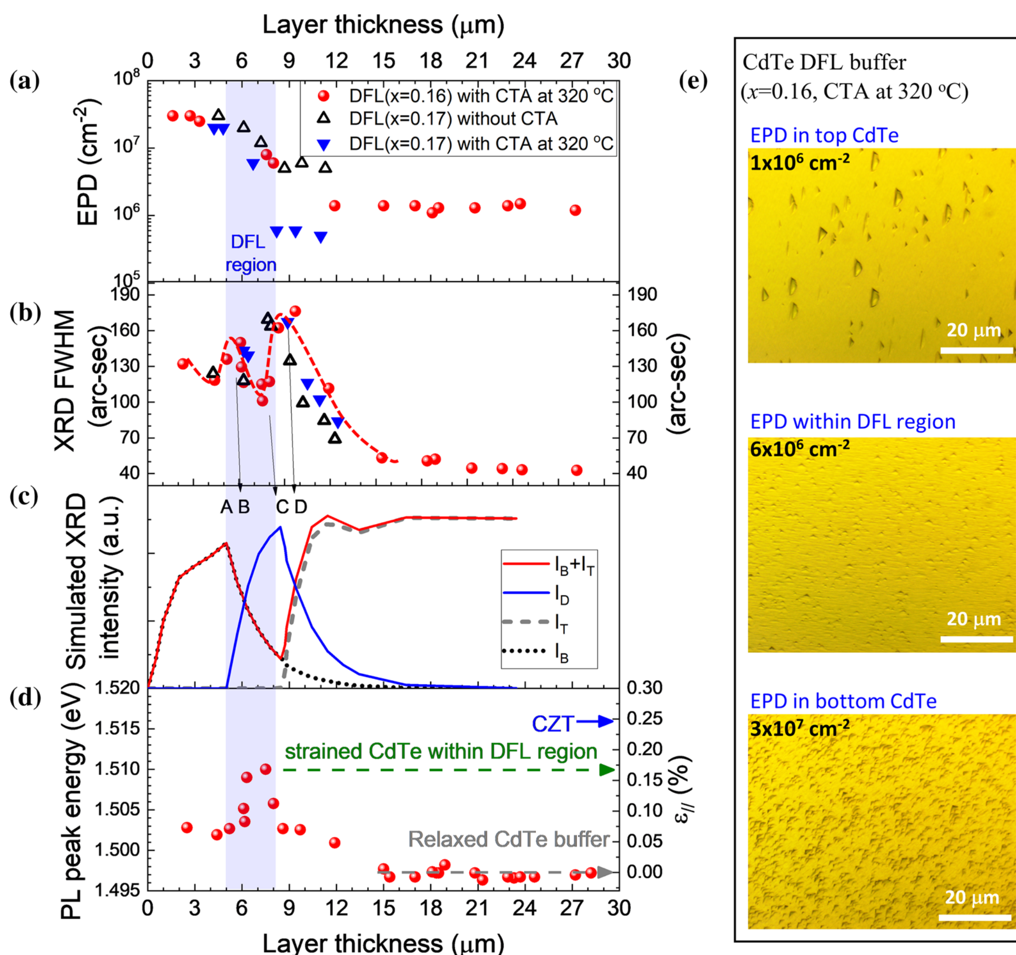

Fig. 8 Measured (a) EPD, (b) XRD FWHM, (c) simulated XRD intensity, and (d) PL peak energy plotted as a function of thickness measured for CdTe DFL buffer layers. The DFL buffer with $x = 0.17$ was grown with 2-μm-thick bottom CdTe layer/five sets of DFL/5-μm-thick top CdTe layer, and the DFL buffer with $x = 0.16$ was grown with 5-μm-thick bottom CdTe layer/five sets of DFL/20-μm-thick top CdTe layer. In order to align the DFL region for these buffer layers, the data from the DFL buffer layers with $x = 0.17$ were offset horizontally. (e) Optical images of EPD measurements at different depths of the CdTe DFL buffer grown with $x = 0.16$ and CTA at 320°C.

is related to mosaic misorientation due to screw and mixed TDs as well as residual strain field due to lattice-mismatched growth.[53] As the layer grows, the remainder of the strain is relaxed by forming dislocations, which results in reduction of the TD density and FWHM with increasing CdTe thickness. By using XRD measurements, it has previously been found for CdTe layers grown on Ge (211)B with in situ annealing after growth at 400°C for 1 h, that the stress of 100 MPa and in-plane strain of 1.5×10^{-3} observed for thin CdTe layers with thickness of ~25 nm relaxed rapidly in thicker CdTe layers and became negligible beyond 1 μm.[54] Even so, the stress near the heterogeneous interface contributes to FWHM broadening for layers with thickness up to 5 μm due to the considerable XRD sampling depth.

To interpret the "M" relationship observed in Fig. 8b for the DFL sample, we modeled the XRD intensity of the (422) plane. For simplicity, it was assumed that both the bottom and top CdTe were fully relaxed. The XRD FWHM broadening was modeled based on the assumption that the slightly strained CdTe in/near the DFL region and the remaining CdTe layers contribute equally to the total XRD intensity. Thus, the dynamics of the XRD for the (422) plane from the buffer layer with DFL involves a continuum description of XRD intensities contributed by the bottom CdTe layer (I_B), CdTe in/near the DFL region (I_D), and the top CdTe (I_T). The results for I_D, I_T, I_B as a function of layer thickness in a CdTe DFL buffer are plotted in Fig. 8c. The total XRD intensity ($I_D + I_T + I_B$) increases as the layer thickness increases up to 10 μm and then maintains an almost constant value, indicating an average XRD sampling depth of 10 μm. It is noted that the positions in the modeled data where $I_D = I_T + I_B$ in Fig. 8c tend to correlate well with the positions (B, D) where the local maxima of XRD FWHM occur experimentally, as shown in Fig. 8b. In addition, the local minimum of XRD FWHM observed within the DFL region in Fig. 8b can be attributed to position "C" where the XRD intensity is mainly due to CdTe in/near the DFL region, i.e., I_D, as shown in Fig. 8c. After the growth of 7-μm or more of the top CdTe, I_D becomes negligible, and the XRD FWHM is mainly determined by the relaxed top CdTe layer with reduced EPD, resulting in the smallest FWHM of 42 arc-sec.

In order to assess the strain of the CdTe buffer layers, RT PL spectra were taken for samples at different etch depths. The energies of the PL peaks obtained in this way are compared in Fig. 8d as a function of thickness. For depth-profiling positions in which the etched surface is close to the top DFL, a blueshift of PL peak is observed, which presumably originates from stress in the CdTe layers rather than from quantum-confinement effects induced by the CdZnTe layers. This is because no relaxed CdTe-related PL peak was observed when changing the working distance of the confocal microscopy PL system, and because the PL lineshape remains the same as that observed for other bulk CdTe layers, as shown in Fig. 5a. Considering that the strain-induced blueshift coefficient of the CdTe band gap is about 1.7×10^{-2} eV GPa^{-1},[55] the compressive stress in the CdTe around the DFL region ($x = 0.16$, CTA at 320°C) was estimated to be around 100 MPa, which corresponds to a compressive in-plane lattice strain of around 1.5×10^{-3}. The stress falls off rapidly with distance from the DFL region (steeper than that of the XRD FWHM because the sampling depth of the 785 nm laser beam is less than 1 μm), then decreases gradually, and eventually becomes negligible for the top CdTe layer beyond 7 μm from the top DFL.

To confirm the lattice strain present in the CdTe DFL buffer layers, XRD RSM measurements of asymmetric (333) and symmetric (422) planes were undertaken for the CdTe DFL buffer having the structure of 2-μm bottom CdTe/5 sets of DFL/5-μm top CdTe ($x = 0.17$, CTA at 320°C, $EPD_t = 5 \times 10^5$ cm^{-2}). The measured reciprocal lattice points of the (422) planes are shown in Fig. 9a. The dominant bottom peak corresponds to the relaxed top CdTe layer and the nearby sub-peak with lower intensity corresponds to the CdTe layers in/near the DFL region, as indicated in Fig. 9b. The two upper features consist of several interference fringes corresponding to the strained CdZnTe/CdTe DFLs, indicating that sharp CdZnTe/CdTe interfaces have been achieved. The direction for the XRD ω scan for obtaining FWHM for the CdTe DFL buffer layer is also denoted in Fig. 9a and c, and the FWHM would broaden when the top CdTe peak fades away with its thickness decreasing, corresponding with the observations in Fig. 8b.

Based on the RSM results, the extracted strain parameters for each layer in the CdTe DFL buffer are summarized in Table I. The mean in-plane compressive strain for the CdTe layers in/near the DFL region is determined to be 0.13%, which is in good agreement with the PL results shown in Fig. 8d. The in-plane lattice of the CdTe layers near the DFL region is compressively strained and slightly tilted with respect to the top CdTe layer, leading to a spread in XRD FWHM but better in-plane lattice-matching with HgCdTe, in comparison to conventional single-layer CdTe buffer layers/AS. The tilt direction towards the $[11\bar{1}]$ crystallographic direction and the small tilt angle of 0.05° is due to the small in-plane lattice-mismatch between the compressively strained CdTe in/near the DFL region and the relaxed CdTe top layer.[56]

Although an EPD of ~10^5 cm^{-2} has been reported for CdTe/Si with the use of optimal CTA, the typical EPD values for HgCdTe/CdTe/AS, and even for HgCdTe layers grown on CdTe substrates, appear to be limited to the level of low-10^6 cm^{-2}.[17,18] Defects in the HgCdTe originate not only from defects in the CdTe buffer but also from the small in-plane lattice-mismatch between HgCdTe/CdTe ($f_1 = 0.25\%$). The EPD saturation at a level of low-10^6 cm^{-2} is believed to be due to the formation of sessile (immobile)

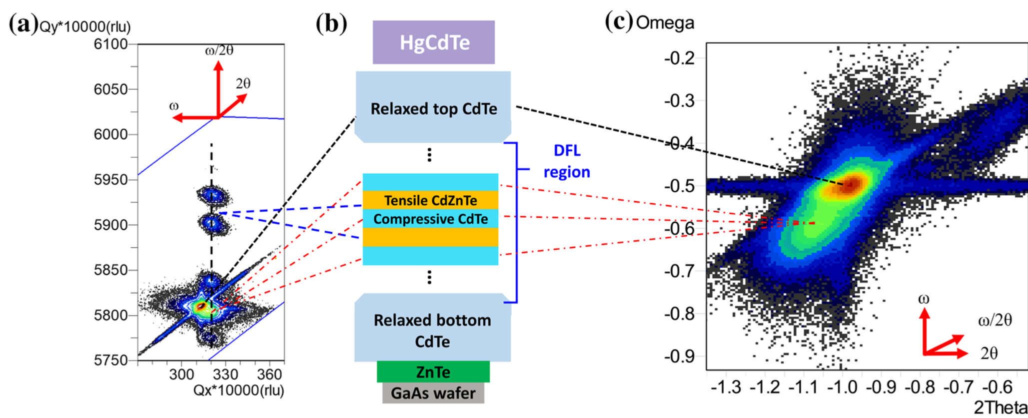

Fig. 9 (a) XRD RSM map for the (422) plane and (c) the corresponding ω–2θ map measured for the DFL buffer grown with $x = 0.17$ and CTA at 320°C; (b) a schematic representation of CdTe DFL buffer structure on GaAs. The difference in width of each layer represents the difference (not to scale) in in-plane lattice constant. The in-plane lattice relaxes far from the DFL region for the sufficiently thick bottom and top CdTe layers. In/near the DFL region, the in-plane lattice of CdTe is compressively strained, resulting in better lattice-matching with HgCdTe than a relaxed CdTe layer. For the symmetric (422) RSM in (a), the peak separation in the Q_x direction indicates the presence of lattice tilting, whereas the peak separation in the Q_y direction indicates the presence of lattice mismatch.

Table I Summary of XRD results of the CdTe DFL buffer shown in Fig. 9

Layers in CdTe DFL buffer	α (°)	$m_{\perp}$ (%)	$m_{\parallel}$ (%)
Top CdTe layer	3.087	−0.01	0.04
CdTe in/near DFL region	3.137	0.13	−0.13
CdZnTe layers	3.099	−2.26	−0.11
CdZnTe layers with respect to CdTe in/near DFL region	0.025	−2.16	<0.01

α, $m_{\perp}$, and $m_{\parallel}$ represent the lattice tilting, the out-of-plane lattice strain, and the in-plane lattice strain, respectively.

dislocations from the fusion of glissile dislocations since it cannot be further reduced by thermal annealing of the HgCdTe layers. In face-centered-cubic semiconductors, such as III–V GaAs and II–VI CdTe, there is an exchange between mobile and sessile TDs that leads to a balance between the two defect populations, allowing continued TDD reduction.[24] Therefore, it can be expected that DFL provides a promising approach towards high-quality heteroepitaxy of HgCdTe on large lattice-mismatched substrates having lower dislocation density and smaller lattice-mismatch for future applications in next-generation IR detectors.

Conclusions

This study has demonstrated a dramatic improvement in the material quality of CdTe buffer layers grown on 2-inch lattice-mismatched GaAs (211)B substrates by using CdZnTe/CdTe SLS-based DFL. The DFL approach has reduced the routine EPD from low-10^7 cm^{-2} to low-10^6 cm^{-2}, and 5×10^5 cm^{-2} for the best layer, which approaches the critical EPD level required for fabricating high-performance LWIR HgCdTe detectors. The dislocation filtering efficiency is found to be highly dependent on the balance between stress and thermal annealing, and even lower EPD can be expected with further optimization of the DFL structural design, growth parameters, and annealing conditions. Moreover, the in-plane lattice of the CdTe layers near the DFL region is found to be compressively strained, leading to a spread in XRD FWHM but better in-plane lattice-matching with HgCdTe, in comparison to conventional single-layer CdTe buffers/AS.

More work needs to be done to investigate the impact of growth and annealing temperature, and the thickness and composition of superlattice layers on the final EPD of the top HgCdTe layer, and their impact on HgCdTe device performance. The beneficial effects of CdZnTe/CdTe DFL are not limited to GaAs and GaSb substrates but could also be applied to the growth of CdTe buffer layers on other alternative substrates such as Si and Ge, which would be a feasible approach for growing high-quality CdTe and HgCdTe materials on large-area alternative substrates for next-generation HgCdTe IR detectors and imaging FPAs with lower cost and larger array format. We anticipate that this technology and associated IR applications will continue to expand in the foreseeable future.

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Conflict of interest The authors declare that they have no conflict of interest.

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References

1. M. Reddy, J.M. Peterson, T. Vang, J.A. Franklin, M.F. Vilela, K. Olsson, E.A. Patten, W.A. Radford, J.W. Bangs, and L. Melkonian, *J. Electron. Mater.* 40, 1706 (2011).
2. M.F. Vilela, K.R. Olsson, E.M. Norton, J.M. Peterson, K. Rybnicek, D.R. Rhiger, C.W. Fulk, J.W. Bangs, D.D. Lofgreen, and S.M. Johnson, *J. Electron. Mater.* 42, 3231 (2013).
3. M.F. Vilela, D.D. Lofgreen, E.P.G. Smith, M.D. Newton, G.M. Venzor, J.M. Peterson, J.J. Franklin, M. Reddy, Y. Thai, E.A. Patten, S.M. Johnson, and M.Z. Tidrow, *J. Electron. Mater.* 37, 1465 (2008).
4. M. Carmody, A. Yulius, D. Edwall, D. Lee, E. Piquette, R. Jacobs, D. Benson, A. Stoltz, J. Markunas, and A. Almeida, *J. Electron. Mater.* 41, 2719 (2012).
5. W. Lei, R.J. Gu, J. Antoszewski, J. Dell, G. Neusser, M. Sieger, B. Mizaikoff, and L. Faraone, *J. Electron. Mater.* 44, 3180 (2015).
6. W. Lei, Y.L. Ren, I. Madni, and L. Faraone, *Infrared Phys. Technol.* 92, 96 (2018).
7. W. Lei, J. Antoszewski, and L. Faraone, *Appl. Phys. Rev.* 2, 041303 (2015).
8. A. Rogalski, J. Antoszewski, and L. Faraone, *J. Appl. Phys.* 105, 091101 (2009).
9. L. He, L. Chen, Y. Wu, X.L. Fu, Y.Z. Wang, J. Wu, M.F. Yu, J.R. Yang, R.J. Ding, and X.N. Hu, *J. Cryst. Growth* 301, 268 (2007).
10. J.P. Zanatta, G. Badano, P. Ballet, C. Largeron, J. Baylet, O. Gravrand, J. Rothman, P. Castelein, J.P. Chamonal, A. Million, G. Destefanis, S. Mibord, E. Brochier, and P. Costa, *J. Electron. Mater.* 35, 1231 (2006).
11. S.H. Shin, J.M. Arias, D.D. Edwall, M. Zandian, J.G. Pasko, and R.E. DeWames, *J. Vac. Sci. Technol. B* 10, 1492 (1992).
12. H. Figgemeier, M. Bruder, K.-M. Mahlein, R. Wollrab, and J. Ziegler, *J. Electron. Mater.* 32, 588 (2003).
13. J.J. Kim, R.N. Jacobs, L.A. Almeida, M. Jaime-Vasquez, C. Nozaki, and D.J. Smith, *J. Electron. Mater.* 42, 3142 (2013).
14. Y. Chen, S. Farrell, G. Brill, P. Wijewarnasuriya, and N. Dhar, *J. Cryst. Growth* 310, 5303 (2008).
15. S.M. Johnson, D.R. Rhiger, J.P. Rosbeck, J.M. Peterson, S.M. Taylor, and M.E. Boyd, *J. Vac. Sci. Technol. B* 10, 1499 (1992).
16. J. He, P. Wang, Q. Li, F. Wang, Y. Gu, C. Shen, L. Chen, P. Martyniuk, A. Rogalski, X. Chen, W. Lu, and W. Hu, *IEEE Trans. Electron Devices* 67, 2001 (2020).
17. J.D. Benson, L.O. Bubulac, P.J. Smith, R.N. Jacobs, J.K. Markunas, M. Jaime-Vasquez, L.A. Almeida, A. Stoltz, J.M. Arias, G. Brill, Y. Chen, P.S. Wijewarnasuriya, S. Farrell, and U. Lee, *J. Electron. Mater.* 41, 2971 (2012).
18. J.-P. Faurie, *Prog. Cryst. Growth Charact. Mater.* 29, 85 (1994).
19. Y.P. Chen, G. Brill, and N.K. Dhar, *J. Cryst. Growth* 252, 270 (2003).
20. P.S. Wijewarnasuriya, Y.P. Chen, G. Brill, B. Zandi, and N.K. Dhar, *IEEE Trans. Electron Devices* 57, 782 (2010).
21. Y.P. Chen, G. Brill, E.M. Campo, T. Hierl, J.C.M. Hwang, and N.K. Dhar, *J. Electron. Mater.* 33, 498 (2004).
22. P.L. Gourley, T.J. Drummond, and B.L. Doyle, *Appl. Phys. Lett.* 49, 1101 (1986).
23. R. Fischer, D. Neuman, H. Zabel, H. Morkoc, C. Choi, and N. Otsuka, *Appl. Phys. Lett.* 48, 1223 (1986).
24. T. Ward, A.M. Sánchez, M. Tang, J. Wu, H. Liu, D.J. Dunstan, and R. Beanland, *J. Appl. Phys.* 116, 063508 (2014).
25. M. Yamaguchi, *J. Mater. Res.* 6, 376 (1991).
26. S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S.N. Elliott, A. Sobiesierski, A.J. Seeds, and I. Ross, *Nat. Photonics* 10, 307 (2016).
27. Z. Mi and Y.-L. Chang, *J. Nanophotonics* 3, 031602 (2009).
28. J. Yang, P. Bhattacharya, and Z. Mi, *IEEE Trans. Electron Devices* 54, 2849 (2007).
29. H.-M. Wang, J.-P. Zhang, C.-Q. Chen, Q. Fareed, J.-W. Yang, and M.A. Khan, *Appl. Phys. Lett.* 81, 604 (2002).
30. J.L. Reno, S. Chadda, and K. Malloy, *Appl. Phys. Lett.* 63, 1827 (1993).
31. A. Tanaka, Y. Masa, S. Seto, and T. Kawasaki, *J. Cryst. Growth* 94, 166 (1989).
32. W.W. Pan, R.J. Gu, Z.K. Zhang, J.L. Liu, W. Lei, and L. Faraone, *J. Electron. Mater.* 49, 6983 (2020).
33. W. Lei, R.J. Gu, J. Antoszewski, J. Dell, and L. Faraone, *J. Electron. Mater.* 43, 2788 (2014).
34. A. Million, N.K. Dhar, and J.H. Dinan, *J. Cryst. Growth* 159, 76 (1996).
35. W.J. Everson, C.K. Ard, J.L. Sepich, B.E. Dean, G.T. Neugebauer, and H.F. Schaake, *J. Electron. Mater.* 24, 505 (1995).
36. G. MacPherson and P.J. Goodhew, *J. Appl. Phys.* 80, 6706 (1996).
37. A.G. Cullis, N.G. Chew, and J.L. Hutchison, *Ultramicroscopy* 17, 203 (1985).
38. J.D. Benson, P.J. Smith, R.N. Jacobs, J.K. Markunas, M. Jaime-Vasquez, L.A. Almeida, A. Stoltz, L.O. Bubulac, M. Groenert, and P.S. Wijewarnasuriya, *J. Electron. Mater.* 38, 1771 (2009).
39. L. Burgess, F.J. Kumar, and J. Mackenzie, *J. Electron. Mater.* 44, 3277 (2015).
40. W. Tseng, S. Prokes, B. Wilkins, M. Fatemi, and A. Christou, *Mater. Lett.* 6, 281 (1988).
41. W. Li, S. Chen, M. Tang, J. Wu, R. Hogg, A. Seeds, H. Liu, and I. Ross, *J. Appl. Phys.* 123, 215303 (2018).
42. R.F. Brebrick, *J. Electrochem. Soc.* 118, 2014 (1971).
43. G. Badano, I.C. Robin, B. Amstatt, F. Gemain, and X. Baudry, *J. Cryst. Growth* 312, 1721 (2010).
44. E. Bakali, Y. Selamet, and E. Tarhan, *J. Electron. Mater.* 47, 4780 (2018).

45. R.N. Jacobs, C. Nozaki, L.A. Almeida, M. Jaime-Vasquez, C. Lennon, J.K. Markunas, D. Benson, P. Smith, W.F. Zhao, and D.J. Smith, *J. Electron. Mater.* 41, 2707 (2012).
46. M.G. Williams, R.D. Tomlinson, and M.J. Hampshire, *Solid State Commun.* 7, 1831 (1969).
47. H.P. Singh and B. Dayal, *Acta Cryst. A* 26, 363 (1970).
48. L.S. Dang, J. Cibert, Y. Gobil, K. Saminadayar, and S. Tatarenko, *Appl. Phys. Lett.* 55, 235 (1989).
49. R.H. Miles, T.C. McGill, P.P. Chow, D.C. Johnson, R.J. Hauenstein, C.W. Nieh, and M.D. Strathman, *Appl. Phys. Lett.* 52, 916 (1988).
50. S.C. Jain and W. Hayes, *Semicond. Sci. Technol.* 6, 547 (1991).
51. J. Zou, D.J.H. Cockayne, and B.F. Usher, *J. Appl. Phys.* 73, 619 (1993).
52. G.W. Blackmore, E.D. Jones, J.B. Mullin, and N.M. Stewart, *Mater. Sci. Eng. B* 16, 186 (1993).
53. J.E. Ayers, T. Kujofsa, P. Rago, and J. Raphael, *Heteroepitaxy of Semiconductors: Theory, Growth, and Characterization* (Boca Raton: CRC Press, 2016).
54. G. Badano, P. Gergaud, I.C. Robin, X. Baudry, B. Amstatt, and F. Gemain, *J. Electron. Mater.* 39, 908 (2010).
55. M.S. Boley, R.J. Thomas, M. Chandrasekhar, H.R. Chandrasekhar, A.K. Ramdas, M. Kobayashi, and R.L. Gunshor, *J. Appl. Phys.* 74, 4136 (1993).
56. F.J. Yu, *J. Cryst. Growth* 204, 35 (1999).

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