Journal of Electronic Materials (2022) 51:923–937
https://doi.org/10.1007/s11664-021-09384-8

REVIEW ARTICLE

A Review on a Negative Capacitance Field-Effect Transistor for Low-Power Applications

Malvika[1] · Bijit Choudhuri[1] · Kavicharan Mummaneni[1]

Received: 9 August 2021 / Accepted: 1 December 2021 / Published online: 5 January 2022

Abstract

Low-power devices have emerged as a topic of intense research investigations as the need for a better and more comfortable life requirement has escalated to small and efficient devices. The current (I)-voltage (V) characteristics of metal oxide semiconductor field-effect transistors (MOSFET) are mainly defined through the source-to-drain barrier that is regulated by the gate voltage (V_G). The Boltzmann statistics reveal that at least 60 mV is required at the gate of a conventional MOSFET to raise the current magnitude by an order. As a result of this limitation, the threshold voltage of the present-day MOSFETs cannot be less than around 0.3 V for an I_{ON} to I_{OFF} ratio of five decades. This has created a fundamental bottleneck in voltage downscaling that increases power consumption in billions of transistors in modern IC. To resolve this issue, the concept of incorporating ferroelectric material in the MOSFET gate stack came into existence. It allows the amplification of internal voltage in the vicinity of the MOSFET channel, which can achieve a small sub-threshold swing (SS) to reduce the device's power consumption. Ferroelectric FETs are evolving devices with a vast ability to replace conventional MOSFETs by steep switching characteristics. Both negative capacitance field effect transistors (NCFET) and ferroelectric FETs (Fe-FETs) have a similar structure, but they are distinct in function. A Fe-FET has hysteretic behavior, whereas a NCFET does not. This article aims to conduct a comprehensive survey of the state-of-art of NCFET and Fe-FET for improving device parameters such as ON/OFF ratio, SS, and hysteresis. Furthermore, comparative analysis of various NCFET structures for low power applications has been discussed and summarized based on various characteristics from its inception.

Keywords Ferroelectric · NCFET · sub-threshold swing (SS) · hysteresis · Fe-FET · current ON/OFF ratio

Introduction

Motivation

Through the increasing advancement of technology, the requirement for smaller and more powerful tools has increased for a smarter and simpler life. According to an observation by Gordon Moore in 1966, every 2 years, the number of transistors in an IC (integrated circuit) doubles, which is significant in accelerating the scaling trend of transistors. The scaling trend of MOS was driven by this need for more integrated and efficient circuits. The channel length of MOS is reduced to shrink MOS into smaller units, resulting in decreased power per switching event and improvement in density. Still, it also causes undesirable changes in system properties such as various short-channel effects such as drain-induced barrier lowering and punch through, surface scattering, velocity saturation, impact ionization, and hot electron effect.[1]

Over the last five decades, CMOS technology scaling has driven the electronics industry to achieve more features and has provided a dense and fast integration.[2] In almost every system, the need for more performance and integration has accelerated scaling trends. Therefore, today's transistors occupy less than 1% space and are 20 times faster than the transistor developed five decades ago.[3] The power density and overall power consumption of the chips have also increased along with this. Similarly, the various parameters of the VLSI design such as gate dielectric constant,

✉ Malvika
malvikathakur16@gmail.com

Bijit Choudhuri
bijitchoudhuri@ece.nits.ac.in

Kavicharan Mummaneni
kavicharan@ece.nits.ac.in

[1] Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam, India

supply voltage, device leakage current have significantly been modified to achieve the desired performance of the integrated circuits. CMOS became the leading technology for integrated circuits because it can be scaled down to offer higher performance and smaller dimensions.

As per Moore's law, the downscaling of channel length is accompanied by a shrink in oxide thickness, introducing a hindrance for further scaling. The voltage supply, and transistor dimensions need to be scaled down linearly to accommodate dense integration of transistors.[4] Reduced transistor sizes can be defined by the basic electromagnetism equations, which causes a decrease in capacitance, resulting in increased thermal noise (defined by Nyquist). As a result, the probability of bit-flipping is increased, which decreases the overall reliability. According to Dennard scaling rules,[1] scaling down device dimensions reduces capacitance values and lowers overall power consumption. However, according to the scaling laws, the supply voltage V_{DD} could not be scaled at the same pace considering the delay, showing itself as a constraint in achieving high-speed, low-power devices.[5] This is because carriers in the source and drain regions of the MOSFET are controlled by Boltzmann statistics which restrict the rate of increase in drain current with respect to gate-source voltage to 60 mV/decade and, therefore, prevent further lowering of V_{DD} and overall power consumption.

Background

For a conventional MOSFET, the drain current (I_D) of the device is assumed to be negligible if the gate-to-source voltage is lower than the threshold voltage ($V_{GS} < V_T$). When $V_{GS} < V_T$, the drain current decreases exponentially, resulting in OFF-state current or sub-threshold current. The slope of sub-threshold current can be presented as $d(V_G)/d\log(I_D)$ where V_G and I_D are gate voltage and drain current, respectively. Analytically, sub-threshold swing (SS) is represented as

$$SS = \frac{d(V_G)}{d\log(I_D)} = \left(\frac{KT}{q}\ln 10\right)\left(1 + \frac{C_D}{C_{OX}}\right) \quad (1)$$

where C_D is the channel depletion capacitance. At room temperature, SS is defined as

$$SS = \left(60 \times 10^{-3}\right)\left(1 + \frac{C_D}{C_{OX}}\right) \quad (2)$$

Theoretically, if $C_D << Cox$, SS will be 60 mV/decade;[1] however, SS must be steeper to attain high performance. However, the smaller the ratio of the currents at $V_{GS} = V_T$ and $V_{GS} = 0$ or the I_{ON}/I_{OFF}, the greater the leakage current. Consequently, the current ratio must be as high as possible for a high-performance chip, and the sub-threshold slope must be steeper, which can be a solution for the situation. Different transport mechanisms can be implemented to solve this problem, such as impact ionization, tunneling, and positive feedback, essentially by amplifying the gate voltage. Also, different types of doping and structure lower the effect of random dopant fluctuation.[6] Recently, transistors with novel transport and switching mechanisms such as nano-electromechanical FET (NEMFET), resistive gate FET,[7–9] impact ionization of metal oxide semiconductor (I-MOS),[10,11] FET tunnelling [12,13] and negative capacitance FET (NCFET) are being investigated extensively to achieve SS below the Boltzmann limit. Since MOS is engineered to be ON at V_T, the immense value of sub-threshold current results in device performance reliability issues.

Nevertheless, if the supply voltage is not scaled the same as the thickness of the oxide, its electric field will increase. This inconsistency in supply voltage scaling results in the gradual degradation of the oxide layer and dielectric breakdown.[14] As a result, the gate oxide layer thickness cannot be scaled down significantly for an extended period of reliable operation. A severe constraint in resistive FET is hysteresis behavior. Further, the device will be in an ON-state for the reverse sweep until a reset operation is performed at $V_G<0$.

In NEMFET, an abrupt SS is achieved, but operation speed and reliability are limited due to the mechanical movement of the gate. I-MOS have very quick switching, but still it is unlikely for practical applications due to the following two reasons. First, there is a very high breakdown voltage and drain voltage. In addition, hot-carrier degradation of oxides becomes a severe issue due to a high lateral electric field. Furthermore, a complicated fabrication process and low reliability limit the practical application of TFET and I-MOS devices. Among the devices mentioned above, NCFET has attracted much interest because it can achieve steep SS by a voltage amplification mechanism without losing the drive current shown in Fig. 1. High ON-state current along with the suppressed OFF-state current and low power dissipation are its additional advantages. Compared with other sub-60 mV/decade devices, NCFETs possess a simple structure, more compatible fabrication techniques, and excellent working performance such as a steep sub-threshold swing (SS), high ON/OFF ratio, and adjustable hysteresis. Because of the above-listed reasons, the NCFET is a good remedy for the problem faced by TFET, NEMFET, I-MOS, and resistive gate FET.

In this review article, we have discussed the physics of various NCFET types of devices and observed how doping could lead to significant changes in their properties. Also, we have elaborated on how structural modification can result in efficiency enhancement. After making all the studies, we have summarized the results of different structures in a table. In addition, outcomes based on the various related reports, negative capacitance (NC) devices are categorized according

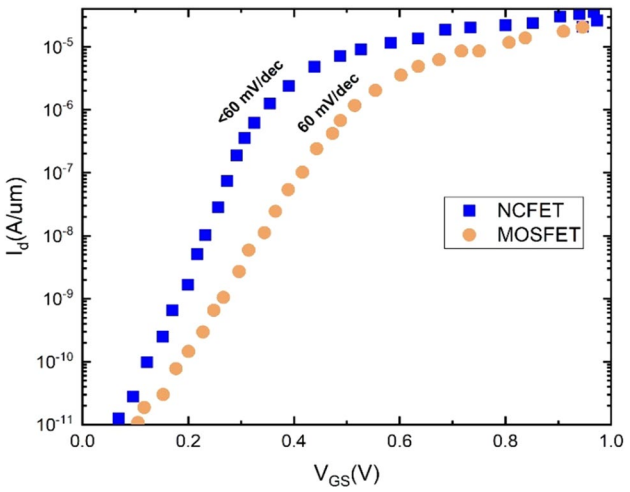

Fig. 1 Steep slope of MOSFET and NCFET.

to constraints such as devices for low sub-threshold slope, high ON current, negligible hysteresis, and improved SS, application-specific devices. Considering the above parameters, the MOSFET can be replaced by a promising substitute in terms of NCFET for ultra-low power, high speed, and cost-effective circuits. In addition, NCFET has yielded better results in several applications such as high-gain inverters, ultra-low power devices, internet of things (IoT), memories, biomedical devices, radio frequency (RF) sensing, analog circuits, and filters.

This article is structured as follows: "Working Principle of NCFET" elaborates on the working principle of NCFET and the physics of ferroelectric FET. "Different NC Devices" explores the systematic analysis of different NCFET devices. "Comparison of Fe-FET and NCFET" discusses the comparison of Fe-FET and NCFET, followed by a summarized comparison table. Finally, "Conclusion" lists the challenges in the practical implementation of NCFET and the conclusion of the article.

Working Principle of NCFET

Datta and Salahuddin[15] proposed a new idea of using a ferroelectric as an oxide material which makes $C_{ox} < 0$ and can result in a SS < 60mV/decade. Capacitance is the inverse of the double derivative of energy with charge. The negative capacitance mechanism of NCFET is depicted in Fig. 2. Ferroelectric polarization points upward when biasing is zero and inverts when the gate voltage exceeds coercive field (E_c), as presented in Fig. 2a and b. The curvature around charge (Q)=0 in the energy landscape of a ferroelectric is the opposite of an ordinary capacitor, i.e., an inverted parabola, as shown in Fig. 2c, and provides a negative capacitance. It depicts that a slight change in gate voltage causes a significant difference in the surface potential. However, obtaining the negative capacitance mainly relies upon the capability for driving ferroelectric material away from local minimum to non-equilibrium state.

Figure 2c and d shows the energy landscape variation before and after inversion of polarization. In the non-equilibrium state, the capacitance is negative, but the stage does not offer stability. The stability can be achieved by following any of the two steps in the CMOS gate stack: (1) providing a direct link between the ferroelectric and dielectric layer or (2) a ferroelectric-metal-dielectric connection.

In several studies,[16–18] it has been shown that the second approach results in a sudden amplification of the MOSFET's internal voltage (V_{int}) by the negative capacitance of the ferroelectric capacitor (C_{FE}<0) as can be observed in Fig. 4c. The total capacitance increases with negative C_{FE}, and the negative capacitance effect greatly amplifies V_{int}. Moreover, the introduction of series capacitance enhances the stability and the channel potential (ψ_s) on an internal node to adjust above the applied voltage.[19] The NCFET structures depicted in Fig. 4a and b are exactly similar to MOSFET, except an additional thin layer of ferroelectric material. The two primary structures of NCFET are metal-ferroelectric-insulator-semiconductor (MFIS) and metal-ferroelectric-metal-insulator-semiconductor (MFMIS). MFIS has an insulator layer that adds an advantage to ferroelectric materials such as barium titanate and lead zirconate titanate to be directly incorporated in the gate stack because of their imperfect crystal matching with germanium and silicon substrates. The MFMIS has an internal metal layer sandwiched between the insulator and ferroelectric, maintaining ferroelectric polarization uniformly along the channel because the potential difference between the top electrode and inner metal is uniform.

Recently, many research papers [20–22] have reported steep switching characteristics of NCFETs by integrating silicon and zirconium doped ferroelectric layer and replacing the transistor channel with the carbon nanotube. In a ferroelectric MOS capacitor, the polarization charge density and channel charge density must match to find the operating point. Thus, NCFET static operating point is figured out through the cross-point of polarization-electric field (P-E) curve and load line of channel charge shown in Fig. 3. If the curve has a single cross point in the NC region (the P-E curve has a negative slope), the ferroelectric MOS transistor acts as NCFET. The different structures and circuit models are shown in Fig. 4.

Kim et al. reported in[23] that the hysteresis in NCFETs occurs by the leakage current, which flows into the ferroelectric film through the dielectric layer, develops a ferroelectric depolarization field and causes charge traps. However, ferroelectric capacitor hysteresis can be avoided by modifying ferroelectric layer thickness. Here, static

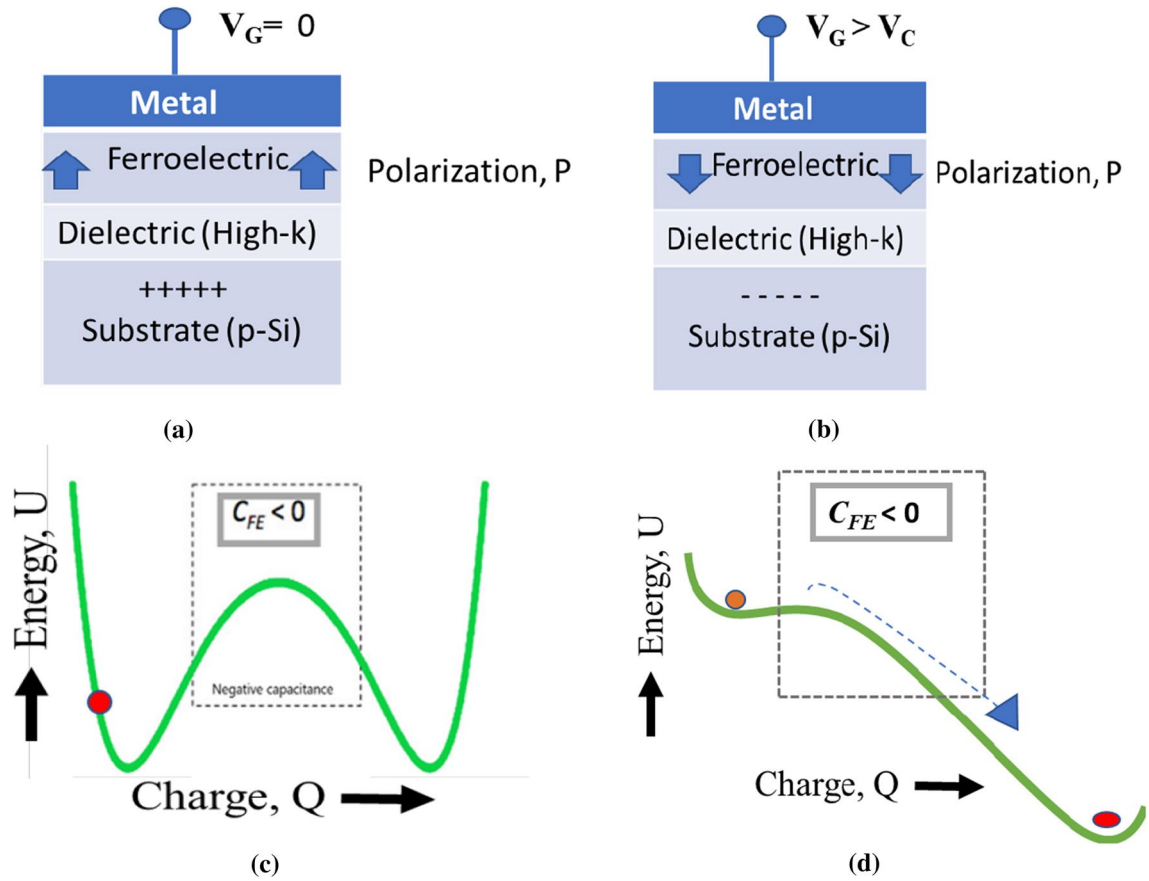

Fig. 2 Working operation of NCFET (a) Polarization under zero bias (b) Polarization when V_g is greater than coercive voltage (V_C) (c) Energy landscape of ferroelectric under no bias (d) Energy state after inversion of polarization.

operation points of reference materials parameters are optimized. These materials have thickness dependence on the ψ_s–V_g characteristics of the NCFET MOS capacitor with positive ferroelectric voltage. In the thickness range of 3-5 nm, ψ_s is amplified without hysteresis. This amplification is an inspiring outcome because the ferroelectric's thickness is only a few nanometers. In addition, only V_g of 0.2 V is required to amplify ψ_s (channel potential) that allows low supply voltage operation. It should be noted that the point of static operation will not be set appropriately for too high thickness, and the ψ_s-V_g curve will show a hysteresis effect.[24] Notwithstanding hysteresis, NCFET has excellent potential for operation under the SS limit. For negative capacitance,

$$\frac{d(V_g)}{d(\Psi s)} = \left(1 + \frac{C_S}{C_{OX}}\right) \tag{3}$$

which may be less than 1 if the C_{OX} is negative.[6] In the case of negative capacitance, C_{OX} is negative, which can cause SS to cross the theoretical limit of MOSFET less than 60mV/decade. The advantage of this process is that it enables the use of existing fabrication flow by only the inclusion of an oxide layer leading to a negative capacitance effect. The typical structure, circuit model, and equivalent capacitance of the substrate of the NCFET device are shown in Fig. 4.

A negative capacitance field-effect transistor (NCFET) introduces a thin ferroelectric material (FE) layer to an existing MOSFET gate oxide, as shown in Fig. 4a and b. The addition of ferroelectric material leads to a surface potential variation even for the slight change in the V_G. The key to negative capacitance is that it compensates the positive device capacitance such that the derived gate capacitance (C_G) can be written as,

$$C_G = \left(C_{FE^{-1}} + C_{MOS^{-1}}\right)^{-1} \tag{4}$$

results in sub-60mv/decade as understood from Fig. 4c and d. Fig. 4c and d are the capacitor equivalent model of NCFET, which represents the ferroelectric MOS capacitor as a series combination of channel capacitance and ferroelectric capacitance.

In an NCFET structure, the underlying MOSFET acts as a positive capacitance (C_{MOS}) (Fig. 4c), which can stabilize

the ferroelectric in the NC state if the total gate capacitance (Eq. 4) is positive. This condition states that $|C_{Fe}|$ must be greater than C_{MOS} to realize a stable NC state of the ferroelectric in NCFET. In addition, both the $|C_{Fe}|$ and C_{MOS} can be affected by the applied voltages. When the above condition is violated for any combination of gate voltage (V_G) and drain voltage (V_D), NCFETs become unstable, resulting in hysteresis in the electrical characteristics. To avoid such violation, the thickness of ferroelectric should be constrained because $|C_{Fe}|$ varies proportionally with the ferroelectric thickness (T_{Fe}). Additionally, $|C_{Fe}|$ also depends on the coercive field (E_c) and the ferroelectric's remnant polarization (P_r) values. The ferroelectric with a high remnant polarization (P_r) and low coercive field (E_c) leads to an increase in the value of $|C_{Fe}|$. This implies that the condition of no hysteresis ($|C_{Fe}| > C_{MOS}$) is always met across the operating voltage range. In addition, a low T_{fe}, high P_r, and low E_c reduces capacitance matching between C_{Fe} and C_{MOS}. The FE oxide interface has an internal voltage greater than V_G, such that the SS can be reduced below the 60 mV/decade (Boltzmann maximum limit) at 300K. As a result, as opposed to the classical transistor, we can have a larger current in the device for a smaller gate voltage.

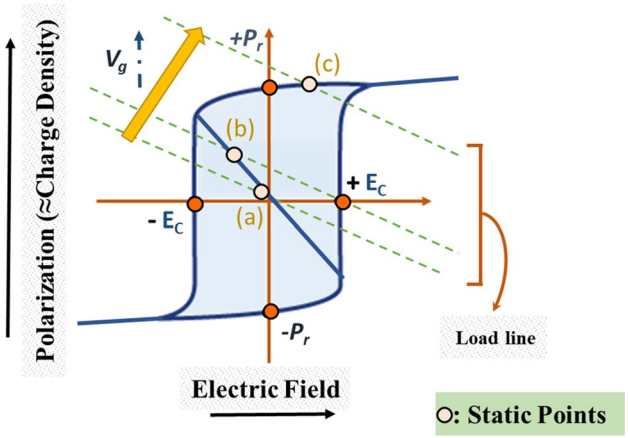

Fig. 3 Schematic of polarization-electric field and channel load line.

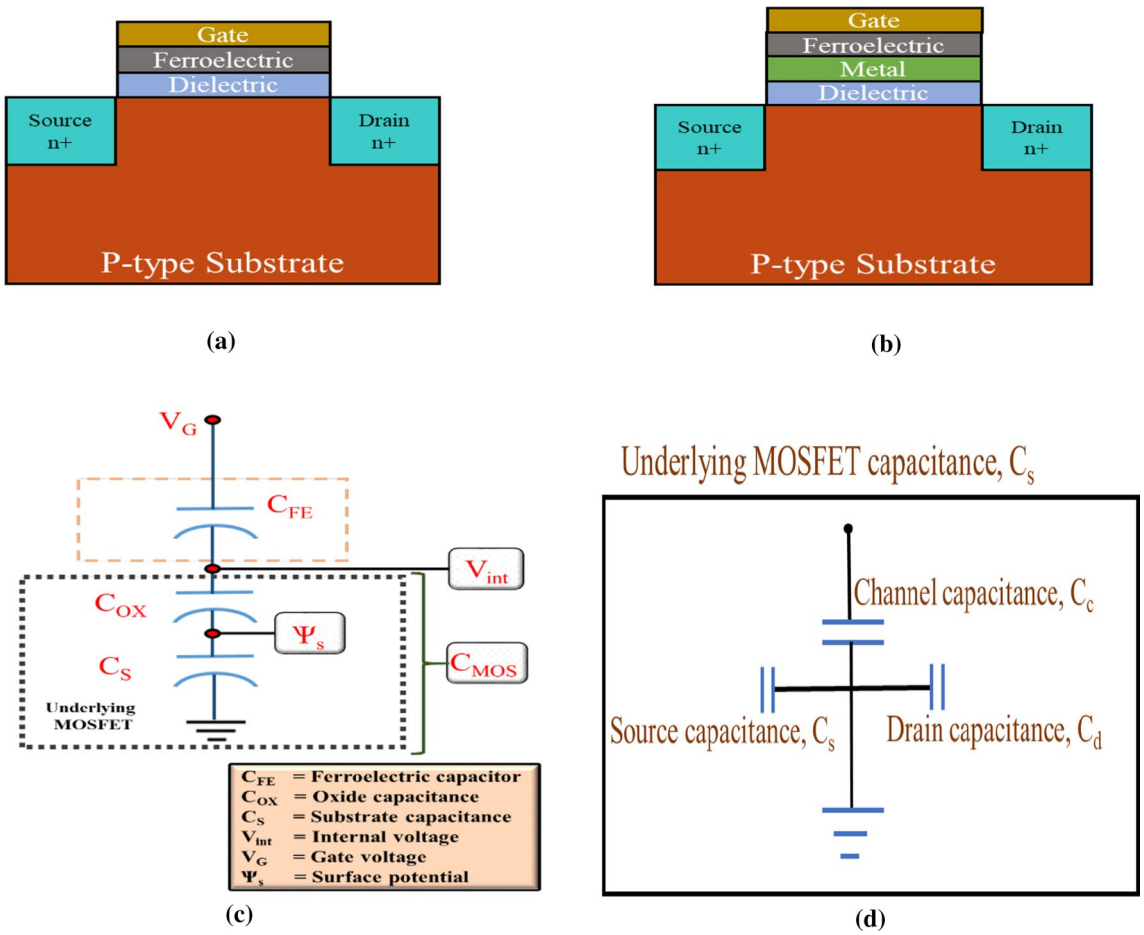

Fig. 4 Ferroelectric-based structure of NCFET: (a) MFIS, (b) MFMIS, (c) Circuit model of NCFET, and (d) Equivalent capacitance of substrate.

Physics of Ferroelectric FET

The ability of certain dielectrics to have a spontaneous polarization that can be reversed by an applied electric field (E) is termed ferroelectricity. A ferroelectric is an insulating device with two or more distinct stable states. It has distinct non-zero electrical polarisation without an electrical field called "spontaneous" polarization. For ferroelectric devices, the switching probability between these states in the presence of an applied electrical field (E) is greater than the coercive field that adjusts the relative energy of the states by coupling to the field to the polarization (P). Joseph Valasek discovered this property in the course of Rochelle salt studies in 1921.[25] Since then, there has been extensive study of materials that exhibit ferroelectric properties. Such materials show reversible and spontaneous polarization even when there is no external electric field. Electric polarization in ferroelectric materials occurs spontaneously due to phase transition at a critical temperature known as Curie temperature, T_c, without any external electric field. The crystal undergoes a phase transition from the ordered phase to the disordered phase at and below Curie temperature. Above the Curie temperature, materials are polarized under the electric field by the change in transition. Hence, the ferroelectric materials polarize spontaneously below the Curie temperature.

One of the critical characteristics of ferroelectric material is hysteresis. In hysteresis, all dipoles are pointed in specific directions, and these regions are known as domains. In the absence of an electric field, the net polarization is equal to zero due to random orientations of domains. However, dipole moments align themselves along the electric field by rotation under the influence of an applied electric field, thus forming a region with a net dipole moment oriented in a single direction. With the removal of the electric field, these created domains do not disappear. These irreversible processes of polarization result in hysteresis in material characteristics, as illustrated in Fig. 5. P-E hysteresis is not a sufficient condition for a ferroelectric material. Trapping phenomenon or leakage currents,[26] surface polarization can also result in hysteresis loop detection.

It can be observed that small displacements in weak electrical fields are reversible. Furthermore, remnant polarization (P_r) refers to the polarization value when an electric field is zero. The strength of the electric field required to bring the polarization back to zero is known as the coercive field (E_C). The threshold electrical field must be higher than the coercive field to alter the state of a ferroelectric device. If the electric field is applied in the same direction as the previous applied electric field, there will be no switching, and the charge will remain the same. The minimum electric field must be larger than the coercive field (E_c) for changing the state of the ferroelectric device. Unlike ferroelectrics, where the dielectric permittivity decreases with the electric field, the dielectric properties of antiferroelectric (AFE) materials can be improved at a high field due to the electric field-induced transition from an antiferroelectric state to a ferroelectric one. AFE materials exhibit low coercive fields and dielectric losses (at low field), as well as a high saturated polarization.

Until now, many researchers have focused on ferroelectric materials such as strontium bismuth tantalite (SBT) and lead zirconate titanate (PZT)[27,28] because of their dielectric, ferroelectric properties, leakage current characteristics, and long polarization retention. However, these materials show unstable ferroelectric behavior at thin film morphology, and they are also incompatible with standard IC processing technology. Hence, the discovery of hafnium oxide (HfO_2)-based dielectrics yields the potential to overcome these limitations. HfO_2 is preferred due to its high dielectric constant (~20), large band gap (~5 eV), large conduction band offset (1.5eV), and thermal stability. Ferroelectricity is observed in thin HfO_2 film without generating a large leakage current because of its wide band gap. Several studies show that controlling crystalline phases of HfO_2 thin film can lead to ferroelectricity in HfO_2, making it an attractive element. In addition, as a gate dielectric, this material is compatible with current IC technology. Dopants such as yttrium,[29,30] silicon,[31–35] and aluminum[36] have been used to cause ferroelectricity in doped HfO_2. Silicon-doped hafnium dioxide (Si: HfO_2) exhibit favorable results with a stronger coercive field (1 MV/cm versus 50 kV/cm for PZT/SBT) and a low dielectric constant (~30 versus 200-300 for PZT/SBT)[33] and is successfully incorporated into Fe-FET devices.[26]

Different NC Devices

The property of ferroelectricity was first observed in the 1920s, but the negative capacitance theory in ferroelectric material is more recent. McKee et al. suggested that incremental change in capacitance beyond classical limits could

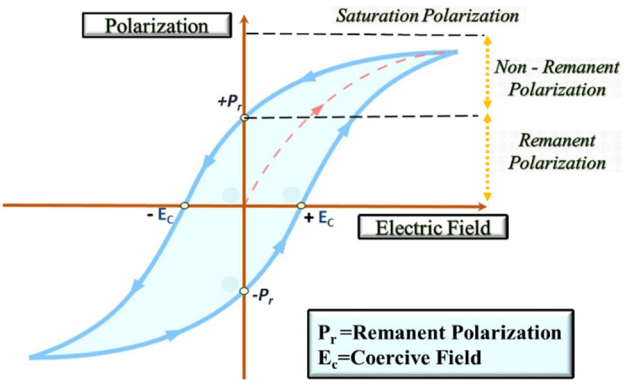

Fig. 5 Variation of polarization with electric field.

generate novel super capacitance structures.[37] The significant developments of NCFET structures are shown below in Fig. 6 and further discussed in the upcoming section.

Devices for Low Sub-threshold Slope

The NCFET became a promising candidate to achieve SS less than 60 mV/decade at room temperature. Many researchers tried to lower the Boltzmann limit by proposing structural and materials modification. Initially, in 2008 Salahuddin et al. reported that the SS could be below the fundamental limit by using ferroelectric material as a gate insulator in MOSFET.[15] Later, Khan and his research group explained the impact of negative capacitance in the nanoscale ferroelectric dielectric heterostructure in 2011.[38] They used a ferroelectric bi-layer $Pb(Zr_{0.2}Ti_{0.8})O_3$ and a dielectric material $SrTiO_3$. In,[39] hysteretic switching together with a sub-kT/q steep slope (13 mV/decade at 300K) in MOSFET with $PbZr_{0.52}Ti_{0.48}O_3$ is experimentally demonstrated as a FE gate insulator, integrated as a buffer interlayer on a silicon (si) channel with a non-perovskite high-k dielectric (HfO_2). The abrupt transition is independent of the bias drain. In addition, sub-kT/q switching is noticed for the first time due to FE negative capacitance in the strong inversion (I_d = 100 µA/µm) instead of low currents. Steep switching in strong inversion gives a significant consistency point with the assumptions of the Landau–Devonshire approach and the Landau–Khalatnikov equation.[40–46] An experimental investigation of the negative capacitance FinFET device revealed that the length of source/drain (L_{ext}) extension affects the hysteresis window. It was observed that an increase in L_{ext} decreases hystersis. The same device exhibited a 0.48 V hysteresis window with an ON/OFF current ratio of approximately 10^7 by controlling L_{ext}. Additionally, a sub-20 mV/decade SS_{avg} expected to counter the Boltzmann limit was experimentally verified versus a FinFET baseline with an SS_{avg} of approximately 105 mV/decade.[47]

Various ferroelectric materials such as BFO, SBT, and PZT exhibit compatibility with CMOS process technology; for example, the ferroelectric layer thickness should be less than 10 nm to be accepted in the current CMOS gate stack. Thus, a new sub-10 nm thick FE material compatible with CMOS, such as doped Hf-based FE material, can be incorporated in CMOS design. In,[48] a sub-10 nm thick HfZrO capacitor-based NC FinFET exhibited a steep switching feature compared to baseline FinFET. The NC FinFET's minimum SS was ~36 mV/decade at room temperature, which implies that the internal voltage is amplified due to the NC effect of the Hf-based ferroelectric layer. Rahman et al. reported the inclusion of Si-doped HfO_2 as ferroelectric material in NCFET to achieve a lower SS of 30 mV/decade, which was much lower than the regular MOSFET device.[49] Similarly, the use of multi-layer ferroelectric material achieved an excellent matching for the entire operating gate voltage range. The degree of improvement depends on the capacitance between the FE layer (C_{FE}) and the underlying MOS transistor (C_{MOS}). The technique of using multi-layer ferroelectric proposed in[50] provides better SS and leads to a lower power supply (V_{DD}) than the single-layer NCFET.

In 2013, Yeung with his colleagues proposed a new concept of incorporating an ultrathin body (UTB) structure in NCFET to suppress the short channel effects, thus significantly reducing the power loss.[51] Moreover, using a 1 nm Si body as an example, they demonstrated that NCFET possesses no hysteresis in ultra-thin body configuration. This non-hysteretic NCFET can achieve I_{ON}=250 A/µm, I_{OFF}=10 pA/µm at 0.3 V V_{DD} and 21 mV/decade swing from I_d of 10 pA to 10 µA per micron without considering mobility enhancement by strain. A 1.8 nm Zr-doped HfO_2 gate oxide layer was deposited upon the FDSOI wafer, and this device exhibited hysteresis-free operation.[52] Compared with

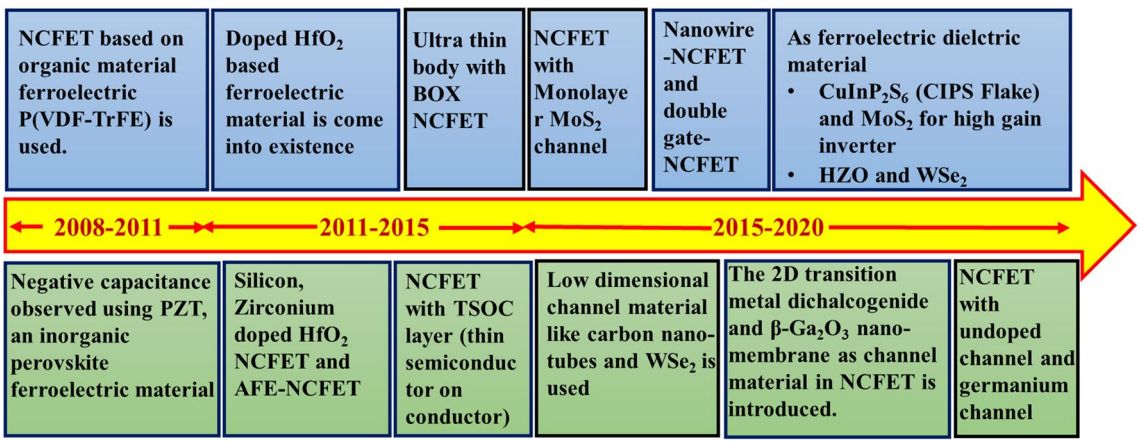

Fig. 6 Major developments of NCFET, highlighting different structures, channel doping, and ferroelectric material.

a crystalline HfO_2 gate oxide-based device, the Zr-doped HfO_2 device showed a 10X reduction in the OFF current (I_{OFF}) and 20 mV/decade steeper SS. On the other hand, this NCFET provided a more significant ON current at constant V_{DD}, at matched $I_{OFF.}$

Alternative Channel Material for Lowering SS

Recently, some functional 1D and 2D materials have been introduced in the channel of various NCFET-based devices. These materials possess some specific features, which dominate the performance of these devices. Some of the important details of different materials have been discussed below and their comparison is represented in tabular form (Table I). An exciting category of these materials is transition metal dichalcogenides (TMDCs) which are two-dimensional van der Waals materials. Their general chemical formula is MX_2, in which M is a transition metal (such as molybdenum (Mo) or tungsten (W)) and X is a chalcogen (such as selenium (Se), sulphur (S), or tellurium (Te)). The metal layer is sandwiched between two chalcogenide layers in bulk TMDCs, and each layer has a thickness of three atoms. A carbon nanotube (CNT) is a one-dimensional (1D) material with high electrical conductivity and small scattering cross section. The nanotube conducts primarily on its surface, where all the chemical bonds are saturated and stable. Additionally, there are no dangling bonds to form interface states. As a result, the interface between the gate dielectric and the nanotube channel does not require careful passivation. CNT have high mobility of approximately 80,000 cm^2/Vs, which stipulates that they are superior for high-speed electronics. Beta gallium oxide (β-Ga_2O_3) is a promising alternative for n-type channel material because of its large electrical breakdown voltage of ~8 $MVcm^{-1}$, ultra-wide band gap of 4.6–4.9 eV, high electron mobility of ~100 cm^2/Vs, and lattice compatibility with other wide band gap semiconductors (ZnO, SiC). All of these properties establish that β-Ga_2O_3 can be used for various electronic applications such as high-power applications, high-frequency devices, and optoelectronics. Table I presents the comparison of different channel materials.

Many experiments were done for designing NCFET channels with Group III–V semiconductors but did not succeed in achieving hysteresis-free and sub-60 mV/dec SS[53] simultaneously. Dong et al.[54] proposed an NCFET model with monolayer MoS_2 (molybdenum disulfide) as channel material. They demonstrated a simulation model explaining the effects of DIBL (drain-induced barrier lowering) and negative-output differential conductance (NDC) for a scaled-down NC-MOSFET. In addition, the inclusion of an ultrathin metallic layer with a monolayer channel significantly improves DIBL and NDC with a SS of 53.9 mV/decade. Similarly, low dimensional materials such as carbon nanotubes[22] and WSe_2 (tungsten diselenide)[55] are used as the channel in NCFET.

A comparative study on SS of the UTB NCFET using Ge and Si as channel materials was performed.[56] The results showed that a high permittivity germanium channel is more appropriate due to its high C_{ch} (capacitance of the channel depletion). The Ge channel provides a better sub-threshold gate capacitance due to its higher permittivity leading to higher channel capacitance, C_{ch} (ε_{ch}/T_{ch}). Furthermore, drain coupling (C_{DIBL}) increases as the channel permittivity increases. Thus, germanium on insulator NCFET(GeOI) is better than Si-based NCFET because of its higher C_{CH} and C_{DIBL} (drain coupling). Further, GeOI NCFETs can also achieve lower SS than the Si counterpart. Later, a steep-slope β-Ga_2O_3 (beta gallium oxide) NCFET was demonstrated in the dielectric stack at the gate with ferroelectric material hafnium zirconium oxide (HZO) with hysteresis less than 0.1 V.[57] Additionally, a minimum SS value of 34.3 mV/decade at reverse V_G (gate voltage) sweep and 53.1 mV/decade at forward V_G sweep at $V_{DS} = 0.5V$ is obtained. The enhancement-mode operation with a V_T (threshold voltage) of 0.4 V is achieved by adjusting the β-Ga_2O_3 membrane thickness. A 2D transition metal dichalcogenide (such as MoS_2) is a viable alternative channel material that provides sub-nanometer thickness and a more stabilized channel capacitance. This produces steep switches (slope) over a wide current range when coupled with the NC effect. In,[58] 2D NCFETs are demonstrated utilizing MoS_2 and hafnium zirconium oxide ($HfZrO_2$ or HZO) as channel and FE

Table I Comparison of different types of channel materials

Materials	Crystal Structure				Mobility (cm^2/Vs)		Band Gap (eV)	
	Interlayer distance (Å)	van der Waals gap (Å)	MX_2 sandwich thickness (Å)	M-X bond length (Å)	Bulk (>10 layers)	Monolayer	Bulk	Monolayer
MoS_2	6.15	2.98	3.17	2.42	60-200	>200	1.23	1.89
WSe_2	7	3.76	3.24	2.49	120-150	30-180	1.20	1.66
Carbon nanotube (CNT)	Single walled CNT (SWCNT)				~ 80,000		~1.1	
	Multiple walled CNT (MWCNT)				–		~1.1	
β-Ga_2O_3	Monoclinic				100		4.6-4.9	

materials, respectively. These materials are compatible with CMOS technology which achieves repeatable and sustained sub-60 mV/decade switching, thus making it a promising candidate for scalable and low voltage transistors. Up to that point, the only demonstration of a 2D channel NCFET was done by using polymeric ferroelectric materials, which resulted in unstable and incompatible CMOS but improved low-voltage switching.[59]

Devices for High ON Current

In 2011, Khan et al. suggested anti-ferroelectric (AFE) mode,[60] which achieved a sub-60 mV/decade SS and better current ratio. In this AFE mode, lines of ions in the crystal are spontaneously polarized, but with neighboring lines polarized in antiparallel directions. In simple cubic lattices, the antiferroelectric state is more stable than the ferroelectric state. Hu et al.[61] simulated the first negative capacitance FinFET, resulting in V_{dd} of 0.2V, 0.6mA/μm ON current, and 100pA/μm of leakage current. Later, Jang et al. reported that the ferroelectric HfO_2 -based NCFET with gate-all-around (GAA) nanowire channel design has five times and two times larger I_{ON}/I_{OFF} ratio than classical nanowire MOSFET and DG NCFET, respectively.[62] Another device, negative capacitance independent multi-gate FinFET (NC-IMG-FinFET), achieved SS of 42 mV/decade, larger ON current, and smaller OFF current by addition of 11 nm thick FE film at 300K. The leakage current can be controlled, and a significant high ON current can be obtained by increasing the thickness of FE material within a specific range.[63] However, increasing FE material thickness increases the equivalent input capacitance of the device. Thereafter, the negative capacitance carbon nanotube FETs (NC-CNFETs) were proposed, combining the advantages of carbon nanotube channels and NC effects.[22] The device achieves 20% less SS and 100% more ON current when compared to baseline CNFETs. In,[64] the influence of the coercive field, remnant polarization, and parasitic capacitance on NC-FinFET performance was investigated. A suitable value of P_r is recommended to attain high ON current than baseline. Another experiment was carried out using CIPS flake and MoS_2 2D van der Waals heterostructure, which improves current ON/OFF ratio and suited resistive RAM.[65] CIPS is copper indium thiophosphate ($CuInP_2S_6$), which has van der Waals (vdW) layered structure with switchable polarization down to ~4 nm, low leakage current, and robust ferroelectricity at 300K. The $CuInP_2S_6$ is a 2D ferroelectric insulator incorporated on the top of the MoS_2 channel allowing for a 2D/2D semiconductor/insulator interface with no dangling bonds. The MoS_2/CIPS 2D vdW heterostructure ferroelectric FETs exhibit a counter-clockwise hysteresis loop in transfer characteristics, clearly showing their ferroelectric properties. Additionally, it decreases the interface trap density and reduces interface issues. Furthermore, the back-gate bias of the MoS_2 transistors can modulate its stable nonvolatile memory attribute due to the tuning of capacitance matching between ferroelectric $CuInP_2S_6$ and MoS_2 channel, which consequently improves the ON/OFF current ratio.

Devices with Negligible Hysteresis and Improved SS

In 2012, Yeung et al. obtained sub-30 mV/decade SS in non-hysteretic NCFET by adopting body profile engineering. In this method, using a thin channel layer on a highly doped bottom layer improves the performance of SS by increasing the negative capacitance-voltage amplifying effect. This model achieves SS of 28.3 mV/decade over six orders of magnitude with I_{OFF}=10pA/μm, I_{ON}=0.3mA/μm at V_{DD}=0.3V for a gate length of 100 nm without strain mobility enhancement. However, the inclusion of a semiconductor layer on the conductor (T_{TSOC}) enhances the device's performance by mobility enhancement or shorter gate length.[6] In,[66] antiferroelectric HZO is used, resulting in zero hysteresis and an average SS of 50 mV/dec because of less remnant polarization and coercive field. Furthermore, an experimental analysis of HZO with epi-Ge/Si channel is hysteresis-free, switching at less than 0.2 V and SS of 42 mV/dec in forward sweep and 28 mV/dec in reverse sweep.[67] In 2017, aluminum-doped hafnium dioxide (HAO) was proposed as ferroelectric material.[68] It provides SS of 40 mV/decade and 39 mV/decade for the forward and reverse sweep, respectively, together with an almost hysteresis-free performance at room temperature and low temperature. The HAO-based FET shows a similar steep SS value and is also hysteresis-free as compared to ultra-thin FE-HZO. Among the other 2017 works, Lee et al.[69] demonstrated the FE-HZO (ferroelectric $HfZrO_x$) NCFET along with high-temperature annealing (free of hysteresis), and Nourbakhsh et al.[70] presented NC MoS_2 FET incorporating ferroelectric Al-doped HfO_2. Later, the analysis of hysteresis-free short-channel NCFETs was performed by associating quantum-mechanical calculations and the Landau–Khalatnikov equation which accounts for negative differential resistance (NDR) in the output characteristics.[71] Because of the strong gate controllability, since C_G (gate capacitance) increases with T_{FE} (ferroelectric thickness), both SS and DIBL decrease. When SS has an upper bound of 60 mV/decade, abnormal behavior emerges in NCFETs, such as DIBR (drain induced barrier rising) and NDR. Although both n-type and p-type NCFETs are hysteresis-free, hysteresis behavior is observed in an inverter due to NDR. In conventional MOSFETs, the load lines have a single cross point for one input voltage, but in the case of NCFETs with NDR, two or more cross points are observed. This induces the hysteresis behaviour in voltage transfer characteristics of NCFET inverters. The hysteresis loop can be modified by adjusting T_{FE}. As the T_{FE}

of NCFETs become thicker, the hysteresis loop becomes more apparent due to stronger NDR.

In 2018, methods for obtaining sub-kT/q non-hysteretic operation mode in NCFET for a wide band of V_G were investigated by employing capacitance matching.[72] In an unprecedented move, a unique approach for matching arbitrary MOSFETs with different ferroelectric (FE) materials was tossed. The NC germanium (Ge) pFETs introduce NDR with the different thicknesses of HfZrOx (HZO) was reported in.[73] For non-hysteretic devices, NDR is pronounced with an increased T_{FE} (thickness of ferroelectric film) and V_{GS} (gate voltage), leading to an improved matching between C_{FE} and C_{MOS}. For the hysteretic NC transistors, NDR can be achieved only at a lower V_{GS} because at a higher V_{GS}, $|C_{FE}|$ can be smaller than C_{MOS}, which increases the negative coupling factor.

Application-Specific Devices

The invention of $BaTiO_3$ (barium titanate) led to the development of ferroelectric oxide as a capacitor for industrial applications.[74] Afterward, the FE materials were used in the memories and switching devices for various applications. The use of the NC approach in electronic circuits has much lower power dissipation. Additionally, Yeung et al. reported the implementation of non-hysteretic NCFET to realize ultra-low power devices in.[6] Currently, various researchers are concentrating on developing more energy-efficient NC devices. The article[22] surveys energy-efficient electronic devices merging the advantages of NC effects and carbon nanotube channels for future generations. Capacitance enhancements, which were experimentally demonstrated in,[38] can be advantageous for ultra-dense DRAM applications. In 2014, for the first time, an NCFET-based pNCFET was fabricated.[75] Subsequently, pNCFET were fabricated on SOI MOSFET with PZT and STO (strontium titanate) deposition, and SS of almost 100 mV/decade was observed as the device was fabricated with very low gate leakage. However, it was not further tested because the gate contact pad was damaged when different temperature-dependent I-V measurements were attempted. NC-FinFET[61] was suitable for high-speed, low-power servers to ultra-low power IoT devices. The hysteresis behavior of the NCFET inverter[71] makes it a promising candidate for noise filters. Additionally, NCFET inverters with hysteresis behavior such as the Schmitt trigger can be used as a noise filter that advances the application area.

In 2017, Li et al. designed a non-volatile NCFET D-flip flop (DFF) which retained its state during power outages.[76] They also fabricated an NCFET which produces hysteresis edges below 10 mV/decade upon seven orders in magnitude between the two I_{DS} (drain-source current) states at V_G=0. Additionally, the device is energy efficient and has an ultra-low energy-delay overhead (less than 2.1%) in normal operations and can be used in IoT and power gating applications. Finally, β-Ga_2O_3 NCFETs prove to be a demanding nFET candidate for upcoming wideband gap CMOS logic applications.[57] The NCFET concept helps us to enable arbitrary tailoring of the energy landscape[77,78] and realize Landau switches.

In 2019, for the first time, researchers[79] investigated the outcomes of ferroelectric thickness in an undoped hafnium oxide-based NCFET. They developed a resistive load inverter which shows that increasing the ferroelectric thickness within a range enhances the noise margin and lowers the power dissipation. A charge plasma-based dopingless ring NCFET was designed and analyzed in,[80] which provides SS of 20 mV/dec and high ON current. It has a wide range of applications such as biomedical, RF sensing, analog circuits, and space.

Modifications in Other Attributes of NCFET

The preceding sections discussed the improvement of SS, ON current, and hysteresis of NCFET. However, there are still some other attributes of NCFET which also dominate the performance of the device. Thus, in the light of these attributes, Khan and his colleagues reported a method for measuring NC (negative capacitance) directly in an isolated ferroelectric capacitor.[81] This was a significant achievement because the calculation of negative capacitance in practice was a problem until that time. They also introduced two fundamental concepts called the characteristic negative capacitance transients and the dynamic hysteresis loop in negative capacitance. In 2016, Khandelwal et al. presented an NC FinFET model and extracted various performance parameter values. Nevertheless, the model did not include the effects of trap charges.[82] Subsequently, a spice-compatible model was published for NC FinFETs device, but it did not have the implications of ferroelectric parameters on device characteristics.[83] In their subsequent work, they proposed an enhanced model for NC FinFET in 2017, in which they included the effects of trap charges.[84] However, in 2016, Khan also published a report on a change in charge balance when the ferroelectric material is leaky. In addition, the model includes the non-ideal ferroelectric leakage phenomenon.[85] A ferroelectric capacitor with a parallel resistor is used for modeling the leakage, which offers the additional path to screening charges that degrade the performance. The solution to the above problem is the proper selection of work functions. It also reduces the leakage by modeling leakage as a resistance (I = V/R). The basic methodology for modeling NCFET includes an additional insulating layer which is controlled by the Landau–Khalatnikov equation written as,

$$V_{FE} = 2\alpha Q + 4\beta Q^3 + 6\gamma Q^5 \quad (5)$$

Khan also theoretically studied about leakage with the explanation of ferroelectric dynamics by Landau–Khalatnikov in the presence of a sandwiched metallic layer between the ferroelectric and dielectric material. In 2016, 18 nm and 27 nm thick (gadolinium) Gd:HfO_2 capacitors were presented in series with an external resistor. This provided negative capacitance measurement directly in the polycrystalline HfO_2 -based thin film.[86] Different key parameters reported for a couple of NCFET structures are plotted and compared in Fig. 7. This is an effort to highlight the improved device performance by modifying ferroelectric thickness, gate length, and 2D materials in the channel.

Comparison of Fe-FET and NCFET

Fe-FET has hysteretic V-I properties, but NCFET does not; thus, Fe-FET has a broader application area in memory devices. For an NCFET, the gate's overall capacitance is positive, implying that the negative capacitance state is stable in the ferroelectric insulator for a single state as per the quasi-static NC model. However, for the Fe-FET, the total capacitance of the gate is negative, so that the transistor transfer characteristics between two states result in hysteresis. The first experimental articles discussed the problem of steep-switching associated with Si Fe-FETs and "negative capacitance" using a thick polymer P(VDF-TrFE) as a ferroelectric insulator.[16,87,88] Another ferroelectric material PZT-based Fe-FET is modeled, and its advantage of decreasing the delay in a ring oscillator by 97% is illustrated.[89] Since 2014, several reports have been published on quasi-static or stabilized hysteresis-free Si NCFETs with SS of sub-60 mV/decade at room temperature. Also, researchers have investigated the performance of HZO as a ferroelectric gate insulator that provides a significant performance improvement. Following the above works, Si NCFETs were investigated with different gate stacks and structures falling into either Fe-FET (unstabilized NCFET)[47,90–94] or steep-slope hysteresis-free NCFET[20,68,95–99] with a minimum SS of sub-40 mV/decade at room temperature. This article includes all critical aspects of NCFETs, their physics, different channel engineering, and various low-power applications and their performances. In addition, the comparison of the figure of merit parameters of NCFET is presented in the following Table II.

Conclusion

The search for devices with faster switching speed than the conventional MOSFET has become a ubiquitous research motivation in the semiconductor industry. We have reviewed state-of-art technologies of NCFET for future low-power electronic devices. The paper discusses the development of various negative capacitance field-effect transistors from their initial stages until recent modifications. The incorporation of negative capacitance effect at gate provides sub-60 mV/decade SS which minimizes threshold voltage and thus power consumption. Moreover, it results

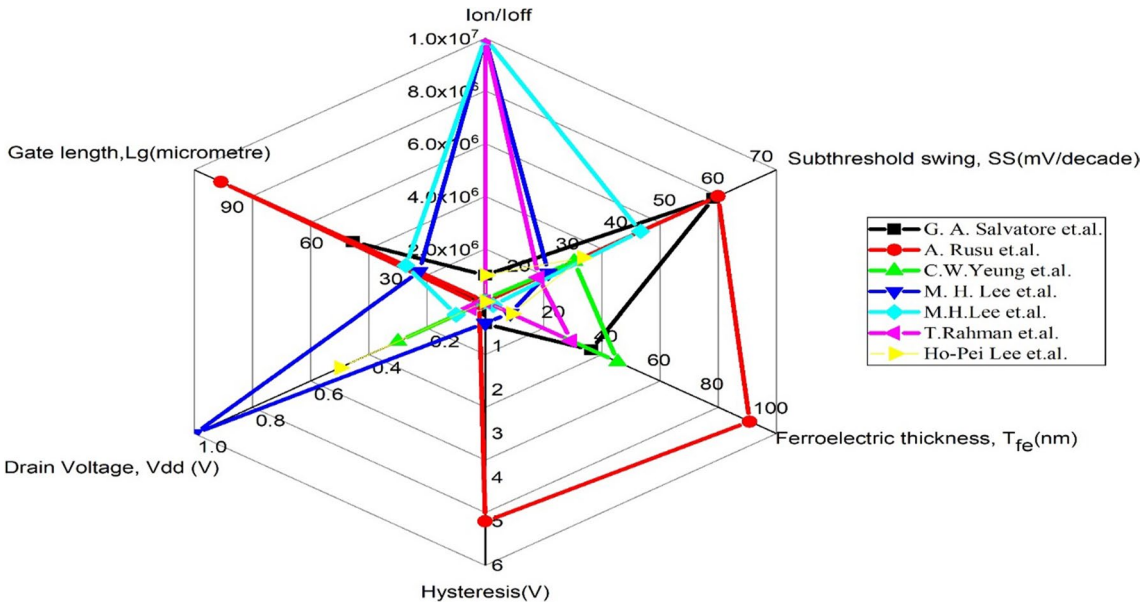

Fig. 7 Radar chart of the different figures of merit (FOMs) for different devices.

Table II Comparison of different types of NCFET based on various characteristics

Material and structure	Hysteresis	Sub-Threshold Slope $\left(\frac{mv}{dec}\right)$		Thickness	$I_{on}\left(\frac{mA}{\mu m}\right)$	$I_{off}\left(\frac{pA}{\mu m}\right)$	$\frac{Ion}{Ioff}$	Year
		With Fe	Without Fe					
NCFET with thin T_{SOC} layer design [6]	Absent	28.3	165	50 nm (Fe)	0.3	10	0.03	2012
$Pb(Zr_{0.2}Ti_{0.5})O_3$ [60]	Present	60	–	210 nm	–	10^5	Very large	2011
UTBNCFET [51]	Absent	21	253	0.5 nm (channel)	0.25	10	0.025	2013
$PbZr_{0.52}Ti_{0.48}O_3$ [39]	Present	13 (turn on), 32 (turn off)	–	100 nm	0.62	10^5	10^3	2015
NCFET with monolayer MOS_2 channel material [54]	Absent	50.1	–	10 nm	–	–	–	2017
FE:HfO_2-based NW-NCFET and DG-NCFET [62]	Absent	20-30	–	Variable 7-8 nm	–	–	5x higher than NW-MOSFET	2017
Al:HfO_2 (FE-HAO) FET [68]	Present (~4 mV)	40 (forward), 39 (reverse)	–	7 nm	–	–	–	2017
HfZrOx (FE-HZO) NCFET [69]	Absent	40.8 (forward), 41.6 (reverse)	–	1.5 nm and 3 nm	–	–	–	2017
NC MoS_2 FETs with Al:HfO_2 / HfO_2 [70]	Absent	57	67	10 nm	0.005	1	$0.05x10^6$	2017
UTB GeOI/SOI NCFET [56]	Absent	27 (Si), 21 (Ge)	–	32 nm-Si, 32.5 nm-Ge	–	–	10^6-10^7	2017
UTB-short-channel NCFET [71]	Absent	43.5	71.5	270 nm	12.9	–	Larger than conventional MOSFET	2017
β-Ga_2O_3 NCFET [57]	< 0.1 V	53.1 (forward), 34.3 (reverse)	–	20 nm	–	–	~10^7	2017
$Pb(Zr_{0.2}Ti_{0.8})O_3$ [47]	0.48 V	83 (forward), 19.6 (reverse)	104.7 (forward), 110.2 (reverse)	60 nm	_	_	10^7	2016
HfZrO [48]	Absent	58.8 (forward), 36 (reverse)	76 (forward) 86 (reverse)	10 nm	0.31	220	10^6	2017
NC-IMG-FinFET with HfSiO [63]	Absent	42	70	11 nm	Large	Small	Improved 2 to 3x	2018
NC-CNFET & [HAO] [22]	Absent	55 (avg.)	70	10 nm	2x improvement (CNT-FET)	–	Improved 2x that of baseline CNTFET	2017
Si:HfO_2 NCFET [49]	Absent	30	–	10 nm	–	–	–	2019
Zr:HfO_2 NCFET [52]	Absent	>20	–	1.8 nm	Large	–	10x increase	2018
Zr:Hfo_2 [91]	Absent	92 (forward), 38 (reverse)	–	5 nm	–	–	–	2017
Zr:Hfo_2 [96]	<1 mV	52	–	1.5 nm	–	–	–	2016
P(VDF-TrFe) [87]	0.5 V	13-57	–	4 nm	–	–	10^6	2007
P(VDF-TrFe) [88]	Large	46-58	–	100 nm	–	–	10^3	2010

in an additional barrier at the drain due to a decrease in internal gate voltage at higher drain voltage. At lower gate voltages and higher ferroelectric thickness, NDR behavior can be noticed in drain characteristics of NCFET. NCFETs also have lower SS and DIBL, which suppress short channel effects.

The discovery of ferroelectric properties of doped hafnium oxide in NCFET provides compatibility with CMOS structure and prevents the issue of limited scaling in conventional ferroelectric devices. As the technology scales below the 5 nm node, the critical device dimensions are extremely small, and the issue of incorporating thick FE layers into a gate stack turns out to be a challenging task. In addition, the incorporation of extremely thin 2D materials in the channel suppresses the short-channel effects. These two findings played a vital role in terms of scaling as well as enhancing the device characteristics. NCFET has brought significant changes to the semiconductor industry, and the design ecosystem is progressing with device new features.

NCFETs with SS<60 mV/decade, high I_{ON} / I_{OFF}, and adjustable hysteresis can reduce supply voltage and power dissipation, thus making them a viable choice for low-power applications. However, NCFET devices suffer from several issues such as difficulty in integration, heavy metal contamination of the manufacturing line, and the presence of thick traditional ferroelectric material. As a result, conventional ferroelectric materials such as barium titanate and lead zirconate titanate are incompatible with modern CMOS technology. Hence, many research efforts are required to improve the performance of NCFET through channel engineering, exploring different structural engineering, ferroelectric materials, and optimizing materials parameters which may enable the rapid commercialization of NCFET-based devices in the near future.

Acknowledgments The author would like to acknowledge NIT SILCHAR for financial support. We do not have involvement in any organization or entity with any financial interest (such as honoraria; educational grants; participation in speakers, bureaus; membership, employment, consultancies, stock ownership, or other equity interest; and expert testimony or patent-licensing arrangements); or non-financial interest (such as personal or professional relationships, affiliations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

Author contributions Malvika: Concept, Manuscript writing; BC, KM: Review and editing

Funding No funding statement was received in connection to this work.

Conflict of interest We declare that there is no conflict of interest in this manuscript.

Availability of data and material Not applicable

Consent to participate Not applicable

Consent for Publication All the authors have agreed to submit the article.

References

1. R.H. Dennard, F.H. Gaensslen, V.L. Rideout, E. Bassous, and A.R. LeBlanc, *IEEE J. Solid-State Circuits.* 9, 256 (1974). https://doi.org/10.1109/JSSC.1974.1050511.
2. S. Thompson, *Intel Tech. J.* Q3, (1998), [Online]. Available: http :// www. intel.com-/technology /itj/q31998/ articles/ art_3.html
3. R. D. Isaac, *IEEE 7th Topical Meet. Electri. Perf. Elect. Packg*., 3 (1998), doi: https://doi.org/10.1109/EPEP.1998.733476
4. L.B. Kish, *Phys. Lett. A*. 305, 144 (2002). https://doi.org/10.1016/S0375-9601(02)01365-8.
5. G. McFarland and M. Flynn, *Technical Report:* CSL-TR-95-662, (1995), [Online]. Available: http ://i.stanford.edu /pub/cstr/reports/ csl/tr/95/662/CSL-TR-95-662.pdf
6. C. W. Yeung, A. Khan, J.-Y. Cheng, S. Salahuddin and C. Hu, *Int. Conf. Sim. Semicon. Processes Dev.,* 257-259 (2012), [Online]. Available: http :// www .scopus -.com/ inward/ record.url?partnerID=HzOxMe3b&scp=85088044108&origin=inward
7. H. Kam, D.T. Lee, R.T. Howe, and T.J. King, *IEEE Int. Elec. Dev. Meet.* (2005). https://doi.org/10.1109/IEDM.2005.1609380.
8. Q. Huang, R. Huang, Y. Pan, S. Tan, Y. Wang, and I.E.E.E. Elec, *Dev. Lett.* 35, 877 (2014). https://doi.org/10.1109/LED.2014.2327219.
9. N. Abele, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A.M. Ionescu, *IEEE Int. Elec. Dev. Meet.* (2005). https://doi.org/10.1109/IEDM.2005.1609384.
10. W.Y. Choi, J.Y. Song, J.D. Lee, Y.J. Park, B.-G. Park, and I.E.E.E. Elec, *Dev. Lett.* 26, 261 (2005). https://doi.org/10.1109/LED.2005.844695.
11. S. Ramaswamy, and M.J. Kumar, *IEEE Trans. Elec. Dev.* 61, 4295 (2014). https://doi.org/10.1109/TED.2014.2361343.
12. G. Han, Y. Wang, Y. Liu, C. Zhang, Q. Feng, M. Liu, S. Zhao, B. Cheng, J. Zhang, Y. Hao, and I.E.E.E. Elect, *Dev. Lett.* 37, 701 (2016). https://doi.org/10.1109/LED.2016.2558823.
13. A.M. Ionescu, and H. Riel, *Nature* 479, 329 (2011). https://doi.org/10.1038/NATURE10679.
14. K. Yamabe, and K. Taniguhi, *IEEE Trans. Elect. Dev.* 32, 423 (1985). https://doi.org/10.1109/T-ED.1985.21958.
15. S. Salahuddin, and S. Datta, *Nano Lett.* 8, 405 (2008). https://doi.org/10.1021/NL071804g.
16. J. Jo, W.Y. Choi, J.D. Park, J.W. Shim, H.Y. Yu, and C. Shin, *Nano Lett.* 15, 4553 (2015). https://doi.org/10.1021/ACS.NANOLETT.5b01130.
17. J. Jo, and C. Shin, *Current Appl. Phys.* 15, 352 (2015). https://doi.org/10.1016/J.CAP.2014.12.029.
18. J. Jo, and C. Shin, *Elect. Lett* 51, 106 (2015). https://doi.org/10.1049/EL.2014.3515.
19. A. Khan, and S. Salahuddin, *IEEE SOI-3D-Subthreshold Microelectron. Tech Unified Conf.* S3S, 1 (2015). https://doi.org/10.1109/S3S.2015.7333485.
20. Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J. Liu, J. Shi, H.J. Kim, R. Sporer, C. Serrao, A. Busquet, P. Polakowski, J. Müller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, *Proc. IEEE Int. Elect. Dev. Meet. (IEDM).* (2017). https://doi.org/10.1109/IEDM.2017.8268393.
21. J. Li, J. Zhou, G. Han, Y. Liu, Y. Peng, J. Zhang, Q.-Q. Sun, D.W. Zhang, and Y. Hao, *IEEE Trans. Elect. Dev.* 65, 1217 (2018). https://doi.org/10.1109/TED.2018.2791420.
22. T. Srimani, G. Hills, M.D. Bishop, U. Radhakrishna, A. Zubair, R.S. Park, Y. Stein, T. Palacios, D. Antoniadis, M.M. Shulaker,

and I.E.E.E. Elect, *Dev. Lett.* 39, 304 (2018). https://doi.org/10.1109/LED.2017.2781901.
23. Y.J. Kim, M.H. Park, W. Jeon, H.J. Kim, T. Moon, Y.H. Lee, K.D. Kim, S.D. Hyun, and C.S. Hwang, *J. Appl. Phys.* 118, 224105 (2015). https://doi.org/10.1063/1.4937544.
24. M. Kobayashi, and T. Hiramoto, *AIP Adv.* 6, 025113 (2016). https://doi.org/10.1063/1.4942427.
25. J. Fousek, *Proc. IEEE Int. Symp. App. Ferro.,* 1-5 (1994), Doi:https://doi.org/10.1109/ISAF.1994.522283
26. E. Yurchuk, J. Muller, J. Paul, T. Schlosser, D. Martin, R. Hoffmann, S. Müeller, S. Slesazeck, U. Schröeder, R. Boschke, R.V. Bentum, and T. Mikolajick, *Elect. Dev. IEEE Trans.* 61, 3699 (2014). https://doi.org/10.1109/TED.2014.2354833.
27. O. Auciello, *Integd. Ferroelectr.* 15, 211 (1997). https://doi.org/10.1080/10584589708015712.
28. R.R. Das, S.B. Majumder, and R.S. Katiyar, *Integd. Ferro.* 42, 323 (2002). https://doi.org/10.1080/10584580210863.
29. J. Mueller, U. Schroeder, T.S. Boescke, I. Mueller, U. Böttger, L. Wilde, J. Sundqvist, M. Lemberger, P. Kücher, T. Mikolajick, and L. Frey, *J App Phy* 110, 114113 (2011). https://doi.org/10.1063/1.3667205.
30. T. Olsen, U. Schroeder, S. Mueller, A. Krause, D. Martin, A. Singh, J. Mueller, M. Geidel, and T. Mikolajick, *App. Phy. Lett.* 101, 082905 (2012). https://doi.org/10.1063/1.4747209.
31. T.S. Boscke, S.T. Teichert, D. Brauhaus, J. Mueller, U. Schroeder, U. Boettger, and T. Mikolajick, *App Phy Lett* 99, 112904 (2011). https://doi.org/10.1063/1.3636434.
32. S. Mueller, J. Mller, R. Homann, E. Yurchuk, T. Schlosser et al., *Elect. Dev. IEEE Trans.* 60, 4199 (2013). https://doi.org/10.1109/TED.2013.2283465.
33. T.S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, *App. Phy. Lett.* 99, 102903 (2011). https://doi.org/10.1063/1.3634052.
34. J. Müller, T.S. Böscke, S. Müller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin et al., *IEEE Int. Elect. Dev. Meet.* (2013). https://doi.org/10.1109/IEDM.2013.6724605.
35. J. Müller, P. Polakowski, S. Müller, and T. Mikolajick, *ECS Trans.* 64, 159 (2014). https://doi.org/10.1149/06408.0159ECST.
36. S. Mueller, J. Mller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, *Adv. Funct. Mat.* 22, 2412 (2012). https://doi.org/10.1002/ADFM.201103119.
37. R.A. McKee, F.J. Walker, and M.F. Chisholm, *Phys. Rev. Lett.* 81, 3014 (1998). https://doi.org/10.1103/PhysRevLett.81.3014.
38. A.I. Khan, D. Bhowmik, P. Yu, S. Joo Kim, X. Pan, R. Ramesh, and S. Salahuddin, *App. Phys. Lett.* 99, 113501 (2011). https://doi.org/10.1063/1.3634072.
39. S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S.T. Mckinstry, and S. Datta, *IEEE J. Explor. Solid-State Comput. Dev. Circuits.* 1, 43 (2015). https://doi.org/10.1109/JXCDC.2015.2448414.
40. A.F. Devonshire, *Adv. Phys.* 3, 85 (1954). https://doi.org/10.1080/00018735400101173.
41. A.F. Devonshire, *Philos. Mag.* 40, 1040 (1949). https://doi.org/10.1080/14786444908561372.
42. A.F. Devonshire, *Philos. Mag.* 42, 1065 (1951). https://doi.org/10.1080/14786445108561354.
43. L.D. Landau, and I.M. Khalatnikov, *Dokl. Akad. Nauk SSSR* 96, 469 (1954). https://doi.org/10.1016/B978-0-08-010586-4.50087-0.
44. P. Chandra, and P.B. Littlewood, *Phy. Ferro.* 105, 69 (2007). https://doi.org/10.1007/978-3-540-34591-6_3.
45. V.C. Lo, *J. App. Phys.* 94, 3353 (2003). https://doi.org/10.1063/1.1598275.
46. W. Zhang, and K. Bhattacharya, *Acta Mater.* 53, 185 (2005). https://doi.org/10.1016/J.ACTAMAT.2004.09.016.
47. E. Ko, J.W. Lee, C. Shin, and I.E.E.E. Elect, *Dev. Lett.* 38, 418 (2017). https://doi.org/10.1109/LED.2017.2672967.
48. E. Ko, H. Lee, Y. Goh, S. Jeon, and C. Shin, *IEEE J. Elect. Dev. Soc.* 5, 306 (2017). https://doi.org/10.1109/JEDS.2017.2731401.
49. T. Rahman, A. Fairooz Khan and N. Nawal, *Ist Int. Conf. Adv. Sci., Engg. & Rob. Tech. (ICASERT),* 1-6 (2019), Doi:https://doi.org/10.1109/ICASERT.2019.8934575
50. H. Agarwal, P. Kushwaha, Y.K. Lin et al., *IEEE Elect. Dev. Lett.* 40, 463 (2019). https://doi.org/10.1109/LED.2019.2891540.
51. C. W. Yeung, A. I. Khan, A. Sarker, S. Salahuddin and C. Hu. *VLSI-TSA, Int. Symp*., 1-2 (2013), Doi:https://doi.org/10.1109/VLSI-TSA.2013.6545648
52. D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y.H. Liao, A.J. Tan, C. Hu, and S. Salahuddin, *IEEE Elec. Dev. Lett.* 40, 993 (2019). https://doi.org/10.1109/LED.2019.2912413.
53. Q. H. Luc, C. C. Fan-Chiang, S. H. Huynh, P. Huang, H. B. Do, M. T. H. Ha, Y. D. Jin, T. A. Nguyen, K. Y. Zhang, H. C.Wang, Y. K. Lin, Y. C. Lin, C. Hu, H. Iwai, and E. Y. Chang, *IEEE Symp. VLSI Tech.* 47–48 (2018), Doi: https://doi.org/10.1109/VLSIT.2018.8510644
54. Z. Dong, and J. Guo, *IEEE Trans. Elect. Dev.* 64, 2927 (2017). https://doi.org/10.1109/TED.2017.2706182.
55. M. Si, C. Jiang, W. Chung, Y. Du, M.A. Alam, and P.D. Ye, *Nano Lett.* 18, 3682 (2018). https://doi.org/10.1021/ACS.NANOLETT.8b00816.
56. H.-P. Lee, C.-L. Yu, W.-X. You and P. Su, *Int. Symp. VLSI technology, systems and application (VLSI-TSA),* 1-2 (2017), doi:https://doi.org/10.1109/VLSI-TSA.2017.7942460
57. M. Si, L. Yang, H. Zhou, and P.D. Ye, *ACS Omega* 2, 7136 (2017). https://doi.org/10.1021/ACSOMEGA.7b01289.
58. F. A. McGuire, Y.-C. Lin, B. Rayner and A. D. Franklin, *In Proc. 75th Annu. Dev. Res. Conf. (DRC)*, 1-2 (2017), Doi:https://doi.org/10.1109/DRC.2017.7999478
59. F.A. McGuire, Z. Cheng, K. Price, and A.D. Franklin, *Appl. Phys. Lett.* 109, 093101 (2016). https://doi.org/10.1063/1.4961108.
60. A.I. Khan, C.W. Yeung, C. Hu, and S. Salahuddin, *IEEE Int. Elect. Dev. Meet.* (2011). https://doi.org/10.1109/IEDM.2011.6131532.
61. C. Hu, S. Salahuddin, C. Lin and A.Khan., *IEEE Dev. Res. Conf. (DRC),* 39-40 (2015), Doi: https://doi.org/10.1109/DRC.2015.7175542
62. K. Jang, T. Saraya, M. Kobayeshi, and T. Hiramoto, *Solid-State Elec.* 136, 60 (2017). https://doi.org/10.1016/J.SSE.2017.06.011.
63. T. Yang, J. Hu and W. Bai, *IEEE Int. Symp. Circuits and Sys. (ISCAS),* 1-5 (2018), Doi: https://doi.org/10.1109/ISCAS.2018.8351762
64. J. Min, and C. Shin, *Elec.* 9, 1423 (2020). https://doi.org/10.3390/ELECTRONICS9091423.
65. M. Si, P.-Y. Liao, G. Qiu, Y. Duan, and P.D. Ye, *ACS Nano* 12, 6700 (2018). https://doi.org/10.1021/ACSNANO.8b01810.
66. M.H. Lee, Y.T. Wei, K.Y. Chu, J.J. Huang, C.W. Chen, C.C. Cheng, M.J. Chen, H.Y. Lee, Y.S. Chen, L.H. Lee, and M.J. Tsai, *IEEE Elect. Dev. Lett.* 36, 294 (2015). https://doi.org/10.1109/LED.2015.2402517.
67. M.H. Lee, P.G. Chen, C. Liu, K. Chu, C.C. Cheng, M.J. Xie, S.N. Liu, J.W. Lee, S.J. Huang, M.H. Liao, K.S. Li, and M.C. Chen, *IEEE Int. Elect. Dev. Meet.* (2015). https://doi.org/10.1109/IEDM.2015.7409759.
68. M.H. Lee, P.G. Chen, S. Fan, Y.C. Chou, C.Y. Kuo, C.H. Tang, H.H. Chen et al., *IEEE Int. Elect. Dev. Meet.* (2017). https://doi.org/10.1109/IEDM.2017.8268445.
69. M. H. Lee, P.-G. Chen, S.-T. Fan, C.-Y. Kuo, H.-H. Chen, S.-S. Gu, Y.-C. Chou, C.-H. Tang, R.-C. Hong, Z.-Y. Wang, M.-H. Liao, K.-S. Li, M.-C. Chen and C. W. Liu, *Int. Symp. VLSI Tech. Sys. App. (VLSI-TSA),* 1-2 (2017), Doi:https://doi.org/10.1109/VLSI-TSA.2017.7942466

70. A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, *Nano Scale* 9, 6122 (2017). https://doi.org/10.1039/C7NR00088J.
71. J. Seo, J. Lee, and M. Shin, *IEEE Trans. Elect. Dev.* 64, 1793 (2017). https://doi.org/10.1109/TED.2017.2658673.
72. P. Bidenko, S. Lee, J.-H. Han, J.D. Song, and S.-H. Kim, *IEEE J. Elect. Dev. Soc.* 6, 910 (2018). https://doi.org/10.1109/JEDS.2018.2864593.
73. J. Zhou, G. Han, J. Li, Y. Liu, Y. Peng, J. Zhang, Q.Q. Sun, D.W. Zhang, and Y. Hao, *IEEE Elect. Dev. Lett.* 39, 622 (2018). https://doi.org/10.1109/LED.2018.2810071.
74. B. Meyer, and D. Vanderbilt, *Phys. Rev.* 63, 205426 (2000). https://doi.org/10.1103/PhysRevB.63.205426.
75. C. W. Yeung, *Berkeley Tech. Rep*., UCB/EECS-2014-226, (2014), [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-226.html
76. X. Li, J. Sampson, A. Khan, K. Ma, S. George, A. Aziz, S.K. Gupta, S. Salahuddin, M.F. Chang, S. Datta, and V. Narayanan, *IEEE Trans. Elect. Dev.* 64, 3452 (2017). https://doi.org/10.1109/TED.2017.2716338.
77. K. Karda, A. Jain, C. Mouli, and M.A. Alam, *Appl. Phys. Lett.* 106, 163501 (2015). https://doi.org/10.1063/1.4918649.
78. A. Jain, and M.A. Alam, *IEEE Trans. Elect. Dev.* 60, 4269 (2013). https://doi.org/10.1109/TED.2013.2286997.
79. B. Awadhiya, P.N. Kondekar, and A.D. Meshram, *J. Elec. Mat.* 48, 6762 (2019). https://doi.org/10.1007/s11664-019-07483-1.
80. A.K. Gupta, A. Raman, and N. Kumar, *J. Elec. Mat.* 49, 4852 (2020). https://doi.org/10.1007/s11664-020-08205-8.
81. A. I. Khan, *Berkeley Tech. Rep.,* UCB/EECS-2015-171, (2015), [Online]. Available: http://www.eecs.ber keley.edu/Pubs/TechRpts/2015/EECS-2015-171.html
82. S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin and C. Hu*, VLSI Tech. Symp.*, 1-2 (2016), Doi:https://doi.org/10.1109/VLSIT.2016.7573446
83. A. Aziz, S. Ghosh, S. Datta, and S. Kumar Gupta, *IEEE Elect. Dev. Lett.* 37, 805 (2016). https://doi.org/10.1109/LED.2016.2558149.
84. S. Khandelwal, J.P. Duarte, A.I. Khan, S. Salahuddin, and C. Hu, *IEEE Elec. Dev. Lett.* 38, 142 (2017). https://doi.org/10.1109/LED.2016.2628349.
85. A.I. Khan, U. Radhakhrishna, K. Chatterjee, S. Salahuddin, and D. Antoniadis, *IEEE Trans. Elec. Dev.* 63, 1 (2016). https://doi.org/10.1109/TED.2016.2612656.
86. M. Hoffman, M. Pesic, K. Chatterjee, A.I. Khan, S. Salahuddin, S. Slesazeck, U. Schroeder, and T.M. Kolajicky, *Adv. Func. Mater.* 26, 8643 (2016). https://doi.org/10.1002/ADFM.201602869.
87. G.A. Salvatore, D. Bouvet, and A.M. Ionescu, *IEEE Int. Elect. Dev. Meet.* (2008). https://doi.org/10.1109/IEDM.2008.4796642.
88. A. Rusu, G.A. Salvatore, D. Jimenez, and A.M. Ionescu, *IEEE Int. Elect. Dev. Meet.* (2010). https://doi.org/10.1063/IEDM.1.5092684.
89. A. Aziz, S. Ghosh, S. Datta, S.K. Gupta, and I.E.E.E. Elect, *Dev. Lett.* 37, 805 (2016). https://doi.org/10.1109/LED.2016.2558149.
90. A.I. Khan, K. Chatterjee, J.P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu, and S. Salahuddin, *IEEE Elec. Dev. Lett.* 37, 111 (2016). https://doi.org/10.1109/LED.2015.2501319.
91. P. Sharma, K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, and S. Datta, *Symp. VLSI Tech.,* 154–155 (2017), Doi:https://doi.org/10.1063/LVT.1.5092684
92. S.R. Bakaul, C.R. Serrao, M. Lee, C.W. Yeung, A. Sarker, S.L. Hsu, A.K. Yadav, L. Dedon, L. You, A.I. Khan, J.D. Clarkson, C. Hu, R. Ramesh, and S. Salahuddin, *Nat. Commun.* 7, 10547 (2016). https://doi.org/10.1038/NCOMMS/10547.
93. M.H. Lee, K.T. Chen, C.Y. Liao, S.S. Gu, G.Y. Siang, Y.C. Chou, H.Y. Chen, J. Le, R.C. Hong, Z.Y. Wang, S.Y. Chen, P.G. Chen, M. Tang, Y.D. Lin, H.Y. Lee, K.S. Li, and C.W. Liu, *IEEE Int. Elect. Dev. Meet.* (2018). https://doi.org/10.1109/IEDM.2018.8614510.
94. K.S. Li, Y.J. Wei, Y.J. Chen, W.C. Chiu, H.C. Chen, M.H. Lee, Y.F. Chiu, F.K. Hsueh, B.W. Wu, P.G. Chen, T.Y. Lai, C.C. Chen, J.M. Shieh, W.K. Yeh, S. Salahuddin, and C. Hu, *IEEE Int. Elect. Dev. Meet.* (2018). https://doi.org/10.1109/IEDM.2018.8614521.
95. J. Jo, C. Shin, and I.E.E.E. Elect, *Dev. Lett.* 37, 245 (2016). https://doi.org/10.1109/JEDS.2017.2731401.
96. M.H. Lee, S.T. Fan, C.H. Tang, P.G. Chen, Y.C. Chou, H.H. Chen, J.Y. Kuo, M.J. Xie, S.N. Liu, M.H. Liao, C.A. Jong, K.S. Li, M.C. Chen, and C.W. Liu, *IEEE Int. Elect. Dev. Meet.* (2016). https://doi.org/10.1109/IEDM.2016.7838400.
97. C. Fan, C. Cheng, Y. Chen, C. Liu, and C. Chang, *IEEE Int. Elect. Dev. Meet.* (2017). https://doi.org/10.1063/IEDM.2017/1.5124915.
98. D. Kwon, K. Chatterjee, A.J. Tan, A.K. Yadav, H. Zhou, A.B. Sachid, R. Dos Reis, C. Hu, S. Salahuddin, and I.E.E.E. Elect, *Dev. Lett.* 39, 300 (2018). https://doi.org/10.1109/LED.2017.2787063.
99. H. Zhou, D. Kwon, A. B. Sachid, Y. Liao, K. Chatterjee, A. J. Tan, A. K. Yadav, C. Hu and S. Salahuddin, *IEEE Symp. VLSI Tech.,* 53–54 (2018), doi:https://doi.org/10.1109/VLSIT.2018.8510691