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ORIGINAL RESEARCH ARTICLE

Analysis of Double Gaussian Distribution on Barrier Inhomogeneity in a Au/n-4H SiC Schottky Diode

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Abstract

A n-4H SiC based diode is fabricated by an Au front metal contact to provide rectification at the metal-semiconductor (MS) junction, and a back ohmic contact is also obtained using Au metal with post-thermal heating. MS diode characteristics are investigated by current–voltage ($I-V$) measurements with a wide range of temperature from 80 K to 300 K. At each temperature, rectifying behavior is achieved and it is improved with an increase in temperature. Barrier height and ideality factor are calculated according to the thermionic emission (TE) model from linearity in the forward bias region of the ln(I) versus V plot. The experimental zero-bias barrier height (Φ_{b0}) values are in a good agreement with literature, and at around room temperature the ideality factor (n) reaches unity. At saturation regions in $I-V$ curves, parasitic resistance values are derived by Ohm's law and the series resistance values are also reevaluated by Cheung's relation. Detailed $I-V$ analysis is performed by modifying the TE model with an approximation of low barrier patches embedded in the main barrier height. Two linear relations in the characteristic plots of Φ_{b0} and n indicate that double Gaussian distribution is a suitable current conduction model via localized barrier patches at low temperatures. Additionally, reverse bias current flow is analyzed under the dominant effect of Poole-Frenkel emission associated with the interfacial traps. According to the characteristic electric field-dependent current density plot, emission barrier height and relative dielectric constant for n-4H SiC are calculated.

Keywords Schottky diode · current transport · double Gaussian distribution · barrier inhomogeneity

Introduction

In today's electronic technology, the conventional Si-based metal-semiconductor (MS) diodes are still popular with alternative contact and also interface layer contribution. Because of their indirect band gap characteristics and mechanical limitations of the wafer nature, a performance and feasibility survey is also in a way to use compatible semiconductor materials with Si.[1–4] Although there are several works on adaptation of an oxide/insulator/dielectric layer at the MS interface to improve rectification, current flow and capacitive characteristics of these diodes, the choice of active semiconductor layer is also important to achieve this aim in metal-oxide-semiconductor (MOS) and metal-insulator-semiconductor (MIS) diodes in addition to the MS applications.[5–7] Among several prominent active layer alternatives, together with GaAs and GaN, SiC is a preferred semiconductor with its well-suited mechanical and physical properties in these diode applications.[8–12] They draw interest as being wide band gap semiconductors which enable high performance in the field of research on diodes. In addition to the ability to extend operation limits of electronic and optoelectronic devices for power, frequency and temperature conditions, SiC is a point of interest when used in a radioactive environment.[9–14] In fact, there are three SiC poly-types, 3H, 4H and 6H SiC, in this field where their band gap, thermal conductivity, and breakdown electric field characteristics present valuable results.[15–17] n-type 4H SiC functions in high-frequency and high-temperature conditions where its material characteristics can provide charge flow and high

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current densities compared to conventional Si.[17–20] There are various reports on different rectifying and ohmic metal contacts deposited on this semiconductor surface to obtain MS diode and interface layer adaptation for MIS/MOS types of diodes.[21–24] However, high reverse leakage current in n-4H SiC based diodes is a key point in current works and it attracts research on interface characteristics at the MS junction.[15,22,25] To meet the technological demand on high rectifying performance, the optimization works are required for metal contact on this active layer and, therefore, there are several contact engineering works, such as the use of Al, Au, Ni, Pd, Ti, W and Co.[26–30] There is also research using multiple layers such as Al/Ti, Ti/Al and Au/Ti/Al to get low contact resistances on the n-4H SiC layer [15]. Among them, with its high work function, Au is popular to obtain good rectification properties in use as a contact on SiC and it can also serve as an ohmic contact by applying post-thermal heating.[22] Additionally, it is used to form both top and bottom contacts in MS diodes with the aim of preventing possible oxidation during thermal treatments to the diode.[15]

This work presents temperature-dependent current–voltage ($I - V$) characteristics of an Au/n-4H SiC MS diode with a predominant effect of double Gaussian distribution (GD) on current flow with barrier inhomogeneity. Conduction process and nature of the barrier at the junction are analyzed in detail with a wide range of temperature. Although it is simply constructed as an MS junction, the ideality in the diode is discussed under the existence and possible effects of parasitic resistance and interface trap states at the junction. The interface quality between layers and their material characteristics can cause a spatial variation in barrier height and deviation from ideal diode behavior with a higher value of ideality factor than unity.[31,32] Among different metal contacts, the n-4H SiC MS diode is constructed with an Au-rectifying layer, and this structure is investigated under effects of operating temperature to discuss its performance and thermal sensitivity. In literature, there are some studies on this type MS diode to realize interfacial properties at the junction; however, the current work is detailed on the goal of research contribution to the literature where abnormal diode behavior is examined by two Gaussian functions.[16,22,33] In fact, this is the case for the presence and localization of small barrier patches with low barrier around the main barrier height. The current conduction mechanism is well-suited to thermionic emission (TE) supported by an approximation of GD of these barriers. With this aim, the electrical properties of the fabricated diode are investigated with a change in ambient temperature between 80 K and 300 K under a bias voltage of ± 3 V. As a function of operating temperature, barrier height, ideality factor, and series and shunt resistances are calculated.

Experimental Details

The Au/n-4H SiC MS diode structure is constructed on an n-4H SiC semiconductor wafer substrate with 7.1×10^{17} cm^{-3} doping concentration and $1.5–2.8 \times 10^{-3}$ Ω cm surface resistivity. It is prepared in pieces of 2 cm^2 surface area where the thickness is 500 µm. To remove organic/inorganic residues on the wafer surface, ultrasonic cleaning is applied using a dilute chemical solution of hydrogen peroxide, undiluted acetone and isopropyl alcohol, separately. Additionally, HF etching is performed to remove the surface oxide layer. Both wafer surfaces are deposited by elemental Au metal evaporation using electron-beam evaporation, and 250-nm-thick front and back contacts are obtained. In these processes, an Au front contact is deposited through a Cu metal shadow mask including dot-shaped holes with an area of 0.015 cm^2. On the other hand, the full surface of the back side is coated with Au and then ohmic behavior is obtained by sequential annealing at 500 °C for 5 min under continuous nitrogen flow. The schematic design structure and the energy band diagram for the diode are shown in Fig. 1 (inset). The rectification is between the Au top contact and n-4H SiC semiconductor layer. The inset figure is presented before merging these two layers to construct the MS junction. Then, the diode includes Au metal with a work function of 5.1 eV and n-4H SiC with electron affinity and band gap energy of 4.17 and 3.26 eV, respectively.[34–36]

Fabricated diode is characterized by temperature-dependent $I - V$ measurements with a bias limit of 3 V between 80 K and 300 K. The diode is fixed inside a Leybold–Heraeus closed-cycle helium cryostat, and the diode temperature is controlled by a Lakeshore DCR-91C controller. At each temperature step, experimental current values are collected by using a Keithley 4200 sourcemeter under a bias voltage range from −3 to +3 V.

Results and Discussion

Current transport properties of the Au/n-4H SiC Schottky diode are characterized in a wide temperature range from 80 K to 300 K. At each temperature point, current–voltage ($I - V$) measurements are performed between − 3 V and + 3 V bias voltage range. The observed temperature-dependent $I - V$ curves in semi-logarithmic form are given in Fig. 1. As shown in this figure, the MS junction between the Au front contact and the n-4H SiC layer satisfies a rectifying behavior. It is observed at all temperatures, and with an increase in temperature this behavior is improved. Although the forward bias current values increase with

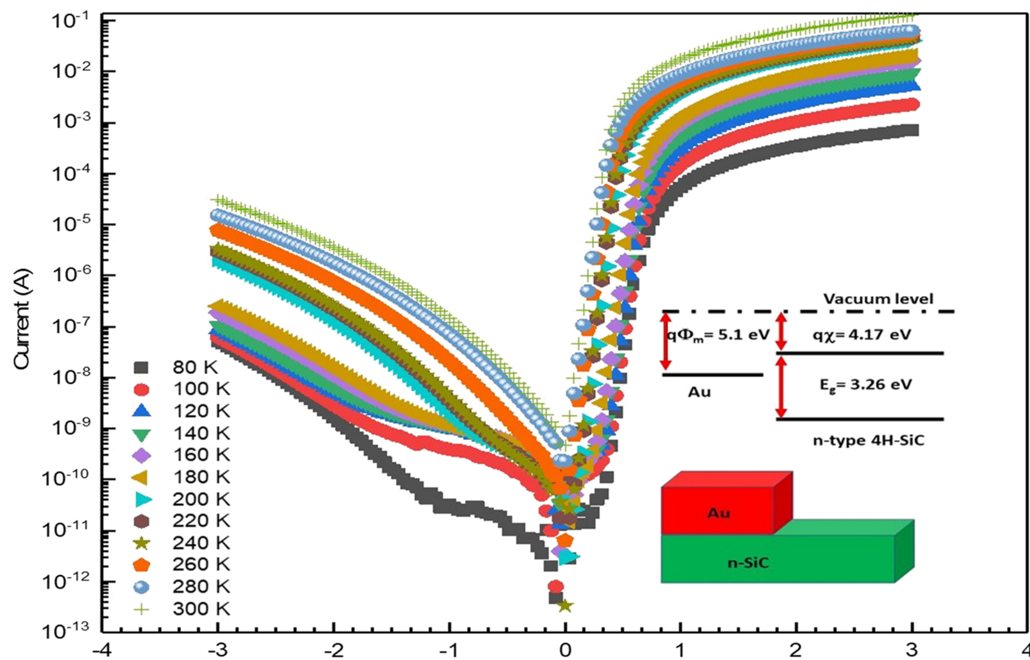

Fig. 1 Temperature-dependent semi-logarithmic $I-V$ plot of the diode. *Inset figure* show schematic and electronic band diagrams of the diode.

temperature effect on current transport, in the low voltage region, leakage current also increases. The linearity in semi-logarithmic curves gives a high slope with temperature where it enhances electrical current flow from the Au metal contact to the n-4H SiC semiconductor layer in the forward bias region. However, on the opposite side, it also triggers generation and flow of minority carriers from the semiconductor to the ohmic Au metal contact.[37] With thermal effect-based improvement in the forward voltage region, the rectification increases up to four orders of magnitude for the average ratio between forward and reverse current values. At the interface of this MS structure, there is no intentional insulator/oxide layer fabrication. However, the real model can be modified due to the unintentional native interfacial region as a result of possible non-ideal experimental processes.[38] Ideally, transport through the diode junction can be assumed to be in a good match with thermionic emission (TE) where carriers are under a dominant effect of temperature. In the real case, it is a common observation on the charge carriers that barrier inhomogeneity and current transport behavior can deviate from the standard TE model. Therefore, $I-V$ relation for a non-ideal case can be introduced for a Schottky barrier formation as,[34,38]

$$I = I_0\left[\exp\left(\frac{qV - IR_s}{nkT}\right) - 1\right] \tag{1}$$

The series resistance (R_s) contribution to Eq. 1 is in use to modify the TE model where possible voltage drop across the diode can be related to the effect of parasitic resistance. It is common in literature that there can be several obstacles along the current path due to material resistance of both contact and semiconductor layers and an intentional/unintentional interfacial layer between them, as well as contact resistance at the interface regions between each of these layers.[4] In the given equation, the other parameters have fixed values that are the magnitude of electron charge (q), Boltzmann constant (k), reverse saturation current (I_0) and ideality factor (n) at a given temperature (T). I_0 is the pre-exponential factor used to express possible reverse current flow due to diffusion of minority carriers.[38] It also includes information for barrier height of the diode in a relation as;

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{2}$$

where zero-bias barrier height (Φ_{b0}) can be obtained from the extrapolation of linearity in a semi-logarithmic $I-V$ graph at zero-bias point (Fig. 1). From Eq. 2, temperature-dependent Φ_{b0} values can be calculated depending on the active diode area (A) limited with the surface area of the front contact and the effective Richardson constant A^*. In the fabricated Au/n-4H SiC diode, the top circular contact area is 0.015 cm^2 and A^* can be estimated as 146 $A/cm^{-2}K^{-2}$ for an active n-4H SiC semiconductor layer.[39] Without the dominant effect of R_s, the obtained linearity at low forward bias voltage in the range of 0.1–0.5 V is used to model $I-V$ relation with TE model. This is the case to match with the approximated values of the parameters used to guide detailed

diode analysis. In this case, I_0 is almost independent of reverse bias voltage with the choice of $V > 3kT/q$ and this condition provides eliminating possible effects of reverse current contribution.[39,40] Then, exponential variation in current values with forward bias voltage can be observed as a straight line in the semi-logarithmic $I - V$ plot (Fig. 1), and Φ_{b0} values are obtained as a function of temperature from the zero-point intercepts of the corresponding lines. The values of I_0 and Φ_{b0} are found as 1.05×10^{-10} A and 0.22 eV (at 80 K) to 5.08×10^{-9} A and 0.81 eV (at 300 K), respectively. The Φ_{b0} values listed in Table I are in the range of reported values of the junctions between Au and n-4H SiC which are fabricated with different deposition methods and conditions.[22,28] As given in Fig. 2a, there is a direct proportionality between Φ_{b0} and temperature. This observation confirms the deviation from the TE model that can be possibly associated with the effects of interface trap states between Au and n-4H SiC layers.[41] This type of junction interface can change the response of the barrier to the carrier flow and it can be correlated with the spatial inhomogenetiy in the barrier height.[41–43] In this case, the carriers come across to lower barriers at low temperature and the highly energetic ones can overcome the high barrier in the junction at high temperature.[44] This type of barrier height difference over the contact area is the result of the presence and variations of interfacial charges.[43] In literature, it is mentioned with the presence and localization of barrier patches and, therefore, the modification of an ideal TE model with considering several alternative current paths is widely used.[40,45]

In Eq. 1, n is the parameter to evaluate the possible deviation from ideal diode behaviour. It is referred to as the ideality factor since the unity ($n = 1$) is used to verify pure TE mechanism in the carrier transport.[30] Therefore, the

Table I Temperature-dependent diode parameters approximated from the TE model

T(K)	n	Φ_{b0}(eV)	$R_s(\Omega)$ from $H(I)$ versus I plot	$R_s(\Omega)$ from $dV/dln(I)$ versus I plot
80	33.37	0.22	1970	3370
100	25.57	0.27	650	1100
120	19.58	0.32	300	490
140	11.41	0.39	220	290
160	5.62	0.46	140	160
180	3.79	0.53	120	130
200	1.54	0.63	65	60
220	1.35	0.68	57	51
240	1.21	0.75	56	50
260	1.13	0.76	45	41
280	1.12	0.79	40	36
300	1.10	0.81	20	18

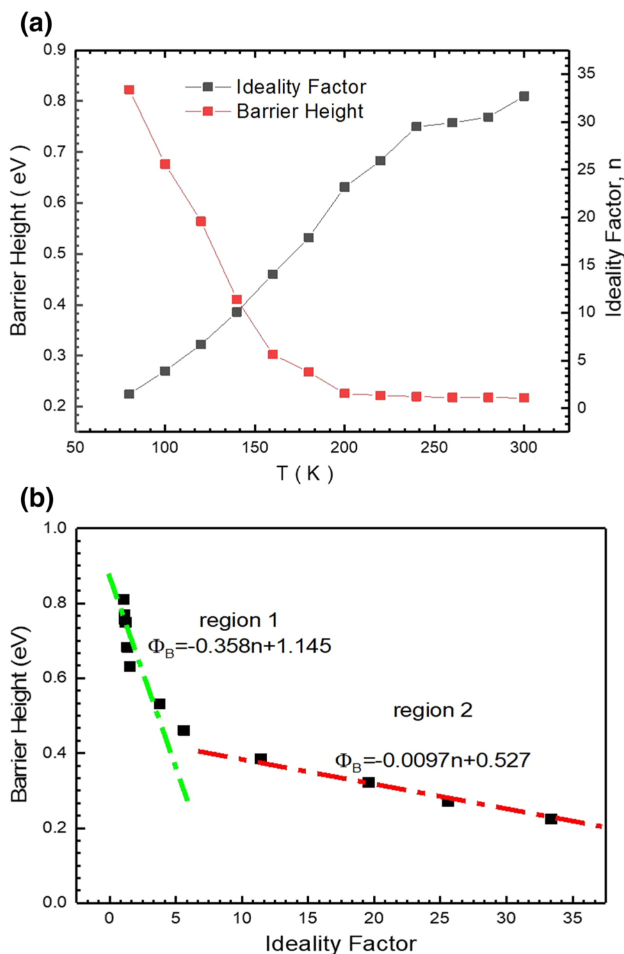

Fig. 2 (a) Temperature dependence of Φ_{b0} and n, and (b) relation between these two parameters.

$I - V$ relation can be modified with the presence of n values greater than unity, and this parameter can be calculated from the corresponding diode equation (Eq. 1) as,[46]

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right) \tag{3}$$

At the same voltage region of interest with Φ_{b0} analysis, the slope of the linear portion of Fig. 1 is used to reach n values for each temperature step. In the temperature interval of 80–300 K, they are found in the range from 33.4 to 1.1 (Table I) where there is an inverse proportionality between this parameter and temperature. The inverse change in the obtained n values with temperature can be found in Fig. 2a and similar to the observed behavior in the Φ_{b0} values, this variation is the indication of effects of interfacial barrier patches at the junction.[9] According to the temperature dependence of these two parameters, the relation between them is also presented in Fig. 2b. At low temperatures, increasing n values is the result of an increase in deviation

from linearity and that can be explained with the change in the path of the carrier flow at low temperatures. That is, when the charge carriers cannot gain enough energy to overcome the main barrier, the flow is directed to the low barrier patches distributed in the background barrier height. Since thermal activation is not sufficient to pass this barrier, it is possible to observe current flow across the MS junction using these patches. This temperature dependence is associated with the deviation from ideality with an increase in the effect of inhomogeneity at the interface for low temperatures. It is possibly due to the surface states originating from defects in the active layer, unintentional interface inhomogeneity, presence of native interfacial layer and interface trap states at the MS junction.[16,40] With an increase in temperature, the effect of the TE mechanism becomes dominant and at around room temperature, n value reaches to unity. This condition can be observed with the dominant effect of thermal activation on the other mechanisms that supports the flow through the main barrier.

Under the aim of improvement in diode behavior, together with high rectifying contact and near-ideal barrier formation to limit reverse leakage current, low parasitic resistance on the path of current flow is required.[39] According to Ohm's law ($R_i = \partial V/\partial I$), parasitic resistance (R_i) values are derived from the experimental $I - V$ values at each temperature.[16] The downward curve at both forward and reverse voltage regions gives saturation state where R_i is dominant in the current flow. Thus, saturation at high forward bias voltage originates from effects of R_s whereas shunt resistance (R_{sh}) can be obtained at zero-bias point in the $I - V$ plot.[22] Using Ohm's relation, the calculated values are presented in Fig. 3a where they are around 10 Ω and 10^6 Ω for R_s and R_{sh}, respectively. The obtained values are close to the expected values for high performance diode structure. In literature, these values are reported in the same order of magnitudes for similar MS diodes.[16,22] Both of these resistances are strong functions of temperature and there is a decrease in these values with increase in temperature. This can be attributed to the lack of free charges due to the presence of trap centers at the diode interface.[47]

The nonlinearity in the forward current flow indicates a saturation behavior in the high forward bias region by the presence of R_s. It can be revealed due to the sum of the resistance effects observed in contact regions, as well as layer materials.[34,38] Although these values are derived from the parasitic resistance relation as given in Fig. 2, the experimental values can also be obtained according to Cheung's functions as,[48]

$$\frac{dV}{d\ln(I)} = IR_s + n\left(\frac{kT}{q}\right) \quad (4)$$

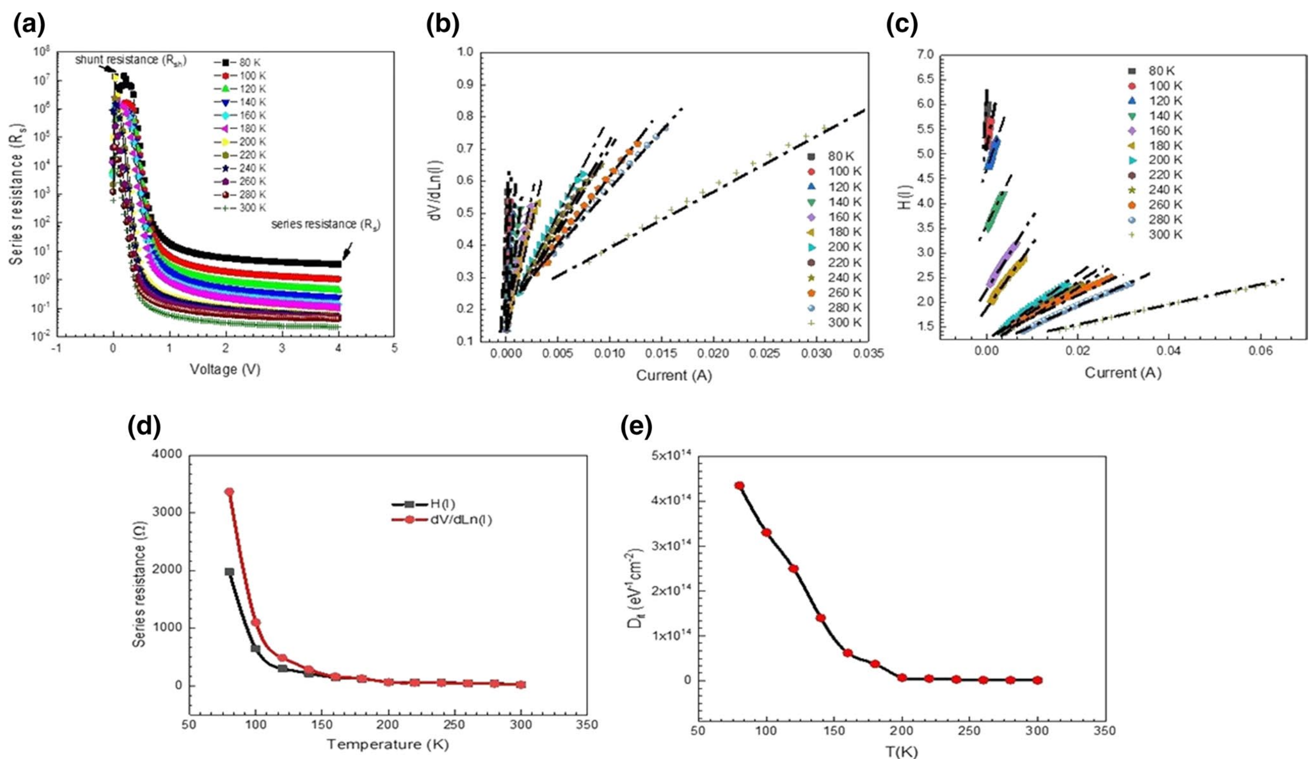

Fig. 3 (a) R_i versus V plot, (b) Cheung's $dV/dln(I)$ versus I plot, (c) Cheung's $H(I)$ versus I plot, (d) R_i values derived from Cheung's functions, and (e) D_{it} values as a function of temperature.

and

$$H(I) = q\Phi_{b0} + IR_s = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{5}$$

These are expressed as the Cheung equations where R_s values can be calculated by using $dV/dln(I)$ versus I (Fig. 3b) and $H(I)$ versus I (Fig. 3c) plots applying Eqs. 4 and 5, respectively.[49] Then, the obtained R_s values from the plots are shown in Fig. 3d. As a result, these values are listed in Table I as a function of operating temperature. At low (80 K) and high (300 K) temperature limits, they are in the range of about 10^3 Ω and 10 Ω, respectively. Both results are in agreement with magnitude and also with the values derived from Ohm's relation. This observation verifies the accuracy of the experimental analysis. This result is in Fig. 3c is in an inverse relation between R_s values with temperature. This temperature dependence can be evaluated within the observed behavior of n values due to lack of free-carrier concentration at low temperatures.[4]

Together with the effects of these resistance, interface behavior at the junction also guides current flow though the diode.[50] From the $I - V$ measurements at the temperatures between 80 K and 300 K, distribution of the interface trap states (D_{it}) at the MS junction is calculated as,

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{w_d} + qD_{it}\right) \tag{6}$$

where δ is the approximated depth of the interface, w_d is depletion length, ε_i and ε_s are the relative dielectric constants of junction interface and semiconductor layers, respectively.[46,50,51] Therefore, depending on the temperature effect on n, D_{it} values are derived at each temperature step and the result is presented in Fig. 3e. There is a continuous decreasing in the obtained values with increasing temperature. This variation as a response to the increase in temperature is associated with the thermal effect on surface states and trap levels at the interface.[52–56]

In Fig. 4, the relation between Φ_{b0} and n is given at each temperature of interest. The obtained values are in an inverse relation depending on their temperature dependence. There is an increasing trend in Φ_{b0} values from 0.22 eV to 0.81 eV and n values decrease from 33.4 to 1.1 with temperature. This observation is related to the carrier motion in the junction with an increase in temperature, whereas the variations in both Φ_{b0} and n values are the results of possible deviation from the TE controlled flow mechanism.[45] The linear behavior of the plot (Fig. 2b) can also be attributed to the lateral inhomogenetiy of the barrier.[16,57] Two independent correlations in linearity verifies the requirement of the double GD model where best linear fits to the experimental values result in 0.79 eV and 0.52 eV at the condition of $n = 1$. These barriers indicate two different types of charge carrier

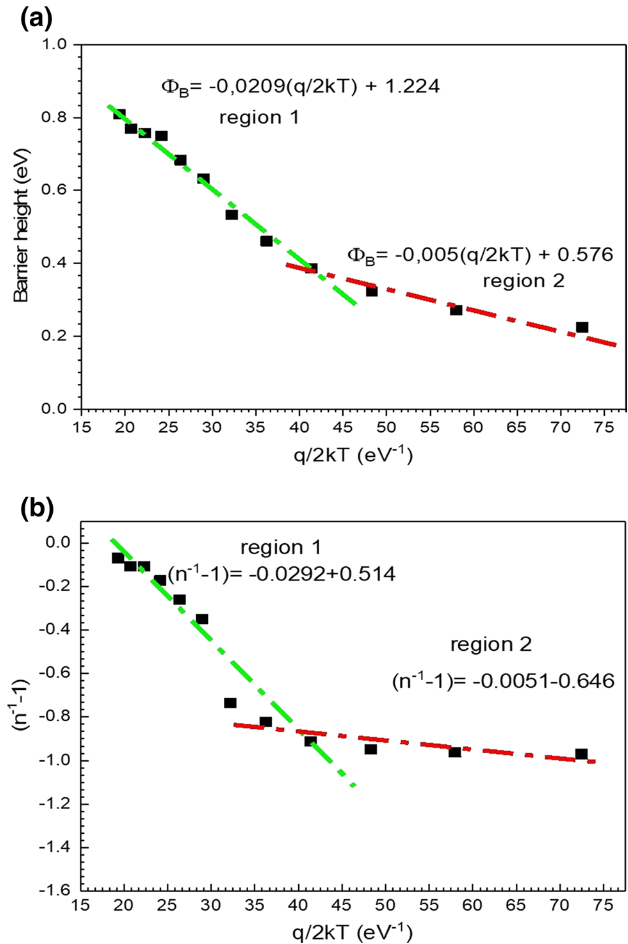

Fig. 4 (a) Φ_{b0} versus $q/2kT$ and (b) $(n^{-1} - 1)$ versus $q/2kT$ plots of the diode.

motion at two different temperature regions, from 80 K to 140 K and from 160 K to 300 K, respectively. Although both show negative coefficients of temperature, there is not enough evidence to support tunneling via surface states.[27] Thus, the linear relation between these two parameters is consistent with the assumption on barrier irregularity.[41] The response of the junction interface causes potential variation which is associated with the presence and localization of low barrier patches around the main barrier height.[45] Therefore, temperature variation affects the interface trap levels due to the localized patches and they direct the current path to ways other than the background homogeneous barrier at low temperatures.

As the main diode parameters, temperature-dependent values of Φ_{b0} and n are derived from Eq. 1. Although it is the modified model of the pure TE mechanism with the contribution of n and R_s, depending on the experimental results, there is also an abnormal deviation from the homogeneous barrier.[34] At this point, it is found that the possible barrier deformation is related to the presence of additional barrier

regions in a GD around the main barrier height. Then, the assumption on the transport mechanism can be re-evaluated by the contribution of barrier inhomogeneity with localized low barrier patches as,[40]

$$I = AA^*T^2\exp\left[\left(-\frac{qV}{kT}\right)\left(\overline{\Phi}_{b0} - \frac{q\sigma_0^2}{2kT}\right)\right]\exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (7)$$

where the parameter I_0 can also be re-expressed as,

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{ap}}{kT}\right) \quad (8)$$

The mean value of the barrier ($\overline{\Phi}_{b0}$) with standard deviation (σ_0) of the localized patches can be described by the following relation,

$$\Phi_{ap} = \overline{\Phi}_{b0} - \frac{q\sigma_0^2}{2kT} \quad (9)$$

where Φ_{ap} is the notation to underline that it is the apparent barrier height obtained from the experimental $I - V$ curves depending on temperature change.[43,58] Distribution of the patches in homogeneous barrier formation is included in Eq. 7 where it is assumed to follow a Gaussian function. In that case, there is a high background barrier height defined as $\overline{\Phi}_{b0}$ and the low barriers are localized around this barrier with σ_0 according to the GD approximation. The variation in σ_0 values with temperature can be neglected in the evaluation of barrier height.[37] The existence of double GD in MS junction barrier can be ascribed to the nature of inhomogeneties valid in two different temperature regions. This may involve change in the chemical characteristics of the interface, charge carriers at the interface trap states and non-stoichiometry of the material surfaces.[40] Based on the GD assisted TE model, the relation in Eq. 9 can be evaluated by Φ_{b0} versus $q/2kT$ plot (Fig. 4a). The observed linear behavior verifies the effects of this conduction mechanism where the parameters $\overline{\Phi}_{b0}$ and σ_0 can be derived from the zero-point intercept and slope of the lines. These regions obey different linear functions with high correlation coefficients. Thus, the obtained values are 1.22 and 0.58 eV, respectively. In the GD function, the σ_0 parameter is a measure of the deviation from the barrier homogeneity and low value of σ_0 results in high diode performance.[39] With increase in the axis of $q/2kT$, the calculated value is 0.15 eV in $\overline{\Phi}_{B0} = 1.22$ eV and 0.07 eV in $\overline{\Phi}_{B0} = 0.58$ eV, indicate 12.3 and 12.1% deviation from these mean values, respectively. The presence of these two different temperature-dependent behaviors can be attributed to a double GD of barrier height in the diode due to the interfacial inhomogeneity.[8] This is the case for potential current flow though low barrier patches since the carriers cannot be sufficiently activated to pass the main barrier height at low temperatures. Then, it is expected that they are directed along the low barrier height regions at the junction.[41]

Similar to the apparent barrier heights in the diode, n_{ap} is the apparent ideality factor and it can be defined as,

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \quad (10)$$

where the characteristic plot of $\left(n^{-1} - 1\right)$ versus $q/2kT$ also provides evidence for the GD model with two straight lines (Fig. 4b). In this equation, ρ_2 and ρ_3 are the coefficients that carry information for temperature and voltage dependence to analyze deformation in barrier height.[59] These coefficients are calculated by modeling the obtained curve with a linear function for each line. The results are − 0.514 and 0.646 obtained at the intercepts give the values of ρ_2. On the other hand, the slopes of the linear portions in the $\left(n^{-1} - 1\right)$ versus $q/2kT$ curves are the values of ρ_3 which are 0.0292 and 0.0051 in two different temperature regions (80–140 K and 160–300 K). These parameters can also be used to express linear relation in mean barrier height and its standard deviation with voltage as,

$$\overline{\Phi}_B = \overline{\Phi}_{B0} + \rho_2 V \quad (11)$$

and

$$\sigma = \sigma_0 + \rho_3 V \quad (12)$$

where the linearity in n values is adapted to explain the bias-dependent barrier, parameters modified by the GD model.[45] Depending on these results, the linearization of Eq. 8 gives,[4]

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln\left(AA^*\right) - \frac{q\overline{\Phi}_{B0}}{kT} \quad (13)$$

According to this expression, the modified Richardson plot of $\left(I_0/T^2\right) - \left(q^2\sigma_0^2/2k^2T^2\right)$ versus q/kT (Fig. 5) is in a good linearity in both temperature regions in the range 80–140 K and 160–300 K. The presence of two linear regions in this characteristic plot can be the indication of lateral inhomogeneity of the diode barrier. From Eq. 13, the intercept of the $\left(I_0/T^2\right) - \left(q^2\sigma_0^2/2k^2T^2\right)$ axis at the ordinate gives the value of A^*. These two different linear variations give different A^* values as 450 and 147 A/cm^{-2}K^{-2} at temperature regions of 80–140 K and 160–300 K, respectively. Difference from the real effective mass can cause deviation from the theoretical value of A^* (about 146 A/cm^{-2}K^{-2}).[43] The experimental value at the region of 160–300 K is in close agreement with literature

on the similar SiC based MS diodes.[16,39,60] Additionally, the values of $\overline{\Phi}_{B0}$ are obtained from the slope of these two straight lines as 1.22 and 0.51 eV at comparatively low and high temperature regions of interest, respectively. The splitting in the given characteristic plot indicates interfacial potential fluctuations and also possible defects in the semiconductor layer cause irregular barrier area.[39] The compatible results for this barrier parameter obtained from

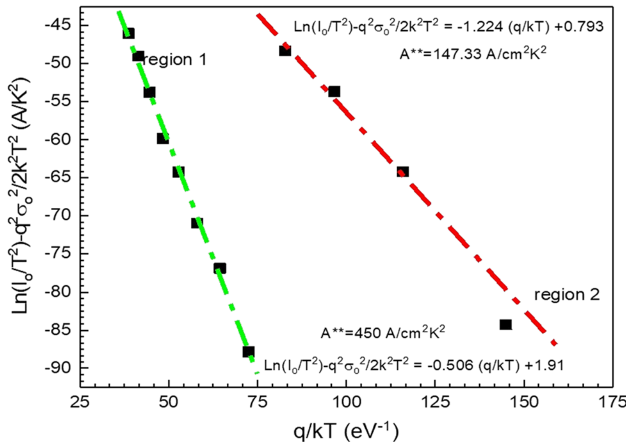

Fig. 5 Modified Richardson plot of the diode

Eqs. 9 and 13 are directly related to the success in modeling of the conduction mechanism by TE theory supported by GD of inhomogeneous barrier height.[61] In consideration of a double GD of barrier height for inhomegeneous Schottky type diodes, Φ_{ap} can be expressed as,[62–65]

$$\Phi_{ap} = -kTln\left[\rho_1 \exp\left(\frac{-\overline{\Phi}_1}{kT} + \frac{\sigma_1^2}{2k^2T^2}\right) + \rho_2 \exp\left(\frac{-\overline{\Phi}_2}{kT} + \frac{\sigma_2^2}{2k^2T^2}\right)\right] \tag{14}$$

where two different Gaussian functions can be incorporated into the relation with their characteristic standard deviations as σ_1 and σ_2, weight coefficients as ρ_1 and ρ_2 ($\rho_2 = 1 - \rho_1$), and mean values as $\overline{\Phi}_1$ and $\overline{\Phi}_2$, respectively.[65] According to this relation, the theoretical barrier height versus $1000/T$ plot is obtained as given in Fig. 6 and the characteristic Gaussian parameters are found by linear fitting processes based on Eq. 1 as $\rho_1 = 4.84 \times 10^{-4}$, $\overline{\Phi}_1 = 1.203$ eV, $\sigma_1 = 144.5$ meV, $\overline{\Phi}_2 = 0.571$, σ_2 =70 meV. This front plot in Fig. 6 also presents a good agreement between the experimental data with the theoretical fitting analysis over temperature range of interest, and the barrier height inhomogeneity of the Au/4H n-SiC diode can be well described by a double GD expression before

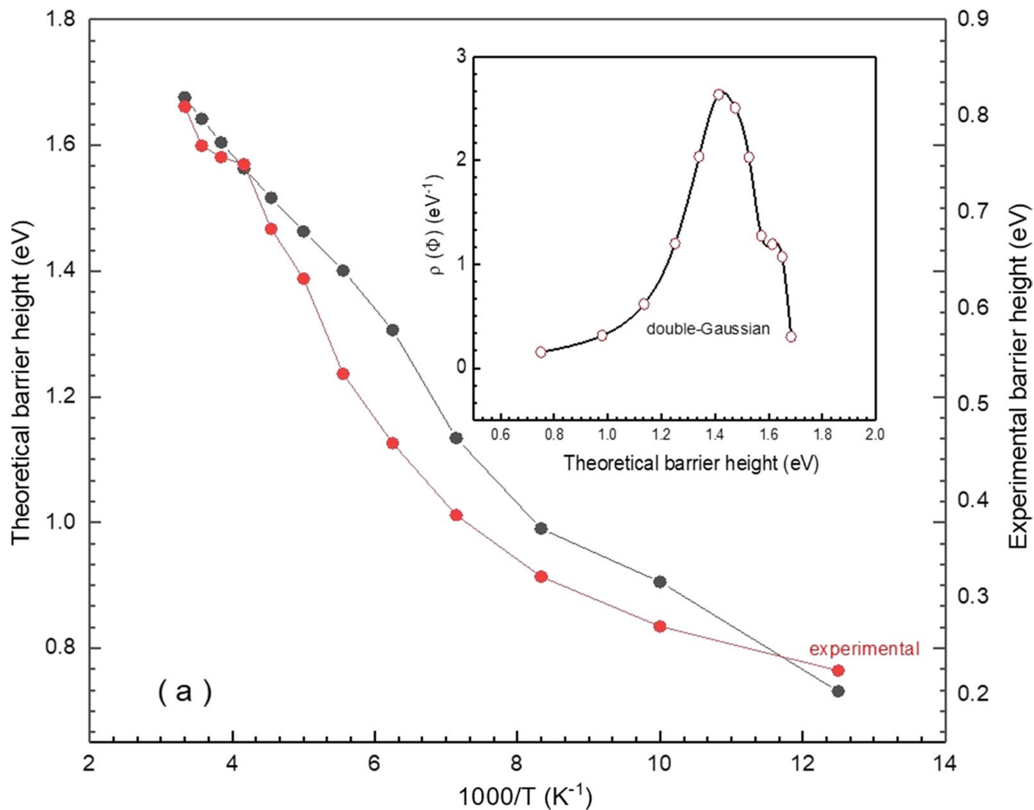

Fig. 6 Barrier height versus 1000/T plot. *Inset*: Barrier height distribution.

correction in terms of interfacial contribution. In addition, the double GD barrier height distribution function can be defined as,[62–65]

$$\rho(\Phi) = \frac{\rho_1}{\sigma_1\sqrt{2\pi}}\exp\left[\frac{-\left(\Phi-\overline{\Phi}_1\right)^2}{2\sigma_1^2}\right] + \frac{\rho_2}{\sigma_2\sqrt{2\pi}}\exp\left[\frac{-\left(\Phi-\overline{\Phi}_2\right)^2}{2\sigma_2^2}\right] \tag{15}$$

where two different distribution functions, $\rho_A(\Phi)$ and $\rho_B(\Phi)$, are shown. The theoretical barrier height functions of $\rho(\Phi)$ for Au/4H n-SiC after interfacial correction can be obtained by using the Gaussian parameters in Eq. 14 as fitting results for two Gaussian functions. Thus, the plot of $\rho(\Phi)$ versus theoretical barrier height is given as inset of Fig. 6. As shown in this figure, the obtained $\rho(\Phi)$ curve indicates a double GD behavior.[61] The presence of a double Gaussian on this type of diode can be experimentally ascribed to the chemical treatment of the semiconductor surface.[66,67] It is also reported that relatively many patch contacts with low barriers due to various contact structures can cause the second GD.[62,63] In addition, it is observed that this type of diode inhomogeneity strongly depends on the metal/semiconductor solid phase reaction.[62–65]

The forward bias carrier conduction is directed through the MS junction by the effect of the GD assisted TE mechanism. At the negative bias region, the increase in barrier height with temperature also affectis leakage current flow. Temperature dependence of barrier indicates that the roles of TE and tunneling over the Schottky barrier are negligibly small on leakage current behavior. Since reverse bias supports electric field in the junction, the carrier recombination process in the depletion region and image force lowering of the barrier can be effective in the current flow.[68] As given in Fig. 7a, there is a linear relation between current flow under reverse bias voltages and square root of the applied voltage, $V^{1/2}$ in the characteristic semi-logarithmic plot. The observed Arrhenius-type behavior of the reverse current-density (J_r) can be modeled according to the Poole–Frenkel (PF) effect, and the reverse bias $I-V$ characteristics of the diode can be evaluated as;[69,70]

$$J_r = KE_b\exp\left(-\frac{q\left(\emptyset_t - \sqrt{\beta_{PF}E_b}\right)}{kT}\right) \tag{16}$$

where $\emptyset_t$ is the barrier height in the emission process of electrons from trapped states and K is a constant depending on the conductivity and concentration of free carriers.[69,71] It is the effect on the carrier transport mechanism where emission from defect states directs the current flow with a more effective way than TE from the metal.[68] In Eq. 16, β_{PF} is the characteristic field lowering coefficient defined by permittivity of free space (ε_0) and ε_i arose from the effect of interface as,

$$\beta_{PF} = \frac{1}{2}\left(\frac{q^3}{\pi\varepsilon_i\varepsilon_0}\right) \tag{17}$$

Equation 16 is a field-dependent conduction model based on generation-recombination of carriers at the interface. Under bias voltage, electric field (E_b) in the semiconductor barrier at the MS interface is found to have a linear dependence of $ln(J_r/E_b)$ and $\sqrt{E_b}$ at each temperature (Fig. 7b). It can be concluded from this linear behavior that the electric field is enhanced by TE from a trapped state into a continuum of electronic states at the MS interface.[72] Therefore, the linear variation in Fig. 8 can be best fitted to the relation derived from Eq. 16 as,[69,71]

$$\ln\left(J_r/E_b\right) = R(T)\sqrt{E_b} + \mathrm{S(T)} \tag{18}$$

where R(T) $= q\beta_{PF}/kT$ is the temperature-dependent leading coefficient to the change in $\ln(J_r/E_b)$ with $\sqrt{E_b}$ and $S(T) = -q\emptyset_t/kT + \ln(K)$ is also a parameter change with a temperature, whereas it has a fixed value to the change with $\sqrt{E_b}$. These parameters are calculated from the slope and vertical intercept of the plot given in Fig. 7b, respectively. The values of R(T) and S(T) are presented in Fig. 8 as a function of inverse temperature. As a result of this fitting process, ε_s is estimated from the slope of the R(T) versus $1/T$ plot in Fig. 8a and it is found to be 10.53 which is in a good agreement with the value for n-4H SiC.[10] In addition, $\emptyset_t$ is derived from the slope of the obtained linear function of S(T) as 0.107 eV (Fig. 8b). The presence of charges fixed in the PF barrier associated with the interfacial traps is associated with the leakage current in the diode. Therefore, PF emission from the trapped states within the semiconductor and also states near the MS interface into continuum of states dominate the current flow in the reversed bias region.[73,74]

Conclusion

An Au/n-4H SiC MS-type Schottky diode is fabricated by Au metal rectifying contact evaporation on an n-4H SiC active semiconductor layer, and it is also used as a back ohmic contact after post-thermal treatment. The $I-V$ curves at each temperature step between 80 K and 300 K verify the accuracy in rectifying behavior and the results are used to derive Φ_{b0} and n values. The calculated Φ_{b0} values increase whereas n values decrease with increasing temperature. These responses with temperature reveal that there is a deviation from ideal TE model with barrier inhomogeneity. In addition, at low temperatures the charge carriers are found to surmount the barrier of the small patches distributed in

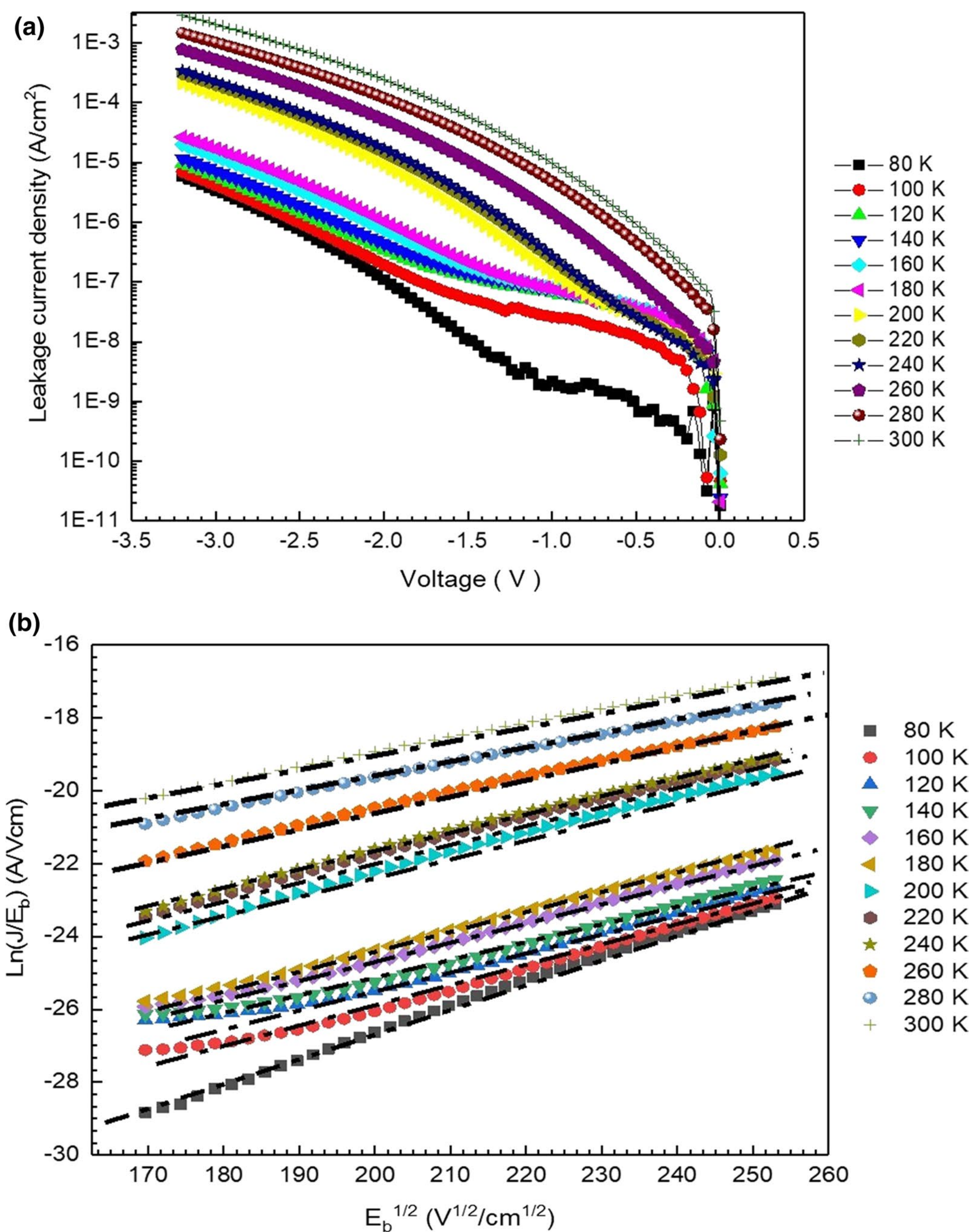

Fig. 7 (a) Semi-logarithmic J_r versus $V^{1/2}$ and (b) characteristic $\ln(J_r/E_b)$ versus $\sqrt{E_b}$ plot of the diode.

the main barrier height. At the limits of bias voltages, R_s and R_{sh} values are derived from Ohm's law and R_s values are found to be around an order of 10 Ω while R_{sh} values are on the order of 10^6 Ω. Additionally, R_s values are obtained by Cheung's functions and they show a decreasing behavior with increasing temperature. As a result of the temperature dependence of diode parameters, the non-ideal TE mechanism in the forward bias region, the GD model is assumed to be dominant on the carrier conduction through the patches with low barrier height. The plots of modified TE relation with GD approximation are correlated with two barrier height distributions. Additionally, leakage current mechanism of the diode is modeled by a field emission model. The characteristic $\ln(J_r/E_b)$ vs. $\sqrt{E_b}$ plot reveals that with the extension in the electric field, PF emission at the MS interface dominates the current flow at the reverse bias region. According to this plot, the $R(T)$ and $S(T)$ are obtained. From their relation with temperature, $\emptyset_t$ and ε_s values are approximated as 0.107 eV and 10.53, respectively.

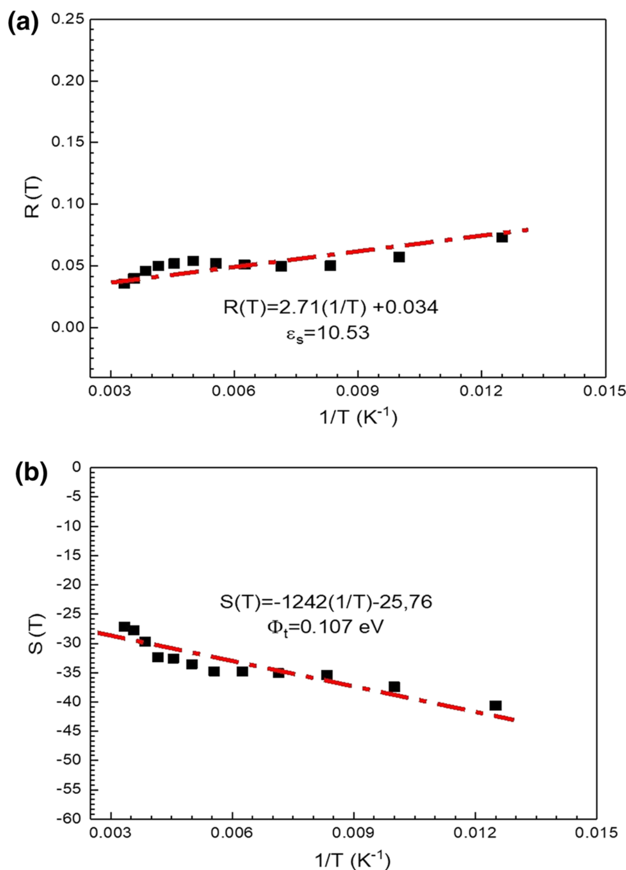

Fig. 8 (a) R(T) versus $1/T$ and (b) S(T) versus $1/T$ plots of the diode.

Data Availability The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interest The authors declare that there are no conflicts of interest regarding the publication of this paper.

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