Journal of Electronic Materials (2021) 50:7143–7149
https://doi.org/10.1007/s11664-021-09225-8

ORIGINAL RESEARCH ARTICLE

# Optimization of Thick Photoresist for Uniform Thickness in RF MEMS Applications

**Anuroop Bajpai**[1,2] · **Kamaljit Rangra**[3] · **Deepak Bansal**[1,2]

Received: 5 July 2021 / Accepted: 7 September 2021 / Published online: 30 September 2021
© The Minerals, Metals & Materials Society 2021

## Abstract

Micro-electromechanical systems (MEMS)-based devices comprise suspended structures. A sacrificial layer is required to realize these structures. Usually, metal and dielectric materials are used as sacrificial layer materials. Metallic sacrificial material has a selectivity problem, whereas dielectric materials require higher deposition temperatures. Hence, in the present paper, photoresist (PR) material is used as the sacrificial layer. PR requires low-temperature processing and has no selectivity issues. Hence, photoresists are preferred as sacrificial layer materials. In the CMOS fabrication process, thin photoresists such as S1818, S1813, and AZ1505 are used. In these photoresists, the processing wafers are placed in a vertical position during patterning, which occupies less space. The recipes of such photoresists are well optimized for a uniform thickness across the wafer. However, special thick photoresists are used as a sacrificial layer for MEMS devices. These thick photoresists reflow in the vertical position and lead to non-uniform thickness; consequently, the yield is decreased. This paper has optimized a special thick photoresist (HiPR 6517) for RF MEMS SPST switches for better yield and uniformity. The measured pull-in voltage and the switch's resonant frequency are 13.00 V and 12.32 kHz, respectively. The fabricated switch offers isolation and insertion loss better than − 35 dB and − 1 dB at 24.5 GHz, respectively.

**Keywords** Lithography · microelectromechanical devices · switches

## Introduction

RF MEMS switches have great potential to replace the existing counterparts such as PIN diodes and coaxial switches. These switches have no leakage current in the OFF state and offer high isolation.[1–6] At present, PIN diodes, CMOS, and GaAs MESFET-based SPST switches are used in transceiver systems.[7,8] MEMS technology-based SPST RF switches can be a better alternative to the existing switches used in transceivers.[9–13]

MEMS switches consist of both suspended mechanical (cantilevers, bridge, etc.) and electrical parts. The suspended structures are the critical elements of RF MEMS switches. A sacrificial layer is used to fabricate these mechanical hanging structures. Metals (copper, nickle, etc.), silicon dioxide ($SiO_2$), and silicon nitride ($Si_3N_4$) are broadly used as the sacrificial layer material.[14–19]

Copper, nickel, and other metallic materials as a sacrificial layer have selectivity challenges during the release of the hanging structures.[20–22] Dielectric materials such as silicon dioxide ($SiO_2$) and silicon nitride ($Si_3N_4$) required high deposition temperature and selective etching process during removal of the sacrificial layer.[23–26] Hence, metallic and dielectric materials are not compatible with most MEMS devices. The photoresist-based sacrificial material is another good alternative for MEMS devices. It can be deposited easily by spin coating and has a low processing temperature. The photoresist-based sacrificial layer is either removed by dry etching (plasma etching) or wet etching (Piranha solution).[17,18,23,27]

Based on gap and device, a photoresist for the sacrificial layer is chosen. For thin photoresists such as S1800, S1300, or AZ1505, recipes are optimized and the layer is easily removed with acetone.[17,18,28] However, optimization of thick photoresists suchh as HiPR 6517 is required. The standard

✉ Anuroop Bajpai
anuroopbajpai@gmail.com

1 Academy of Science and Innovative Research (AcSIR), Ghaziabad 201002, India

2 CSIR-Central Electronics Engineering Research Institute, Pilani 333031, India

3 Indian Institute of Technology-Jodhpur, Jodhpur 342037, India

patterning process involves the vertical placement of wafers during baking. The same process for thick photoresists leads to non-uniform thickness across the wafer. Researchers have published literature on sacrificial layer thickness, profile, and edge coverage optimization.[18] However, the effect of the non-uniform thickness of the sacrificial layer on the device yield is least explored. In this paper, HiPR 6517 is selected as the sacrificial layer material and optimized to achieve uniform thickness across the wafer for a better yield. The pull-in voltage, mechanical resonance frequency, insertion loss, and isolation of the fabricated SPST RF MEMS switch are measured.

## HiPR Thickness Optimization

An RF MEMS switch is an essential building block of most RF MEMS devices such as phase shifters, varactors, T-matrixes, and tunable filters. Hence, in this paper, the sacrificial layer is optimized for an RF MEMS switch to cover most RF devices.

In the RF MEMS switches, the pull-in voltage depends upon the gap between the actuation electrode and the suspended bridge. A large gap leads to a larger pull-in voltage, and a small gap leads to a lower pull-in voltage. But small gap introduces the capacitive loss and degrades the switch's RF performance. The bridge's gap is optimized such that the pull-in voltage of the switch should be minimal without degrading the switch's RF performance.

The HiPR 6517 photoresist is optimized for use as a sacrificial layer of the RF MEMS switch. Spin coating is used for the deposition of the film. The spin-coating time and acceleration are fixed to 60 s and 1000 rpm, respectively. The ambient temperature of the spin coating room is fixed at 18°C. The HiPR is spin-coated at different RPMs to achieve the desired thickness. The approximate spin-coated thickness (T) of the photoresist is given by the following Eq. 1:[29]

$$T = \frac{KC^{\beta}\eta^{\gamma}}{\omega^{\alpha}} \tag{1}$$

where $K$—overall calibration constant, $C$—polymer concentration, $\eta$—intrinsic viscosity, and ω is the spin-coating speed (rpm). $\alpha$, $\beta$, and $\gamma$ are the exponential constants.

The spin-coated wafers are placed vertically in the specially designed boat, as shown in Fig. 1. The wafer's vertical placement is preferred as it occupies less space to accommodate the multiple wafers and ease of handling. We have taken five samples in a single run. All the wafers are spin-coated one by one, which takes around 6-7 mins. During this duration, wafers are kept at 18°C in the vertical position. After that, wafers are placed in an oven for pre-baking at 90°C for 25 min.

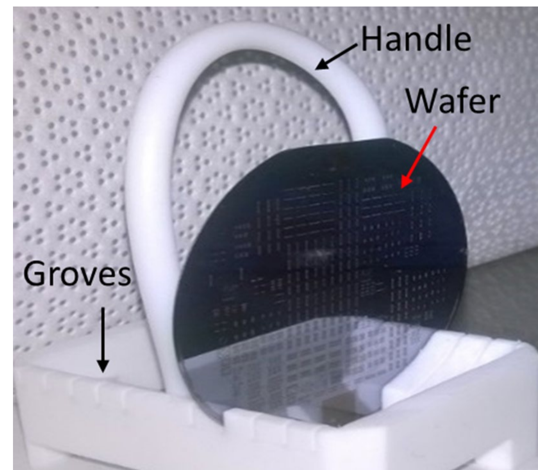


**Fig. 1** The vertical placement of the wafer.

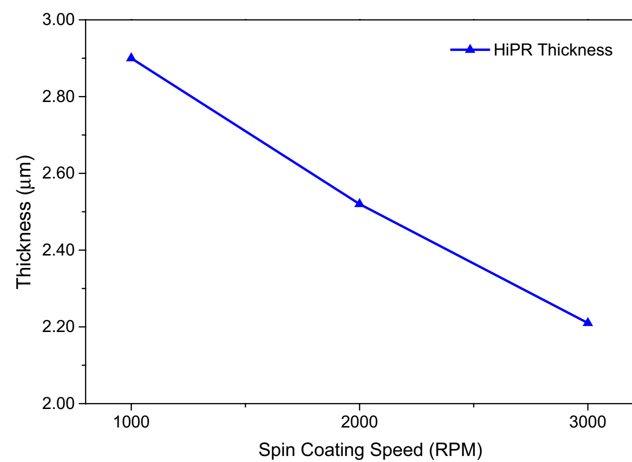


**Fig. 2** RPM versus thickness variation of HiPR 6517 photoresist.

The thickness of the spin-coated HiPR 6517 layer is measured using an optical surface profiler. The advantage of an optical surface profiler is that it does not require any step height in the photoresist for thickness measurement. The thickness measured after the pre-baked HiPR 6517 photoresists at different coating speeds is shown in Fig. 2. The required thickness of the HiPR 6517 sacrificial layer for the RF MEMS switch is achieved at 3000 rpm.

## Fabrication of the RF MEMS Switch

The capacitive SPST RF MEMS switch is fabricated using surface micromachining technology with the help of a recipe optimized for the sacrificial layer described in "HiPR Thickness Optimization" section. The design and stress-related concerns of the switch are addressed in the earlier

publication.[30] The complete fabrication process of the capacitive SPST switch is illustrated in Fig. 3. It comprises five levels: lithography, oxidation, diffusion, metallization, and etching stages.

The selection of substrate plays a vital role in the RF performance of the switch. Hence, to achieve better RF performance, a highly resistive (> 4000 Ω cm) silicon wafer of 280-µm thickness is chosen as a substrate material (Fig. 3a). The switch's fabrication procedure starts with the standard microelectronics fabrication cleaning procedure to remove the wafer's contamination. A 1-µm-thick silicon dioxide layer is thermally grown over silicon for surface passivation (Fig. 3b), and a 0.4-µm-thick polysilicon layer is deposited over the silicon oxide layer by using low-pressure chemical vapor deposition (LPCVD) to define the actuation electrodes and bumps (Fig. 3c, d). Subsequently, the underpass area of the transmission line of 200-nm-thick gold (Au) is defined by using lift-off (Fig. 3e). A 0.1-µm-thick silicon dioxide layer is deposited using plasma enhanced chemical vapor deposition (PECVD). This silicon dioxide layer prevents the electrical shorting between the actuation electrode and bridge in a downstate position (Fig. 3f). A 0.1-µm-thick Cr/Au floating metal layer is patterned using a lift-off process (Fig. 3g). After that, a 2-µm-thick sacrificial layer of HiPR 6517 photoresist is spin-coated and patterned to provide initial support to the bridge structure (Fig. 3h). Further, lithography of AZ 9260 is done for mold formation (Fig. 5i). A 2-µm-thick gold bridge and CPW lines are patterned using a LIGA-like process as shown in Fig. 3j. Then, an AZ 9260 mold is removed in the acetone, as shown in Fig. (Fig. 3k).

The HiPR 6517 sacrificial layer is detached from underneath the bridge using wet etching. Piranha solution in a 3:1 ratio is used to eradicate the sacrificial layer. The RF MEMS switch's bridge structure is finally released with a critical point dryer (CPD), as shown in Fig. 3l. The optical image of the released wafer is shown in Fig. 4.

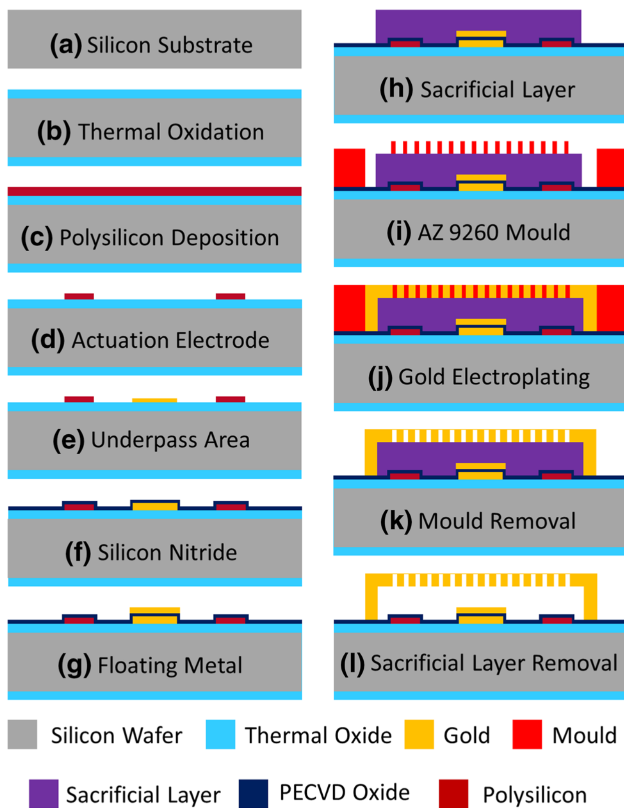


**Fig. 3** (a-l) Fabrication process flow of the RF MEMS Switch.

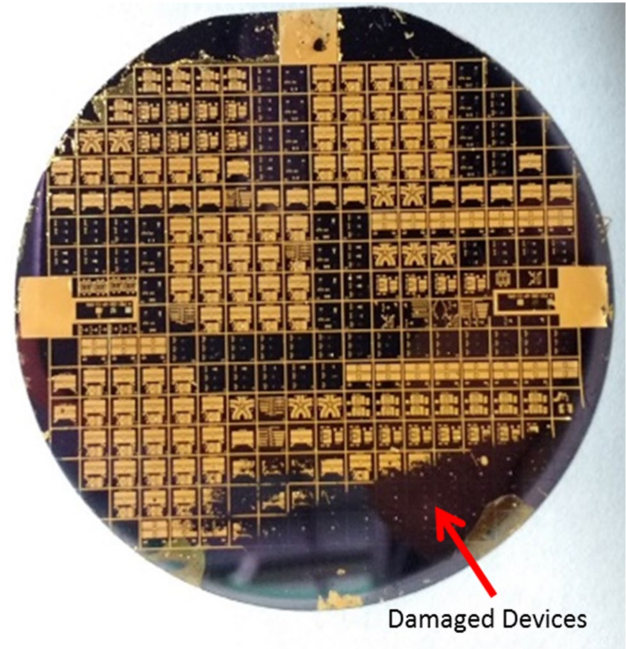


**Fig. 4** Top view of the released wafer after vertical placement.

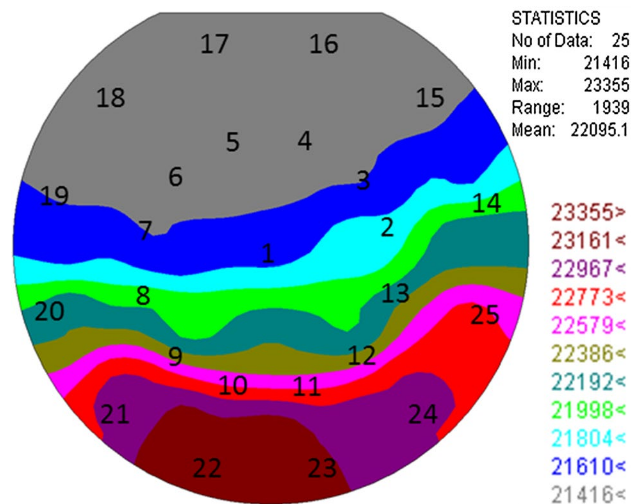


**Fig. 5** Thickness profiling of the vertically placed wafer.

The devices located at the bottom side are damaged in the released wafer, as shown in Fig. 4. Hence, the yield of the switches degrades. The reason for this damage is the non-uniformity in the sacrificial layer. The HiPR recipe is optimized to make it uniform across the wafer and improve the yield.

## Photoresist Uniformity Optimization

The thickness uniformity of the spin-coated sacrificial layer plays a significant role in switch fabrication. The spin-coater leveling and cleaning of the substrate are done to achieve a uniform thickness profile of HiPR 6517. Further, the photoresist's thickness is measured over the 25 points on a 2-inch diameter substrate after pre-bakinng. The 2-D contour map is plotted for the visualization of the thickness uniformity. The points where the thickness has been measured are also marked in the contour maps. The contour map of the wafer is shown in Fig. 5.

From Fig. 5, it is observed that the thickness at the bottom of the wafer is high. The value of the minimum measured thickness of the HiPR 6517 sacrificial layer at the top side of the wafer is 2.1446 µm, and the thickness measured at the bottom side of the wafer is 2.3355 µm. The total thickness variation (TTV) of the photoresist is 0.1939 µm. The non-uniformity in the vertically placed wafer is due to the slow drying process of the HiPR photoresist at low temperature (at 18° C). At this temperature, the drying process of the photoresist is slow, and it starts to reflow. Hence, due to gravity, the photoresist accumulates at the lower side of the wafer, which leads to higher TTV.

Because of the greater thickness in the lower side of the wafer, the photoresist could not be resolved entirely, and some traces of the photoresists are left, which results in poor adhesion to subsequent layers. Hence, the structures are lifted off from that region during the final release, as shown in Fig. 4.

The best way to resolve this challenge is to place the wafers in a horizontal position after the photoresist coating for uniform thickness, as shown in Fig. 6.

The HiPR 6517 is spin-coated with the same optimized recipe. However, the wafers are placed horizontally instead of vertically. The thickness of the photoresist is measured over the 25 points to plot the counter map, as shown in Fig. 7. The measured thickness ranges from 2.1569 µm to 2.1901 µm, and the TTV of the spin-coated HiPR 6517 layer is 0.0332 µm.

The TTV of the horizontally placed wafer is five times less than the TTV of the vertically placed wafer. Hence, no residues remain after the HiPR 6517 developing process of the horizontally placed wafer. Thus, the wafer is released without damaging the devices, as shown in Fig. 8. The SEM micrograph of the final released capacitive SPST RF MEMS switch is shown in Fig. 9.

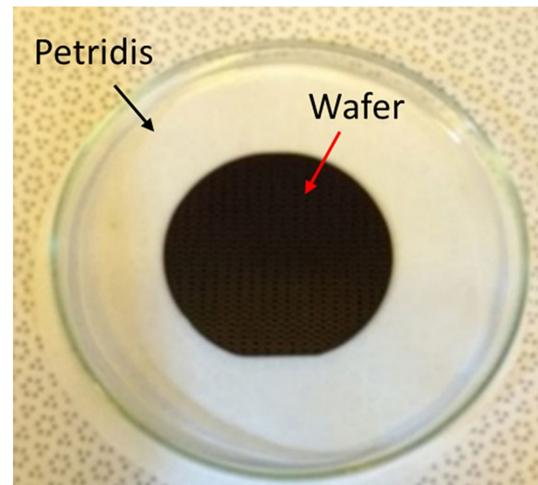


**Fig. 6** Horizontal placement of the wafer.

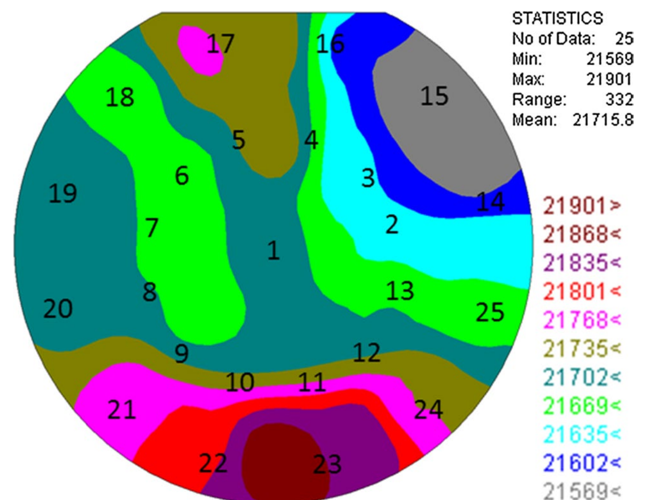


**Fig. 7** Thickness profiling of the horizontally placed wafer.

## Result and Discussion

The SEM image of the fabricated and released capacitive SPST RF MEMS switch is shown in Fig. 9. RF measurement and mechanical analysis of the switch are performed. A laser Doppler vibrometer (LDV) is used to measure the resonance frequency of the released bridge. The first resonating mode of the beam is at 12.33 kHz, shown in Fig. 10. A C-V analysis is carried out to measure the pull-in voltage of the switch by using an impedance analyzer, and a hysteresis curve is plotted for the switch, as shown in Fig. 11. The switch actuates at 13 V, and the

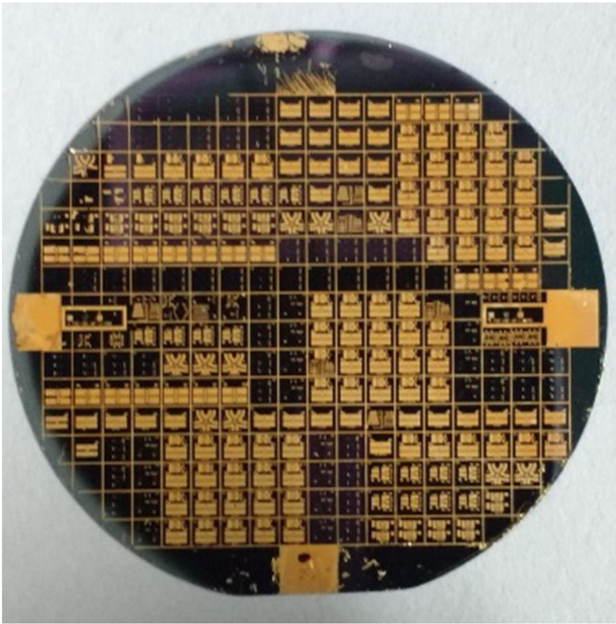

**Fig. 8** Top view of the released wafer after horizontal placement.

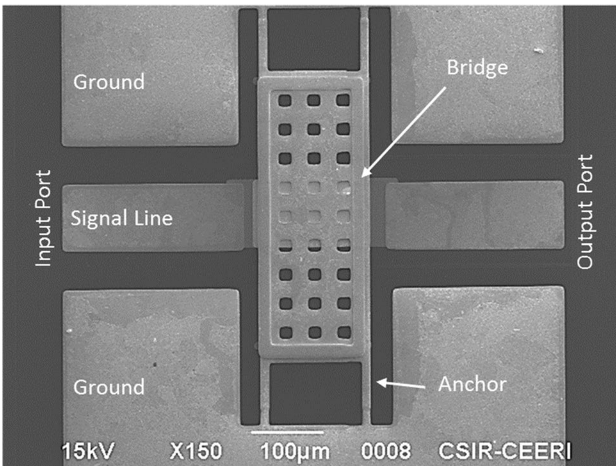


**Fig. 9** SEM image of the fabricated capacitive SPST RF MEMS Switch.

hold-on voltage is 7 V. The RF parameters of the switch are measured by using a vector network analyser (VNA), and results are presented in Fig. 12. The switch's isolation at 24.5 GHz is about – 35 dB, and insertion loss is better than – 1 dB.

The characteristics of the switch for both vertically and horizontally placed wafers are almost similar. However, the yield of the devices is increased in the horizontally placed wafer compared to vertical placement.

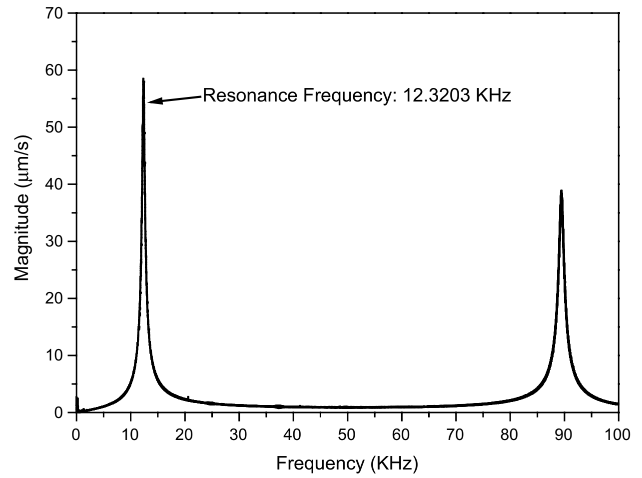


**Fig. 10** LDV measurement of the capacitive SPST RF MEMS switch.

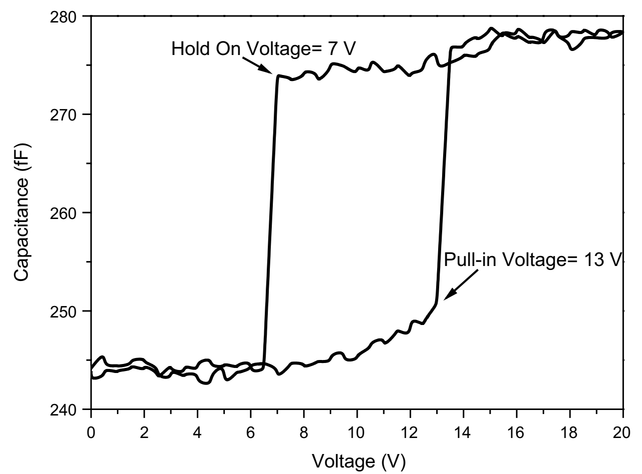


**Fig. 11** Pull-in voltage measurement of the capacitive SPST RF MEMS switch.

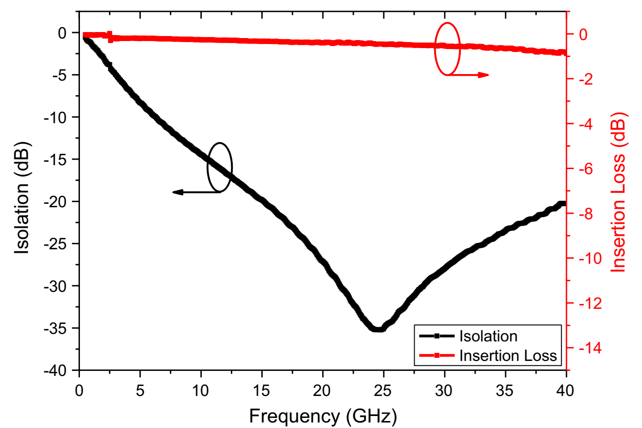


**Fig. 12** RF measurement of the capacitive SPST RF MEMS switch.

## Conclusion

In this work, low-temperature photoresist HiPR 6517 is optimized as a sacrificial layer rather than process incompatible metallic and high-temperature dielectric materials for fabricating MEMS devices. In the standard vertical placement of wafers, the thick photoresist reflows and results in non-uniformity across the wafer. The bottom side of the wafer has a greater thickness compared to the top, which damages the devices located at the bottom side of the wafer. To overcome this issue, the wafers are placed horizontally to achieve uniform thickness. The TTV of the vertically placed wafer is 0.1939 µm, while the TTV of the horizontally placed wafer is 0.0332 µm. So, the uniformity of the horizontally placed wafer increased more than 500%. Hence, the yield of the devices is also increased using horizontal placement. The fabricated switch using the optimized recipe of low-temperature thick photoresist shows excellent characteristics. The measured actuation voltage of the switch is 13 V, and the mechanical resonant frequency is 12.32 kHz. The fabricated switch offers isolation and insertion loss better than − 35dB and − 1 dB at 24.5 GHz, respectively.

**Acknowledgment** Anuroop Bajpai would like to thank CSIR-India for supporting the work.

**Conflict of Interest** The authors declare that they have no conflict of interest.

## References


1. G.M. Rebeiz, *RF MEMS* (Hoboken: Wiley, 2003). https://doi.org/10.1002/0471225282.
2. J.C.M. Hwang, Reliability of electrostatically actuated RF MEMS switches, in *RFIT 2007—IEEE International Workshop on Radio-Frequency Integration Technology* (IEEE, Singapore, 2007), pp. 168–171. https://doi.org/10.1109/RFIT.2007.4443942
3. D. Bansal, A. Bajpai, P. Kumar, M. Kaur, and K. Rangra, *J. Electr. Comput. Eng.* (2016). https://doi.org/10.1155/2016/7984548.
4. V. Mulloni, F. Solazzi, G. Resta, F. Giacomozzi, and B. Margesin, *Circuit Signal Process* 78, 323 (2014). https://doi.org/10.1007/s10470-013-0220-x.
5. J. Robert Reid, L.V.A. Starman, and R.T. Webster, RF actuation of capacitive MEMS switches, in *IEEE MTT-S International Microwave Symposium Digest* (IEEE, 2003), pp. 1919–1922. https://doi.org/10.1109/mwsym.2003.1210533
6. M. Angira, and K.J. Rangra, *Eng. Sci. Technol. Int. J.* 19, 171 (2016). https://doi.org/10.1016/j.jestch.2015.07.001.
7. P.K. Datta, X. Fan, and G. Fischer, *IEEE Trans Circuits Syst. II Express Briefs* 54, 362 (2007). https://doi.org/10.1109/TCSII.2007.895073.
8. H. Mirzajani, A.K. Ilkhechi, P. Zolfaghari, M. Azadbakht, E.N. Aghdam, and H.B. Ghavifekr, *Microelectron. J.* 69, 64 (2017). https://doi.org/10.1016/j.mejo.2017.09.004.
9. H. Qiu, H. Wang, and F. Ke, *Sensors (Switzerland)* 13, 16360 (2013). https://doi.org/10.3390/s131216360.
10. C.W. Dyck, T.A. Plut, C.D. Nordquist, P.S. Finnegan, F. Austin, I.C. Reines, and C. Goldsmith, Fabrication and characterization of ohmic contacting RF MEMS switches, in (2004), pp. 5310–5344
11. C. Palego, J. Deng, Z. Peng, S. Halder, J.C.M. Hwang, D.I. Forehand, D. Scarbrough, C.L. Goldsmith, I. Johnston, S.K. Sampath, and A. Datta, *IEEE Trans. Microw. Theory Tech.* 57, 3262 (2009). https://doi.org/10.1109/TMTT.2009.2033885.
12. J. Iannacci, M. Huhn, C. Tschoban, and H. Potter, *IEEE Electron Device Lett.* 37, 1336 (2016). https://doi.org/10.1109/LED.2016.2604426.
13. M. Angira, *Trans. Electr. Electron. Mater.* 20, 52 (2019). https://doi.org/10.1007/s42341-018-0077-x.
14. V. Mulloni, F. Giacomozzi, and B. Margesin, *Sens. Actuators A Phys.* 162, 93 (2010). https://doi.org/10.1016/j.sna.2010.06.013.
15. Y. Jang, S. Kang, H.C. Kim, and K. Chun, *J. Micromech. Microeng.* 21, 075016 (2011). https://doi.org/10.1088/0960-1317/21/7/075016.
16. C. Villeneuve, P. Pons, V. Puyal, and R. Plana, *J. Micromech. Microeng.* 20, 064013 (2010). https://doi.org/10.1088/0960-1317/20/6/064013.
17. K. Srinivasa Rao, L.N. Thalluri, K. Guha, and K. Girija Sravani, *IEEE Access* 6, 77519 (2018). https://doi.org/10.1109/ACCESS.2018.2883353.
18. P. Kumar, D. Bansal, A. Kumar, A. Bajpai, K. Mehta, Ashudeep, K. Rangra, and D. Boolchandani, *Microsyst. Technol.* (2020). https://doi.org/10.1007/s00542-020-05000-7.
19. C.L. Goldsmith, Z. Yao, S. Eshelman, and D. Denniston, *IEEE Microw. Guid. Wave Lett.* 8, 269 (1998). https://doi.org/10.1109/75.704410.
20. B. Liu, Z. Lv, Z. Li, X. He, and Y. Hao, A surface micromachining process utilizing dual metal sacrificial layer for fabrication of RF MEMS switch, in *2010 IEEE 5th International Conference Nano/Micro Engineered and Molecular Systems NEMS 2010* (IEEE, 2010), pp. 620–623. https://doi.org/10.1109/NEMS.2010.5592479
21. Y. Liu, Y. Bey, and X. Liu, *IEEE Trans. Microw. Theory Tech.* 64, 3151 (2016). https://doi.org/10.1109/TMTT.2016.2598170.
22. A.J. Dowling, M.K. Ghantasala, J.P. Hayes, E.C. Harvey, and E.D. Doyle, *Smart Mater. Struct.* 11, 715 (2002). https://doi.org/10.1088/0964-1726/11/5/314.
23. J. Yang, Y. Shi, H. Zhong, X. Jiao, R. Zhang, and B. Du, *Microsyst. Technol.* 20, 259 (2014). https://doi.org/10.1007/s00542-013-1946-1.
24. A. Bertacchini, S. Scorcioni, D. Dondi, L. Larcher, P. Pavan, M.T. Todaro, A. Campa, G. Caretto, S. Petroni, A. Passaseo, and M. De Vittorio, AlN-based MEMS devices for vibrational energy harvesting applications, in *Europena Solid-State Device Research Conference* (IEEE, 2011), pp. 119–122. https://doi.org/10.1109/ESSDERC.2011.6044220
25. P. Ekkels, R.W. Tjerkstra, G.J.M. Krijnen, J.W. Berenschot, J. Brugger, and M.C. Elwenspoek, *Microelectron. Eng.* 67–68, 422 (2003). https://doi.org/10.1016/S0167-9317(03)00098-4.
26. S. Evoy, D.W. Carr, L. Sekaric, A. Olkhovets, J.M. Parpia, and H.G. Craighead, *J. Appl. Phys.* 86, 6072 (1999). https://doi.org/10.1063/1.371656.
27. A. Sharma, P. Jhanwar, D. Bansal, A. Kumar, M. Kaur, S. Pandey, P. Kumar, D. Kumar, and K. Rangra, *J. Micro/Nanolithogr.*

*MEMS MOEMS* 13, 013005 (2014). https://doi.org/10.1117/1.jmm.13.1.013005.

28. I.E. Obuh, V. Doychinov, D.P. Steenson, P. Akkaraekthalin, I.D. Robertson, and N. Somjit, *IEEE Trans. Compon. Packag. Manuf. Technol.* 8, 1702 (2018). https://doi.org/10.1109/TCPMT.2018.2834865.
29. M.J. Madou, *Fundamentals of Microfabrication*, 2nd ed., (Boca Raton: CRC Press, 2002). https://doi.org/10.1201/9781482274004.
30. D. Bansal, A. Bajpai, P. Kumar, M. Kaur, and A. Kumar, *IEEE Trans. Electron Devices* 67, 2147–2152 (2020). https://doi.org/10.1109/TED.2020.2982667.

**Publisher's Note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.