Journal of Electronic Materials (2021) 50:4050–4057
https://doi.org/10.1007/s11664-021-08907-7

ORIGINAL RESEARCH ARTICLE

# A Multiple-Trapping-and-Release Transport Based Threshold Voltage Model for Oxide Thin Film Transistors

**Mohil S. Desai[1] · Kavindra Kandpal[2] · Rupam Goswami[3]**

Received: 3 February 2021 / Accepted: 25 March 2021 / Published online: 23 April 2021
© The Minerals, Metals & Materials Society 2021


## Abstract

This article proposes a generic approach for modelling threshold voltage of oxide thin film transistors (TFTs). Threshold voltage has always been ambiguous in TFTs due to the disordered nature of semiconducting thin films, and in operation in accumulation mode. This differs from the situation with metal oxide field-effect transistors (MOSFETs), wherein strong inversion can be specifically defined. The proposed model considers double exponential distribution of deep state and tail state densities in the bandgap with the multiple-trapping-and-release (MTR) transport model. In this surface potential-based approach, pinned surface potential is defined as the surface potential at which free carrier densities exceed deep state carrier density in the deep state-dominated region. The threshold voltage is defined using pinned surface potential and carrier densities obtained at that surface potential. The model is validated using data from fabricated oxide based TFTs with silicon dioxide ($SiO_2$) and other dielectrics. This article develops and reports a systematic approach for fitting an oxide based TFT analytical model with experimental devices, thus ensuring the flexibility needed for compatibility with various devices.


**Keywords** Thin film transistors · multiple-trapping-and-release · pinned surface potential · threshold voltage · deep states · tail states

## Introduction

Applications of thin film transistors (TFTs) in transparent and flexible electronics, including displays, pixel circuits and various types of sensors, have gained a significant boost in recent years. Among various TFTs, oxide TFTs exhibit particularly interesting characteristics such as high mobility, flexibility, wide bandgap and optical transparency.[1] Accordingly, oxide TFTs have emerged as a superior alternative to existing a-Si and poly-Si TFTs for large area electronic applications. TFTs include three basic elements: (1) a semiconducting channel layer; (2) a gate dielectric layer; and (3) three electrodes (gate, source and drain). In an attempt to improve device performance, various architectures have been proposed. Bottom gate gallium indium zinc oxide (GIZO) TFTs have good threshold voltage control.[2] Other configurations such as double gate TFTs find use in high performance pixel circuits. In TFTs, top gate structure provides protection to the channel, whereas coplanar structures offer enhanced performance due to less parasitic capacitance.[3] Another architecture called the source gated TFT has shown improved device characteristics and parameters.[4]

Compact models play an important role in circuit design. Importance of compact models has been highlighted in Ref. 5 with descriptions of TFT models and charge transport properties. In the design and implementation of circuits, it is important to have a detailed understanding of the device behaviour for various conditions and parametric variations. Hence, it is essential to develop a non-iterative, simple and accurate mathematical model to represent the device parameters. Such a model not only describes the physics of the device, but is suitable for use in circuit simulators. Threshold voltage is a critical parameter for any field-effect device, as it determines characteristics such as switching, ratio of on and off currents ($I_{on}/I_{off}$) and subthreshold slope. Unlike metal

✉ Rupam Goswami
rupam21@tezu.ernet.in

[1] Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science Pilani, Rajasthan 333031, India

[2] Department of Electronics and Communication Engineering, Indian Institute of Information Technology Allahabad, Prayagraj, Uttar Pradesh 211015, India

[3] Department of Electronics and Communication Engineering, Tezpur University, Napaam, Assam 784028, India

oxide semiconductor field-effect transistors (MOSFETs), TFTs do not operate by the mechanism of charge inversion at the surface to form a channel, therefore, it becomes difficult to model the threshold voltage. MOSFETs have a single crystalline silicon channel which is devoid of any traps. Also, MOSFETs operate in inversion mode for conduction, hence it is simpler to demarcate a clear threshold point at strong inversion. On other hand, oxide TFTs mainly operate in accumulation mode and have amorphous or polycrystalline channels. Ideally, for gate-to-source voltage beyond flat band voltage, TFTs should show the initiation of accumulation, and the active oxide layer should conduct, but the disordered channel gives rise to trap states, leading to mobility degradation, trapping and a decrease in free carrier density. It is quite challenging to consider the effect of disordered channels on carrier density, and have clear demarcation of the threshold point where there are enough free carriers accumulated in the channel for conduction.

Threshold voltage mainly depends on the material of the conducting film,[6,7] the quality of the interface and the gate dielectric. Variations in threshold voltage in TFTs having the same channel material but different gate dielectrics like Hafnium Oxide ($HfO_2$) and Aluminium Oxide ($Al_2O_3$) has been reported in Ref. 8. The accuracy of threshold voltage models may vary with device configurations and architecture, channel oxide, gate dielectric, process of fabrication, and transport model, as these parameters determine the trap state carriers and free carriers in the device. Many attempts have been made recently to address this issue. Efforts have been made to model the traps and consider their impact while modelling the threshold voltage. Scaled oxide can lower the threshold voltage, which can be modelled using a single grain boundary in a grain boundary transport model.[9] In Ref. 10, line charge approximation of traps was considered due to single line grains (1-Dimension) and threshold voltage was modelled using potential due to this line charge. Single exponential distribution of trap densities with constant deep state density was considered in Ref. 11, and threshold voltage was defined at the interface of the dominant deep state and tail state regions. In Ref. 12 trap states were considered to have a Gaussian distribution. The authors in Ref. 13 defined threshold voltage at degenerate conduction with the help of free charge density and an empirical constant. In Ref. 14, four surface potentials were extracted using different approximations to find their relation with threshold voltage. However, there is a need for a model which takes into account the significant parameters which determine the threshold voltage in TFTs. To address the non-uniformity in existing models for TFTs, this study focuses on reporting a compact and closed form expression of threshold voltage, which can universally take into account the traps and carrier densities without posing a threat to computation time. This work proposes a threshold voltage model based on surface potential and multiple-trapping-and-release (MTR) transport. Using conditions involving a pinned surface potential, which is defined with the help of the free carrier density and deep state carrier density, the threshold voltage is derived, and validated with reported works. This paper is organized as follows: "Significance of Trap States" section discusses the significance of trap state densities and the MTR model. "Methodology to Extract the Threshold Voltage" section describes the methodology for extracting the threshold voltage. In "Validation" section, the model is validated based on experimental papers. "Conclusion" section concludes the paper. Table I defines the list of symbols used in the paper.

## Significance of Trap States

Oxide TFT uses an oxide semiconductor as the conduction layer between source and drain. Considering a bottom gate structure, the gate is placed on a substrate. The oxide channel layer and the gate are separated by a gate dielectric to generate the field-effect, as shown in Fig. 1.

During the growth of metal oxide film in an oxygen deficient environment, it is easier for the metal ions to occupy interstitial vacancies in the metal oxide lattice. The free electrons contributed by metal atoms roam freely in the crystal, giving rise to n-type conductivity. Also, there are $O^{2+}$ vacancies giving rise to more electrons. The deposited channel oxide semiconductor is mostly either amorphous or polycrystalline in nature. In a polycrystalline material, presence of grain boundaries gives rise to a lot of defects, which, in turn, gives rise to trap states within the bandgap. Different charge transport models are prevalent to describe conduction in TFTs. Modelling of trap states, which determine the charge transport in polysilicon films, are depicted by the grain boundary model. Additionally, the hopping transport model accounts for charge transport in amorphous films. Materials like metal oxides form polycrystalline films. These semiconductors display regular arrangement, and delocalized orbitals partially overlap, thereby facilitating more efficient charge transfer and carrier mobility that is much larger than that of amorphous films. The charge transport properties of these materials cannot be explained by the grain-boundary trapping theory and hopping transport.[5] As metal oxides like indium gallium zinc oxide (IGZO) become intrinsically *n*-type, therefore, there are already free electrons in the bulk. When we apply gate voltage $V_g$, they are attracted towards the gate, and the Fermi level rises nearly to $E_C$. As a result, more trap states in the bandgap become available for valence band electrons. As these electrons move easily from $E_V$ to these trap states, they can further easily excite to conduction band from these trap states. The reduction in difference between $E_f$ and $E_C$ aids this phenomenon. These carriers get re-trapped in the trap states from $E_C$

**Table I** List of symbols

| Sl. no. | Symbols | Definition | Sl. no. | Symbols | Definition |
|---|---|---|---|---|---|
| 1. | $E_{f0}$ | Flat band Fermi level | 15. | $Q_t$ | Charge density in tail states |
| 2. | $E_f$ | Current Fermi level | 16. | $Q_d$ | Charge density in deep states |
| 3. | $E_c$ | Conduction band edge | 17. | $Q_f$ | Accumulated free charge density |
| 4. | $E_v$ | Valence band edge | 18. | $n_t$ | Carrier density in tail states |
| 5. | $T_d$ | Characteristic temperature of deep states | 19. | $n_d$ | Carrier density in deep states |
| 6. | $T_t$ | Characteristic temperature of tail states | 20. | $n_f$ | Free carrier density |
| Note: Characteristic temperature determines ionization energy of the trap. It is higher for deep states than for tail states | | | 21. | $n_{tot}$ | Total carrier density (free + deep + tail) |
| 7. | $N_d$ | Deep state density per energy change at conduction band (energetic distribution) | 22. | $t_s$ | Channel thickness |
| 8. | $N_t$ | Tail state density per energy change at conduction band (energetic distribution) | 23. | $\Psi_{sp}$ | Surface potential at threshold point (pinned) |
| 9. | $V_{fb}$ | Flat band voltage | 24. | $V_{th}$ | Threshold Voltage |
| 10. | $C_{deep}$ | Capacitance due to deep states charges | 25. | $Q_{dm}$ | Maximum depletion charge of MOSFET |
| 11. | $C_{tail}$ | Capacitance due to tail states charges | 26. | $\Psi_s$ | Surface potential |
| 12. | $C_{free}$ | Capacitance due to accumulated free charges | 27. | $C_{dm}$ | Maximum depletion capacitance in MOSFET |
| 13. | $C_{ox}$ | Oxide Capacitance | 28. | $V_{ox}$ | Potential drop across the oxide |
| 14. | k | Boltzmann constant | | | |

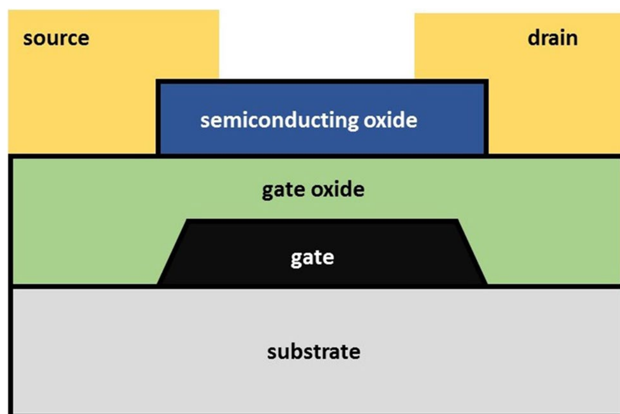


**Fig. 1** A generalized architecture of a TFT (not to scale).

and are thermally excited back to $E_C$ as shown in Fig. 2. At threshold voltage, abundant free carriers are accumulated (at the same time getting trapped and released) and we get trap limited conduction (TLC).[11] Hence, the MTR model is suitable for modelling $V_{\text{th}}$ for oxide TFTs having trap states. If $V_g$ is reduced, the Fermi level moves down. Therefore, the carriers which are trapped find it difficult to rise up to $E_C$; instead, they (the carriers initially trapped due to higher Fermi level) fall to back to $E_v$ as Fermi level goes down.

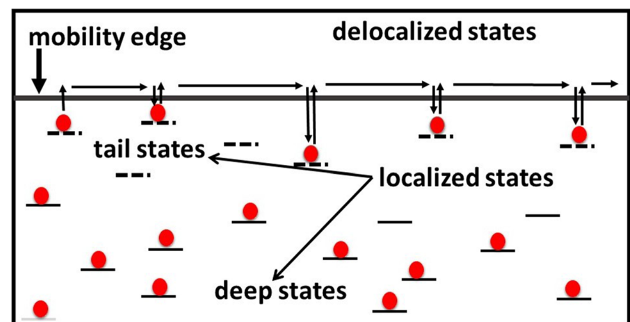


**Fig. 2** Representation of the MTR charge transport model.

Considering the MTR, we assume that charge transport takes place in the delocalized states, which resembles conduction and valence bands for electrons and holes, respectively. The mobility edge separates localized and delocalized states (Fig. 2). There are two types of trap state densities in the region of localized states, namely deep states and tail states. These trap states account for both inter-grain and intra-grain defects in the film. Deep states are dominant near the centre of the bandgap, while tail states become dominant as we move towards the conduction or valence band (Fig. 3). The deep states are mainly due to oxygen vacancies and the tail

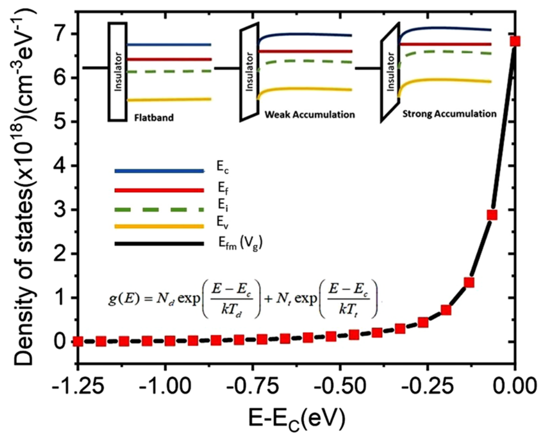


**Fig. 3** Double exponential distribution of trap states (deep and tail).

states arise from metal. Conduction occurs due to free charge carriers in delocalized states above the mobility edge. We have considered a double exponential distribution model for distribution of density of states (DOS).[15] These trap states play a critical role in predicting the device parameters and behaviour.

## Methodology to Extract the Threshold Voltage

This section discusses the steps in arriving at the equation of threshold voltage through different subsections.

### DOS and Charge Density

The double exponential distribution of deep and tail states is given by:

$$g(E) = N_d \exp\left(\frac{E - E_c}{kT_d}\right) + N_t \exp\left(\frac{E - E_c}{kT_t}\right). \quad (1)$$

The exponential functions at low and high energy values represent the dominant distribution of deep and tail states in the energy gap, respectively. At flat band, the Fermi level is at $E_{f0}$. As the gate voltage increases, the Fermi level begins to rise and bands start bending near the oxide-semiconductor interface. Consider the band bending due to surface potential within the channel thickness, $t_s$.[16] As the band bending starts, free charges begin to accumulate at a slow rate initially as per the MTR model. As the Fermi level rises, these trapped states become occupied by the carriers up until the Fermi level, at which point it becomes more feasible to excite them thermally. Initially, the Fermi level resides in the deep state dominated region near the middle of the band gap. The distribution of deep state carrier density is given by $n_d = \int_{Ef0}^{Ef} N_{\text{deep}}(E)f(E)\text{d}E$, where $f(E) = \frac{1}{1+\exp\left(\frac{E-E_f}{kT}\right)}$ is the probability function, and $N_{\text{deep}}(E) = N_d \exp\left(\frac{E-E_C}{kT_d}\right)$. When we substitute $E = E_f$, we get

$$n_d = N_d kT_d \left( \ln \left( \frac{2}{\exp\left(\left(E_{f0} - E_f\right)/kT_d\right) + 1} \right) \right) \exp - \left( \frac{E_c - E_f}{kT_d} \right). \quad (2)$$

This can be approximated as $n_d = N_d kT_d \ln(2) \exp - \left(\frac{E_c - E_f}{kT_d}\right)$. Trapped state charge density in deep states is given by:

$$Q_d = qn_d t_s. \quad (3)$$

If the Fermi level rises further, there is an increase in tail state trap densities and they start becoming dominant. Tail state carrier density is defined as $n_t = \int_{Ef0}^{Ef} N_{\text{tail}}(E)f(E)\text{d}E$, where $N_{\text{tail}}(E) = N_t \exp\left(\frac{E-E_c}{kT_t}\right)$. When we substitute $E = E_f$, we get

$$n_t = N_t kT_t \ln(2) \exp - \left( \frac{E_c - E_f}{kT_t} \right), \quad (4)$$

where $E_f = E_{f0} + q\Psi_s$ is the energy level corresponding to the gate voltage. Trapped state charge density in tail states is given by:

$$Q_t = qn_t t_s, \quad (5)$$

and similarly, free charge density can be defined as:

$$Q_f = qn_f t_s, \quad (6)$$

where

$$n_f = N_c \exp - \left( \frac{E_c - E_{f0} - q\Psi_S}{kT} \right). \quad (7)$$

### Threshold Voltage

Since TFTs work in the accumulation mode of conduction, it becomes inconvenient to define their threshold voltage equation in terms of the inversion-based model in MOSFETs. Although the concept of $V_{fb}$ fits well for both accumulation and inversion mode devices, the major difference lies in defining the surface potential and charge density terms in the $V_{\text{th}}$ equation. In MOSFET, surface potential condition at the threshold point is defined as $\Psi_s = 2\emptyset_f$, where $\emptyset_f$ is the bulk Fermi potential, which suggests that the inverted charge density at this surface potential equals the bulk charge density and is sufficient to shield the bulk charge density; so it is large enough for conduction. Further increase in gate voltage

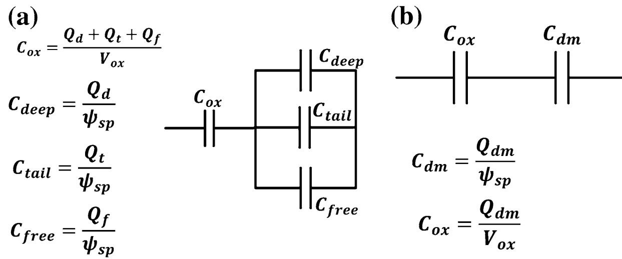


**Fig. 4** Capacitance model at threshold voltage point for (a) TFT and (b) MOSFET.

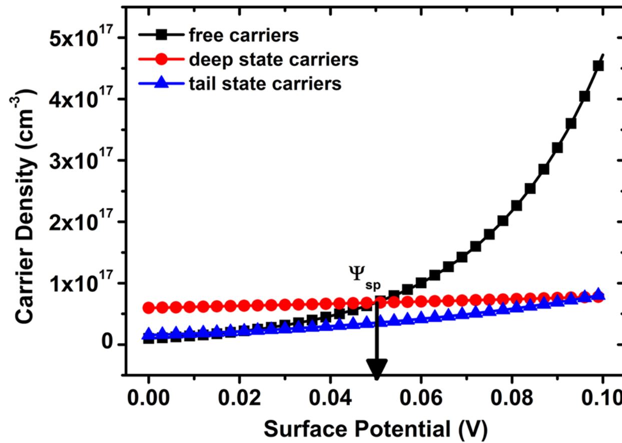


**Fig. 5** Carrier density versus surface potential for the fabricated TFT (data from Ref. 17).

($V_g$) increases inverted charge density without a further rise in surface potential.

In TFTs, threshold voltage can be defined as the gate voltage at which sufficient free carriers are available to conduct drain current. As the gate voltage is increased, the capacitance of the field-effect transistor varies based on charge variation in the bulk and in the channel (Fig. 4a for TFT; similar MOSFET analogy in Fig. 4b). For MOSFET, this depends on bulk charges, while for oxide TFTs it is determined by deep state, tail state and free carrier densities. The gate voltage at which free carrier density exceeds deep-state carrier density is defined as the threshold voltage. This transition point highly depends on properties of the film (largely on trap states), which in-turn depends on fabrication conditions and process. At gate voltages beyond the threshold voltage, there is a large rise in accumulation of free carriers as the gap between $E_f$ and $E_c$ reduces and trapped carriers are easily excited to $E_c$ , further shielding the trap states. The surface potential at which threshold voltage is attained is defined as the pinned surface potential,$\Psi_{sp}$, as shown in Fig. 5. Since at this surface potential, the Fermi level is in the deep state-dominated region, tail state carrier density is less significant, although their effects are considered in the model. Process variation has significant impact on trap densities and, in turn, on pinned surface potential. So, there is no fixed condition for pinned surface potential in TFT as there is in MOSFET. While modelling $V_{th}$, these variations in pinned surface potential due to fabrication conditions and processes have been accounted for by considering a parameter for modelling the traps ($N_d, T_d, N_t, T_t$). This serves as a fitting parameter to bring the modelled properties in line with the fabricated device as shown in "Validation" section. The threshold voltage in Eq. 9 has been defined using surface potential as defined in Eq. 8 from Ref. 17, and corresponding carrier densities.

Figure 5 shows variation in carrier densities with surface potential, plotted for device parameters given in Ref. 17 (Sr no. 2 in Table II). It can be seen that at pinned surface potential ($\Psi_{sp} = 0.05$V), the plot for free carrier density crosses the plot for deep state carrier density, which gives the threshold voltage point.

$$\Psi_s = \int_{V_{g2}}^{V_{g1}} \left(1 - \frac{C}{C_{\mathrm{ox}}}\right) \mathrm{d}V_g \tag{8}$$

$$\Psi_{\mathrm{sp}} = \int_{V_{fb}}^{V_{th}} \mathrm{d}V_g - \int_{V_{fb}}^{V_{th}} \left(\frac{C}{C_{\mathrm{ox}}}\right) \mathrm{d}V_g$$

$$\Psi_{\mathrm{sp}} = V_{\mathrm{th}} - V_{\mathrm{fb}} - \frac{1}{C_{\mathrm{ox}}} \int_0^{\Psi_{\mathrm{sp}}} \left(\frac{\mathrm{d}Q}{\mathrm{d}\Psi_s}\right) \mathrm{d}\Psi_s$$

$$\Psi_{\mathrm{sp}} = V_{\mathrm{th}} - V_{\mathrm{fb}} - \frac{qt_s}{C_{\mathrm{ox}}} \int_0^{\Psi_{\mathrm{sp}}} \left(\frac{d(n_{\mathrm{deep}}(\Psi_s) + n_{\mathrm{tail}}(\Psi_s) + n_{\mathrm{free}}(\Psi_s))}{\mathrm{d}\Psi_s}\right) \mathrm{d}\Psi_s,$$

$$V_{th} = V_{fb} + \Psi_{sp} + \frac{Q_s}{C_{ox}}, \tag{9}$$

where $Q_s = qn_{tot}t_s$ and $n_{\mathrm{tot}}$ is obtained as

$$n_{\mathrm{tot}} = \left[N_d k T_d e^{\left(\frac{E_{f0}-E_c}{kT_d}\right)} \left(e^{\left(\frac{q\Psi_{sp}}{kT_d}\right)} - 1\right) + N_t k T_t e^{\left(\frac{E_{f0}-E_c}{kT_t}\right)} \left(e^{\left(\frac{q\Psi_{sp}}{kT_t}\right)} - 1\right)\right] \ln 2 + N_c e^{\left(\frac{E_{f0}-E_c}{kT}\right)} \left(e^{\left(\frac{q\Psi_{sp}}{kT}\right)} - 1\right) \tag{10}$$

Using this pinned surface potential, we can find the relation between deep state charge density and tail state charge density at the threshold voltage. From Eqs. 3 and 5 we can get the values of deep and tail state charge density. Also, charge density of accumulated free carriers can be obtained at threshold using Eq. 6.

## Validation

The proposed threshold voltage model has been verified and validated using data from experimental papers as shown in Table II. In some cases[1,22–25] where information about trap densities ($N_d, T_d, N_t, T_t$) has not been given in the paper, typical values have been assumed as used in the experimental papers. In experimental papers[17–21] these parameters were extracted from software and used as fitting parameters to validate the simulated model with a fabricated device. Mismatch between reported $V_{th}$ and modelled $V_{th}$ in this work is mainly due to small variations in $n_{tot}$ calculated from the

**Table II** Validation of threshold voltage for fabricated devices, data taken from reported works (cited in the final column)

| Sr no. | Flatband Voltage (V) | $\Psi_{sp}$ (V) | $n_{tot}(\times10^{17})$ (cm$^{-3}$) (from (10)) | $n_{tot}(\times 10^{17})$ (cm$^{-3}$) (from curve-fitting) | $V_{th}$(V) | Data from reported works |
|---|---|---|---|---|---|---|
| 1 | 0.17 | 0.065 | 0.856 | 0.577 | 2.91 | 17 |
| 2 | 1.83 | 0.05 | 0.869 | 0.758 | 5.39 | 17 |
| 3 | 2.73 | 0.038 | 0.891 | 0.527 | 5.21 | 17 |
| 4 | – 1.4 | 0.038 | 0.149 | 0.526 | 0.1 | 18 |
| 5 | 0.21 | 0.088 | 0.472 | 0.104 | 0.49 | 19 |
| 6 | 0.13 | 0.186 | 0.682 | 0.857 | 2.3 | 20 |
| 7 | 0.36 | 0.104 | 0.979 | 0.623 | 3.35 | 17 |
| 8 | 0.2 | 0.082 | 1.037 | 0.777 | 3.89 | 17 |
| 9 | 1.22 | 0.069 | 1.114 | 0.887 | 5.4 | 17 |
| 10 | 0.11 | 0.064 | 1.074 | 1.277 | 1.95 | 21 |
| 11 | 0.21 | 0.07 | 3.16 | 3.81 | 1.85 | 22 |
| 12 | 0.21 | 0.07 | 3.16 | 5.82 | 2.4 | 22 |
| 13 | 0.21 | 0.07 | 3.16 | 6.695 | 2.66 | 22 |
| 14 | – 0.45 | 0.07 | 3.16 | 6.302 | 4 | 23 |
| 15 | – 0.25 | 0.07 | 3.16 | 1.508 | 2 | 24 |
| 16 | – 0.65 | 0.07 | 3.16 | 3.451 | 3.2 | 1 |
| 17 | – 0.45 | 0.07 | 3.16 | 2.747 | 3.6 | 25 |

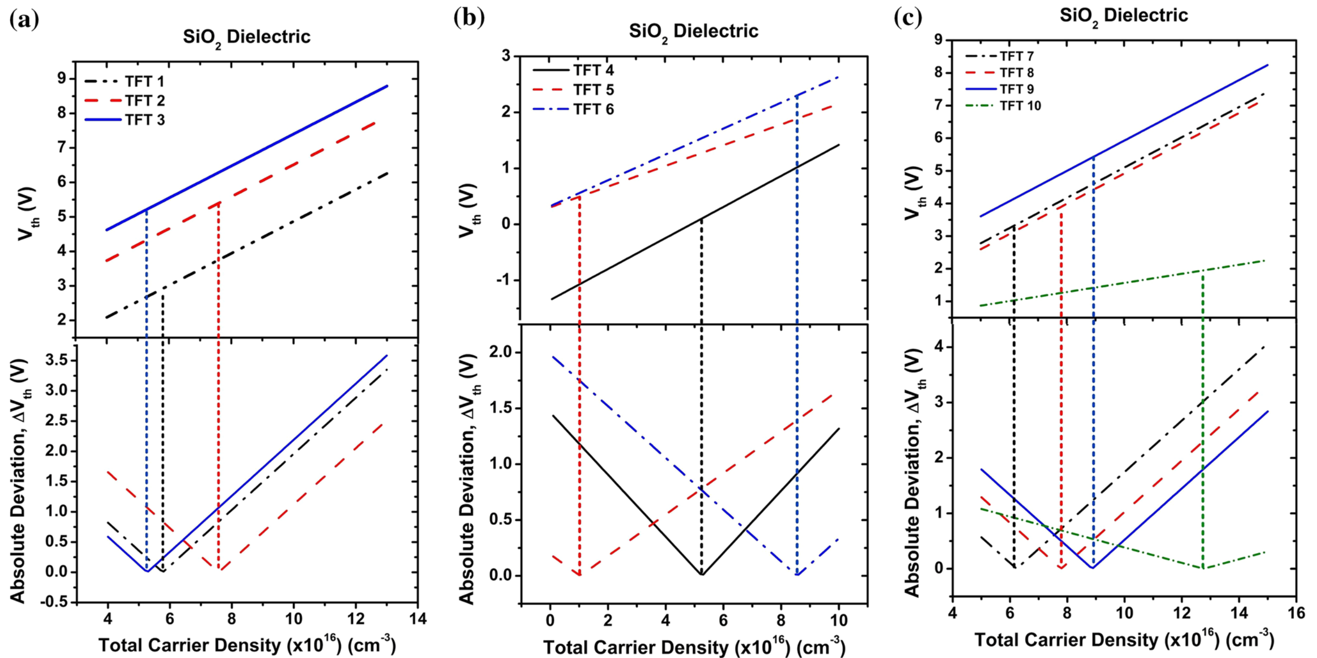


**Fig. 6** Threshold voltage and absolute deviation versus total carrier density for devices with $SiO_2$ dielectric: (a) TFT1, TFT2, TFT3; (b) TFT4, TFT5, TFT6; (c) TFT7, TFT8, TFT9, TFT10, where TFTn represents TFT corresponding to serial number '*n*' in Table II.

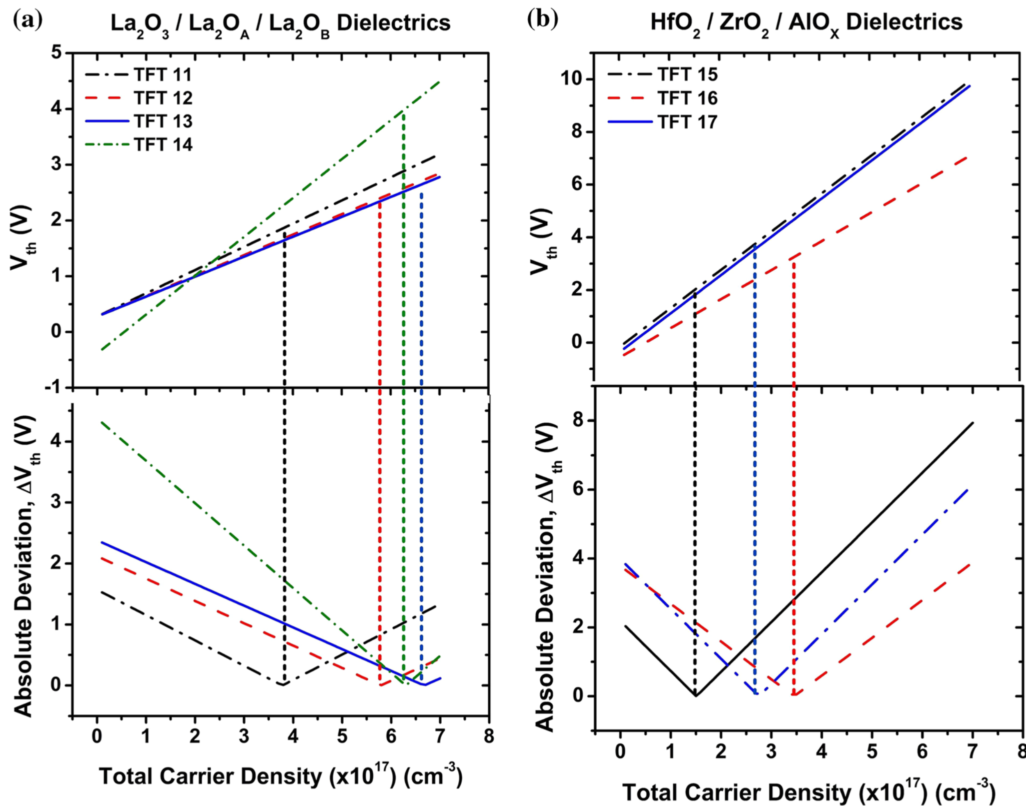


**Fig. 7** Threshold voltage and absolute deviation versus total carrier density for devices with (a) $La_2O_3$/ $La_2O_A$/ $La_2O_B$ dielectrics and (b) $HfO_2$/ $ZrO_2$/ $AlO_x$ dielectrics, where TFTn represents TFT corresponding to serial number '*n*' in Table II.

model, which are small with respect to the order of carrier density.

This mismatch in $n_{tot}$ is accounted for by allowed variations in $N_d, T_d, N_t$ and $T_t$. Since these are physical entities and can be used as fitting parameters, we can tune them to vary $n_{tot}$ , and consequently the modelled $V_{th}$. Graphs in Figs. 6 and 7 show variation of $V_{th}$ and absolute deviation of $V_{th}$ from reported values with $n_{tot}$. It can be seen that at the minima of absolute deviation, we get the $n_{tot}$ (which is a function of $N_d, T_d, N_t, T_t$ and $\Psi_{sp}$) required to get reported $V_{th}$ value of the fabricated device. Modelled $V_{th}$ lies within a permissible range of $n_{tot}$ variation i.e., $\pm 4 \times 10^{16}$ cm$^{-3}$ for devices with $SiO_2$ dielectric and $\pm 4 \times 10^{17}$ cm$^{-3}$ for devices with other dielectrics as per the tuning of $N_d, T_d, N_t$ and $T_t$. Interestingly, the proposed model is able to universally validate the results from fabricated devices through the typical range of $n_{tot}$ used.

## Conclusion

In this paper, we have developed a simple yet robust mathematical model for computing the threshold voltage of oxide TFT. We have demonstrated the impact of charge density in determining the threshold voltage. With the help of surface potential, values of free and trapped carrier densities at threshold voltage can be deduced. As free carrier density exceeds deep state carrier density, corresponding pinned surface potential defines the threshold voltage point. The model defines the threshold voltage in oxide TFTs with reference to the MTR transport model. The dependence of threshold voltage on the fundamental parameters and material properties makes the model compact. The proposed threshold voltage model holds valid for all oxide TFTs with $SiO_2$ as well as other dielectrics. Hence, this generic model can be tuned with trap density parameters as per requirements, which is verified with several fabricated devices.

**Conflict of interest** The authors declare that they have no conflict of interest.

## References

1. J. Lee, S. Chang, S. Koo, and S. Lee, *IEEE Electron Device Lett.* 31, 225 (2010).
2. J. Kwon, K. Son, J. Jung, T. Kim, M. Ryu, K. Park, B. Yoo, J. Kim, Y. Lee, K. Park, S. Lee, and J. Kim, *IEEE Electron Device Lett.* 29, 1309 (2008).

3. L. Zhang L, W. Xiao, W. Wu, B. Liu (2019) Appl. Sci. (Switzerland) 9:1
4. A. Ma, M. Benlamri, A. Afshar, G. Shoute, K. Cadein and D. Barlage, CS Mantech 385 (2014).
5. N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li, and M. Liu, *Micromachines* 9, 1 (2018).
6. C. Chang, and Y. Wu, *J. Electron. Mater.* 37, 1653 (2008).
7. C. Tsay, M. Wang, and S. Chiang, *J. Electron. Mater.* 38, 1962 (2009).
8. P. Carcia, R. McLean, and M. Reilly, *Appl. Phys. Lett.* 88, 30 (2006).
9. N. Gupta, *Phys. Scr.* 76, 628 (2007).
10. K. Kandpal, N. Gupta, J. Singh, and C. Shekhar, *J. Electron. Mater.* 49, 3156 (2020).
11. S. Lee, and A. Nathan, *Sci. Rep.* 6, 1 (2016).
12. F. Hossain, J. Nishii, S. Takagi, A. Ohtomo, T. Fukumura, H. Fujioka, H. Ohno, H. Koinuma, and M. Kawasaki, *J. Appl. Phys.* 94, 7768 (2003).
13. L. Qiang, and R. Yao, *IEEE Trans. Electron Devices* 61, 2394 (2014).
14. C. Chen, W. Chen, L. Zhou, W. Wu, M. Xu, L. Wang, and J. Peng, *AIP Adv.* 6, 035025 (2016).
15. F. Torricelli, J. Meijboom, E. Smits, A. Tripathi, M. Ferroni, S. Federici, G. Gelinck, L. Colalongo, Z. Kovacs-Vajna, D. De Leeuw, and E. Cantatore, *IEEE Trans. Electron Devices* 58, 2610 (2011).
16. S. Lee, S. Jeon, and A. Nathan, *IEEE/OSA J. Disp. Technol.* 9, 883 (2013).
17. P. Migliorato, M. Chowdhury, J. Um, M. Seok, M. Martivenga, and J. Jang, *IEEE/OSA J. Disp. Technol.* 11, 497 (2015).
18. H. Choi, J. Lee, H. Bae, S. Choi, D.H. Kim, and D.M. Kim, *IEEE Trans. Electron Devices* 62, 2689 (2015).
19. H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C. Wu, *Appl. Phys. Lett.* 92, 10 (2008).
20. Y. Jeon, S. Kim, S. Lee, D.M. Kim, D.H. Kim, J. Park, C. Kim, I. Song, Y. Park, U. Chung, J. Lee, B. Ahn, S. Park, J. Park, and J. Kim, *IEEE Trans. Electron Devices* 57, 2988 (2010).
21. W. Chen, G. Qin, L. Zhou, W. Wu, J. Zou, M. Xu, L. Wang, and J. Peng, *AIP Adv.* 8, 065319 (2018).
22. L. Qian, P. Lai, and W. Tang, *Appl. Phys. Lett.* 104, 1 (2014).
23. P. Gogoi, R. Saikia, D. Saikia, R. Dutta, and S. Changmai, *Physica Status Solidi (A) ApplMater. Sci.* 212, 826 (2015).
24. L. Ji, C. Wu, T. Fang, Y. Hsiao, T. Meen, W. Water, Z. Chiu, and K. Lam, *IEEE Sens. J.* 13, 4940 (2013).
25. M. Furuta, T. Kawaharamura, D. Wang, T. Toda, and T. Hirao, *IEEE Electron Device Lett.* 33, 851 (2012).

**Publisher's Note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.