Journal of ELECTRONIC MATERIALS, Vol. 50, No. 4, 2021
https://doi.org/10.1007/s11664-020-08673-y
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ORIGINAL RESEARCH ARTICLE

Atomic Layer Deposition of ZnO for Modulation of Electrical Properties in *n*-GaN Schottky Contacts

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ZnO films (5 nm and 20 nm) have been grown on GaN single-crystal substrates by thermal atomic layer deposition (ALD) and the electrical properties of *n*-GaN Schottky contacts modified by such ultrathin ZnO films have been characterized. Compared with 5-nm-thick ZnO, 20-nm-thick ZnO exhibited a better rectifying nature. The average barrier height and ideality factor at room temperature were extracted to be 0.64 eV and 2.33 eV, and 1.01 eV and 1.16 eV, for 5-nm- and 20-nm-thick ZnO, respectively. These results indicate that both the barrier height and ideality factor were altered effectively by changing the ZnO thickness. The temperature-dependent reverse current–voltage (*I*–*V*) characteristics revealed that tunneling was dominant for the 5-nm-thick ZnO. A laterally inhomogeneous barrier was appropriate to explain the forward *I*–*V* characteristics for both samples. Based on the parallel conductance method and forward *I*–*V* data, a lower interface state density was observed for 20-nm-thick ZnO, implying improved interface quality. These results suggest that the electrical properties of *n*-GaN Schottky contacts could be easily modulated by changing the ZnO thickness.

Key words: GaN, barrier height, interface state density, ZnO thickness

INTRODUCTION

As wide-bandgap semiconductors, both gallium nitride (GaN) and zinc oxide (ZnO) have attracted significant interest for use in optoelectronic devices.[1,2] GaN-based materials are widely used in high-electron-mobility transistors and high-power devices.[3,4] Meanwhile, ZnO offers various advantages over GaN, such as a larger exciton binding energy (∼ 60 meV) and simpler crystal growth technology.[2] However, most of all, the small lattice mismatch between GaN and ZnO (∼ 1.8%) enables the fabrication of high-performance ZnO/GaN heterojunction devices.[5] It has been shown that the high density of dislocations in the GaN/sapphire interface region can be reduced by process optimization, resulting in high-quality ZnO films.[6] Furthermore, *n*-ZnO/*p*-GaN heterojunction light-emitting diodes (LEDs) show higher recombination and improved efficiency compared with GaN homojunction LEDs due to the improved current confinement.[7]

In addition, much research has been carried out on *n*-ZnO/*n*-GaN isotype heterojunctions, because high-quality *n*-type GaN with high electron mobility can be obtained more easily than *p*-GaN. Using diodes with an *n*-ZnO/i-NiO/*n*-GaN isotype heterostructure prepared by organometallic vapor-phase epitaxy (OMVPE), Wang et al. observed strong ultraviolet (UV) emission at 363 nm and weak deep-level emission at around 530 nm.[8] Strong UV emission at ∼ 367 nm has been observed in magnetron-sputtered *n*-ZnO on *n*-GaN heterojunction diodes.[9,10] A low reverse leakage current of

(Received August 6, 2020; accepted December 4, 2020; published online January 21, 2021)

less than 10^{-7} A cm^{-2} at −1 V but a high ideality factor of 3.37 were observed in sol–gel-synthesized n-ZnO on n-GaN heterojunction diodes.[11] The electrical properties of n-ZnO/n-GaN heterostructures obtained by radiofrequency-sputtered ZnO on GaN layers were characterized by temperature-dependent current–voltage and electron beam-induced current measurements.[12] However, the cited works employed thick (> 100 nm) ZnO films, which are unsuitable for use in nanopatterned devices.

On the contrary, atomic layer deposition (ALD) is very promising growth technique for the fabrication of nanostructured devices because of its high conformality for complex nanostructures.[13,14] ALD-grown ZnO has been applied in nonvolatile crossbar memories and organic electronics that require low-temperature processing.[15] It is thus meaningful to study ALD growth of ZnO on n-GaN because the results could be used to fabricate nanostructured ZnO/GaN heterojunction devices. The interface between ZnO and GaN has been found to be atomically sharp with good coherency.[16] ALD-grown ZnO films were found to be epitaxial, and their quality improved with increasing growth temperature near the threshold temperature for two-dimensional growth.[17] ALD-grown ZnO on high extensive lattice mismatch substrates (GaAs and InP) was found to be polycrystalline, whereas ALD growth of ZnO on GaN and 4H-SiC substrates led to epitaxial ordering in the temperature range from 180°C to 250°C.[18] Wachnicki et al.[19] and Krajewski et al.[20] grew ZnO films by ALD and investigated their properties. The cited works focused on material characterization of ZnO films grown on epitaxial GaN/sapphire substrates, not directly on GaN substrate. To the best of the authors' knowledge, however, there is limited knowledge regarding ALD growth of ZnO films on GaN substrate[21] or characterization of devices using this ZnO/GaN heterojunction system. In this work, we thus grew thin ZnO films at 100°C on n-GaN substrate by thermal ALD and investigated the electrical properties of n-GaN Schottky contacts modified by such ultrathin ZnO films.

EXPERIMENTAL PROCEDURES

ALD growth of ZnO films was carried out using c-plane (0001) GaN single-crystal substrate (thickness ~ 320 μm, carrier concentration ~ 2×10^{17} cm^{-3}) as starting material. Small pieces of GaN samples were loaded into a thermal ALD chamber immediately after cleaning in HCl:H_2O (1:1) solution. The temperature was increased up to 100°C to grow ZnO films using diethylzinc [DEZn, $Zn(C_2H_5)_2$] and H_2O as Zn precursor and oxidant, respectively. The ALD pulse sequence for ZnO growth comprised DEZn feeding (0.2 s), N_2 purge (15 s), H_2O feeding (0.1 s), and N_2 purge (15 s) with a growth rate per cycle (GPC) of ~ 1.2 Å/cycle, lower than the values of 1.5 Å/cycle to 1.8 Å/cycle reported at a growth temperature of 100°C.[22–24] Compared with the cited works, the H_2O purge time in this work was slightly longer. Meanwhile, Park et al. reported a decrease in the GPC value with increasing H_2O purge time when growing ZnO films at 170°C.[25] Lu et al. observed lower GPC values for higher Ar flow rates during the purge.[26] Based on these results, we suspect that partial loss of surface hydroxyl groups would occur more significantly during long H_2O purges, resulting in the lower GPC value. The thickness of the ZnO films was determined by using an FS-1 multiwavelength ellipsometer. In this work, we prepared two different ZnO layers with thickness of 5 nm and 20 nm. Top and bottom metal contacts were sputtered onto the ZnO/n-GaN heterojunction. The 100-nm-thick Pt top contacts (diameter 300 μm) were deposited through a shadow mask onto the ZnO surface, while the 100-nm-thick Al back contacts were formed over the entire GaN back surface. Electrical characterization was carried out using current–voltage (I–V) and capacitance–voltage (C–V) measurements with a Keithley 238 current source and HP 4284A LCR meter, respectively.

RESULTS AND DISCUSSION

Figure 1a and b shows atomic force microscopy (AFM) images of the ZnO surface. For the 5-nm-thick ZnO, the surface was fairly smooth. However, the surface of the 20-nm-thick ZnO was thicker. The root-mean-square (rms) values were found to be about 0.67 nm and 3.89 nm for 5-nm- and 20-nm-thick ZnO, respectively. The high-resolution scanning electron microscopy (HRSEM) images in Fig. 1c and d also show a surface morphology similar to that observed in the AFM images. The surface structure of the 20-nm-thick ZnO was composed of grains of various sizes (roughly 10 nm to 30 nm). It has been reported that the surface of ZnO becomes rougher with increasing number of ALD cycles (i.e., increasing ZnO thickness),[27] similar to the current work.

Figure 2a and b shows the room-temperature I–V curves obtained from several diodes for each sample. The current values for 5-nm-thick ZnO were much higher than those for 20-nm-thick ZnO, and the reverse leakage current for 5-nm-thick ZnO increased more rapidly. Assuming that thermionic emission (TE) is the major forward current conduction mechanism, the diode current can be described as[28]

$$I = I_0[\exp(q(V - IR_S)/nkT) - 1], \tag{1}$$

$$I_0 = AA^{**}T^2 \exp(-q\varphi_B/kT), \tag{2}$$

where I_0 is the reverse-bias saturation current, n is the ideality factor, R_S is the series resistance, A is the contact area, A^{**} is the effective Richardson constant (26.4 A/cm^2-K^2 for n-GaN), and $q\phi_B$ is the

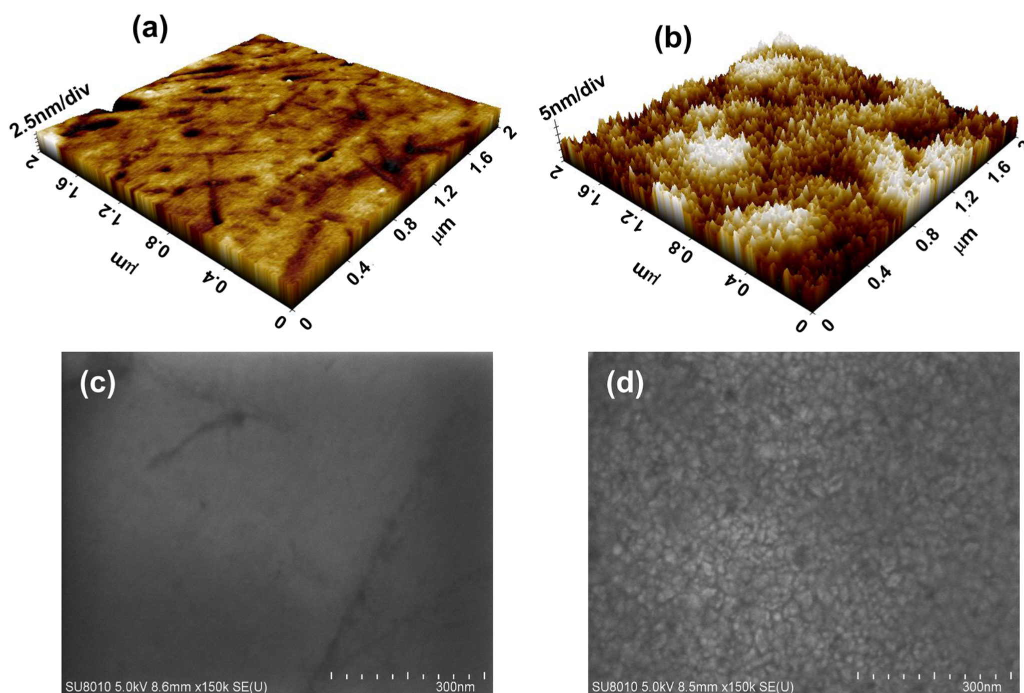

Fig. 1. AFM images of (a) 5-nm- and (b) 20-nm-thick ZnO scanned over 2 μm $\times$ 2 μm area, and scanning electron microscopy images of (c) 5-nm- and (d) 20-nm-thick ZnO.

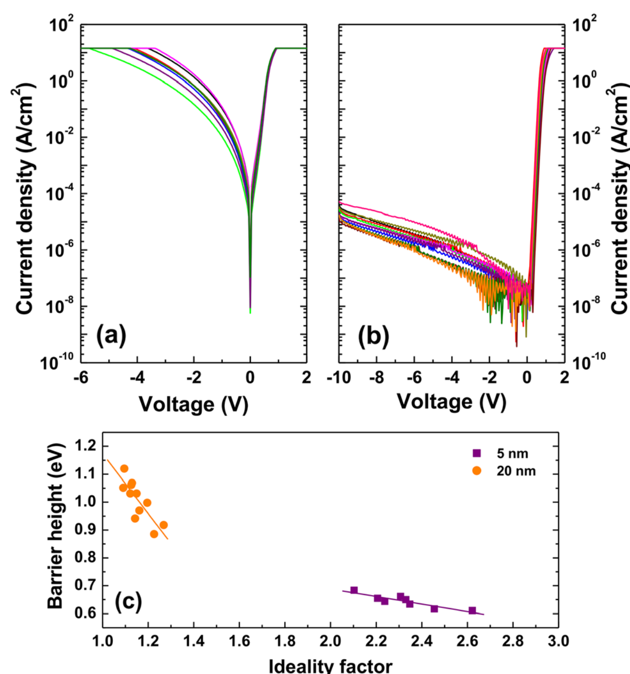

Fig. 2. Semilogarithmic current density–voltage (J–V) curves for (a) 5-nm- and (b) 20-nm-thick ZnO measured at room temperature and (c) barrier height versus ideality factor.

effective barrier height,. The forward I–V analysis for 5-nm-thick ZnO revealed values of $q\phi_{\rm B}^{(I-V)}$ = 0.64 $\pm$ 0.02 eV and n = 2.33 $\pm$ 0.16. Likewise, the analysis for 20-nm-thick ZnO yielded values of $q\phi_{\rm B}^{(I-V)}$ = 1.01 $\pm$ 0.07 eV and n = 1.16 $\pm$ 0.05. The ideality factor above unity for 5-nm-thick ZnO may indicate

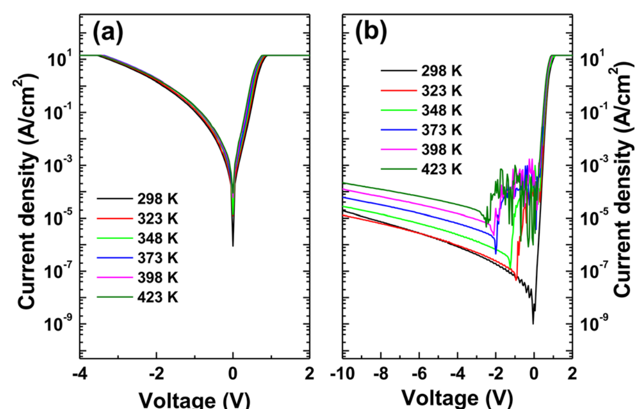

Fig. 3. Semilogarithmic current density–voltage (J–V) curves for (a) 5-nm- and (b) 20-nm-thick ZnO measured at different temperatures.

the presence of interface/surface states and structural nonuniformity. As shown in Fig. 2c, both samples showed a linear correlation between barrier height and ideality factor, implying lateral barrier inhomogeneity. Considering the image-force-lowered barrier height,[29] the homogeneous barrier heights ($q\phi_{\rm B}^{\rm hom}$) were found to be 0.82 eV and 1.16 eV for 5-nm- and 20-nm-thick ZnO, respectively.

To further investigate the electrical properties, the I–V characteristics were measured at different temperatures (Fig. 3). For 5-nm-thick ZnO, only very slight variation of the reverse leakage current was observed, indicating that the tunneling current was dominant. In contrast, the reverse leakage current increased with temperature for 20-nm-thick

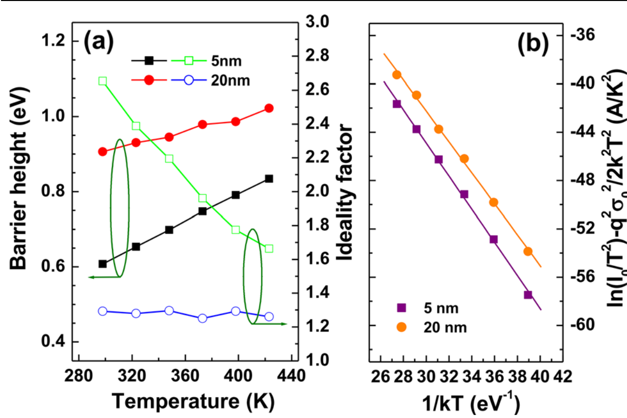

Fig. 4. (a) Temperature dependence of barrier height and ideality factor and (b) modified Richardson plots.

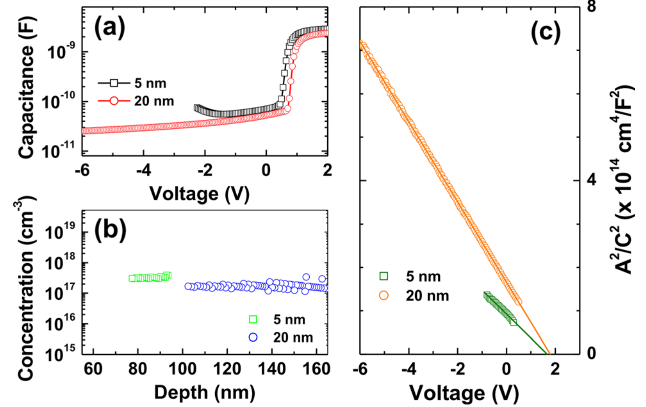

Fig. 5. (a) Capacitance–voltage (C–V) curves measured at 1 MHz and (b) carrier concentration versus depth. (c) A^2/C^2 versus V obtained from the values at 100 kHz.

ZnO, implying the involvement of thermally activated process. From the plots of reverse current versus $1/kT$, the activation energy for 20-nm-thick ZnO was found to be 0.35 eV to 0.44 eV. Figure 3b also shows the complicated I–V behavior under low reverse-bias conditions (i.e., the current increased with decreasing reverse bias). This result indicates the presence of a leakage current conduction path. The origin of this current path is still unclear, but it would be related to current conduction via grain boundaries in the ZnO layer.[30,31]

Figure 4a shows the ideality factor and barrier height at different temperatures. For both samples, the barrier height was found to increase with temperature. The lateral variation in the barrier height has been used to explain such temperature dependence.[32] In the inhomogeneous barrier model,[32] the temperature-dependent effective barrier height ($q\varphi_B$) is expressed as $q\varphi_B = q\bar{\varphi}_B - q^2\sigma_0^2/2kT$, where q $\bar{\varphi}_B$, and σ_0 are the zero-bias mean barrier height and standard deviation, respectively. Based on linear fits to the $q\varphi_B$ versus $1/2kT$ plots, we obtained values of $q\bar{\varphi}_B$ = 1.36 eV (1.28 eV) and σ_0 = 0.198 V (0.139 V) for 5-nm-thick (20-nm-thick) ZnO. Figure 3b shows the modified Richardson plots of $\ln(I_0/T^2) - q^2\sigma_0^2/2k^2T^2$ versus $1/kT$. The intercepts of the linear fits to these plots with the ordinate were used to calculate Richardson constant A^{**} values of 32.3 A cm^{-2} K^{-2} and 30.2 A cm^{-2} K^{-2} for 5-nm- and 20-nm-thick ZnO, respectively. These values are similar to the theoretical value of 26.4 A cm^{-2} K^{-2} for n-GaN. This result means that barrier inhomogeneity can explain the forward current transport for both samples.

Figure 5a shows the C–V characteristics obtained at 1 MHz, exhibiting accumulation and depletion regions, subsequently. With increasing reverse bias, the capacitance decreased continually for 20-nm-thick ZnO. For 5-nm-thick ZnO, the capacitance first decreased then increased, which might be due to the large leakage current. Figure 5b shows the carrier concentration profiles versus junction depth in the GaN layer. The carrier concentrations for both samples were uniform over the depletion regions, but the values were slightly higher for 5-nm-thick ZnO.

From the C–V measurements, we also extracted the barrier height. Here, we analyzed the C–V data measured at 100 kHz, to minimize the measurement error due to the series resistance. The capacitance in a diode is related to the applied voltage through the equation[28]

$$A^2/C^2 = 2\left(\frac{V_{bi} - kT/q - V}{qN_D\varepsilon_S\varepsilon_0}\right), \tag{3}$$

where V_{bi} is the built-in potential, N_D is the donor concentration, and ε_S is the dielectric constant of the semiconductor. From the slope of A^2/C^2 versus V plots as shown in Fig. 5c, the N_D values were calculated to be 3.0×10^{17} cm^{-3} and 1.8×10^{17} cm^{-3} for 5-nm- and 20-nm-thick ZnO, respectively. The barrier height values were then obtained from $q\varphi_B^{(C-V)} = qV_i + q\xi + kT$, where V_i is the intercept with the voltage axis according to Eq. 3. Barrier heights of 1.73 eV and 1.86 eV were calculated for 5-nm- and 20-nm-thick ZnO, respectively. The $q\phi_B^{C-V}$ values for both samples were much higher than the homogeneous barrier height ($q\phi_B^{hom}$) or zero-bias mean barrier height ($q\bar{\varphi}_B$). The presence of a thin oxide layer might be expected to increase the barrier height obtained from C–V measurements.[33,34] Using C–V data, Greco et al. obtained a barrier height of 1.72 eV for the Ni Schottky contact to bulk GaN.[35] The presence of residual contamination from processing was suggested as one possibility to explain the high barrier height obtained by C–V analysis. The higher value of $q\phi_B^{C-V}$ compared with $q\phi_B^{I-V}$ in Ni/n-TiO_2/p-Si/Al heterojunction diodes is associated with nonuniformity in the interfacial layer and the distribution of interfacial charges at the metal–semiconductor interface.[36] At present, we conjecture that the presence of a nonuniform interfacial layer at the

Pt/ZnO interface could be one reason for the high $q\phi_B^{C-V}$ values.

The series resistance is another important parameter determining the device performance. According to the method suggested by S. Cheung and N. Cheung, the series resistance can be obtained from the relation[37]

$$dV/d(\ln I) = nkT/q + IR_S. \quad (4)$$

Figure 6a shows plots of dV/d(ln$I$) versus I obtained from one diode. Based on this method, the series resistance was found to be 20.83 ± 1.45 Ω and 24.53 ± 4.67 Ω for 5-nm- and 20-nm-thick ZnO, respectively. The series resistance was also calculated from the values of the capacitance (C_m) and conductance (G_m) measured at sufficiently high frequencies and in the strong accumulation region, given by Ref. 38

$$R_S = \frac{G_m}{G_m^2 + (\omega C_m)^2}, \quad (5)$$

where ω (= $2\pi f$) is the radial frequency. The voltage-dependent series resistance calculated according to Eq. 5 using the values measured at 1 MHz is shown in Fig. 6b. The series resistance increased up to a maximum and then decreased between 0 V and 1 V. Such voltage dependence has been associated with a particular distribution of localized interface states.[39,40] At high voltage, the series resistance showed almost constant values of 27 Ω and 34 Ω for 5-nm- and 20-nm-thick ZnO, respectively. As for the I–V data, the series resistance was higher for the 20-nm-thick ZnO than for the 5-nm-thick ZnO.

The parallel conductance method was applied to clarify the interface trap density. In this method, the parallel conductance (G_p/ω) is described as a function of the radial frequency and information on the trap density (D_T) and trap response time (τ_T) is provide by the equation[34]

$$\frac{G_p}{\omega} = \frac{q\omega\tau_T D_T}{1 + (\omega\tau_T)^2}. \quad (6)$$

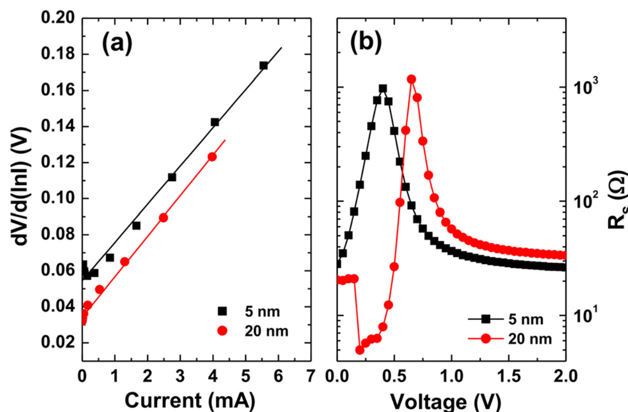

Fig. 6. (a) dV/d(ln$I$) as a function of I and (b) voltage dependence of series resistance measured at 1 MHz.

Using the experimental and fitting data shown in Fig. 7a and b, the trap energy levels below the GaN conduction band ($E_C - E_t$) were calculated from τ_T according to Shockley–Read–Hall statistics.[34]

$$\tau_T = \frac{1}{v_{th}\sigma_n N_C}\exp\left(\frac{E_C - E_t}{kT}\right), \quad (7)$$

where v_{th} is the thermal velocity, σ_n is the electron capture cross-section, and N_C is the effective density of states in the GaN conduction band. The calculated trap density shown in Fig. 7c shows that the trap density for 5-nm-thick ZnO was slightly higher than that for 20-nm-thick ZnO. However, the difference is not significant.

We also calculated the interface state density from the forward I–V characteristics. By considering both the voltage-dependent ideality factor $n(V) = q/kT(dV/d(\ln I)$ and the effective barrier height $\varphi_e = \varphi_B + (1 - 1/n(V))(V - IR_S)$ from the forward I–V data, the distribution of the interface state density (N_{SS}) was calculated. An ideality factor exceeding unity due to interface states is related to the thickness of the interfacial layer (δ) and interface state density as follows:[41]

$$N_{SS}(V,T) = \frac{1}{q}\left[\frac{\varepsilon_i\varepsilon_0}{\delta}\{n(V,T) - 1\} - \frac{\varepsilon_S\varepsilon_0}{W_D}\right], \quad (8)$$

where W_D is the depletion width and ε_i is the dielectric constant of the interfacial layer. The value of $\varepsilon_i\varepsilon_0/\delta$ was extracted from the C–V data in the accumulation region ($C_i = \varepsilon_i\varepsilon_0 A/\delta$, where A is the contact area).[42] The energy level of interface states at the n-type semiconductor surface (E_{SS}) and the effective barrier height can be described as $E_C - E_{SS} = (q\varphi_e - qV)$. Using this process, the interface state density was calculated for both samples. Figure 8a clearly shows that the interface state density for 5-nm-thick ZnO is higher than that for 20-nm-thick ZnO. If the interface states are primarily located along the current path, the forward I–V characteristics can provide an estimation of those local interface states.[43,44] Therefore, the

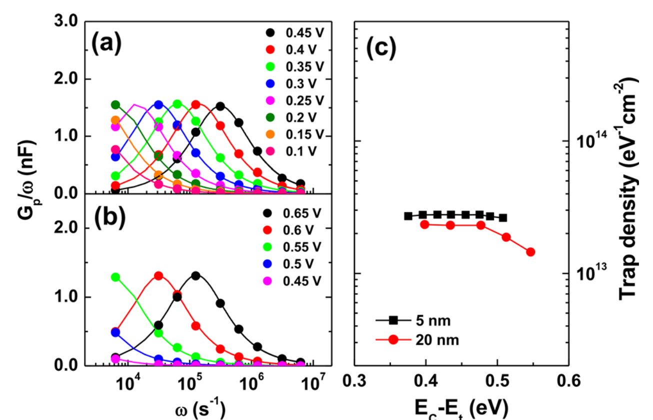

Fig. 7. Frequency-dependent parallel conductance for (a) 5-nm- and (b) 20-nm-thick ZnO and (c) resulting trap density for both samples.

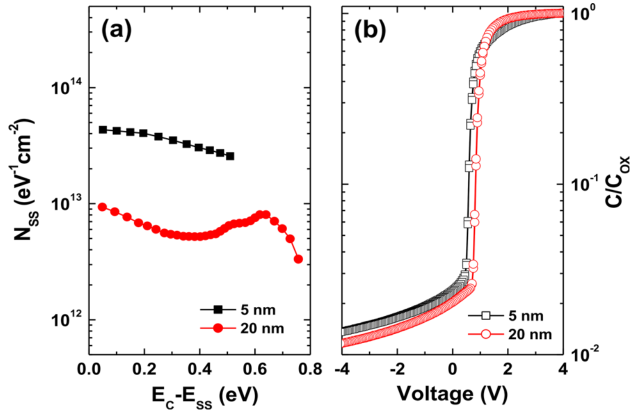

Fig. 8. (a) Energy distribution of interface state density obtained from forward *I–V* data and (b) *C–V* hysteresis plots obtained at 1 MHz.

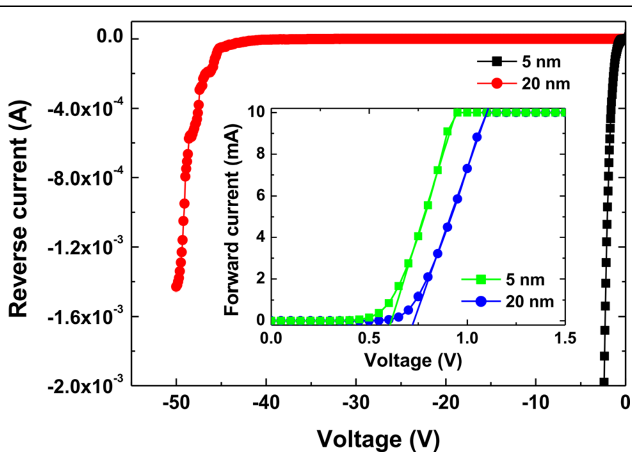

Fig. 9. Reverse-bias *I–V* curves, and forward *I–V* curves in the inset.

higher interface state density for 5-nm-thick ZnO indicates that the contribution of interface states to the current conduction is more significant. Figure 8b shows the *C–V* hysteresis curves measured at 1 MHz. The voltage shift is not distinct for both samples. This indicates that the oxygen-related defects, if present, were generated marginally during the ZnO deposition.

Figure 9 shows the reverse *I–V* characteristics for both samples. A reverse breakdown voltage of ∼ 45 V was obtained for 20-nm-thick ZnO, similar to that for the Au Schottky contact to *n*-GaN on sapphire substrate.[45] However, this value is much lower than reported in previous studies on bulk GaN-based Schottky contacts.[46–48] Note that we did not employ a guard ring structure or field-plate electrode for edge termination. Furthermore, a theoretical model of avalanche breakdown (V_B) in GaN predicts that the dependence of V_B on the carrier concentration can be described as $V_B \propto 1/N_D^{3/4}$.[48] The carrier concentration of bulk GaN (2×10^{17} cm^{-3}) is higher than reported in other works ($\sim 5 \times 10^{15}$ cm^{-3}).[47,48] Considering these facts, we can improve the reverse breakdown characteristics of the *n*-GaN Schottky contact further. The turn-on voltages in the linear forward *I–V* characteristics (Fig. 9, inset), corresponding to the intercepts of the linear fits with the voltage axis, were found to be 0.61 V and 0.73 V for 5-nm- and 20-nm-thick ZnO, respectively. The low barrier height for 5-nm-thick ZnO would be the main reason for the lower turn-on voltage.[49]

Finally, energy-dispersive x-ray spectroscopy (EDS) was carried out for 20-nm-thick ZnO. Figure 10a shows the atomic percent versus depth profile for each element. It was observed that the ZnO layer effectively suppressed diffusion of Pt atoms into the GaN layer. Figure 10b shows a cross-sectional scanning transmission electron microscopy (STEM) image taken from the ZnO/GaN interface. The interfacial oxide layer is barely observed at the ZnO/GaN interface. These features might result in good device performance for 20-nm-thick ZnO. The STEM image in Fig. 10b shows that ZnO films grown by ALD at 100°C are polycrystalline.

Based on these results, energy band diagrams were drawn for the *n*-GaN Schottky contact with ultrathin ZnO films (Fig. 11). The bandgap energy (E_g) values of ZnO and GaN are 3.37 eV and 3.4 eV, while their electron affinities (χ) are 4.35 eV and 4.2 eV, respectively.[8] The W_D values obtained from *C–V* analysis were determined to be 77.4 nm and 102.6 nm for 5-nm- and 20-nm-thick ZnO, respectively. Hence, direct tunneling would hardly occur for both samples. The ZnO layers were also fully depleted for both samples, meaning that ZnO/*n*-GaN heterojunction diodes acted as Schottky barrier diodes. Due to the higher interface state density for 5-nm-thick ZnO, both the tunneling and TE currents would contribute to the total current under forward-bias condition (Fig. 11a). This is related to the lower effective barrier height and higher ideality factor. Under reverse-bias conditions (Fig. 11c), the energy barrier became thinner and thus tunneling occurred more easily. For 20-nm-thick ZnO, the lower interface state density as well as thicker energy barrier would reduce the possibility of tunneling occurring. Thus, the TE current would be dominant under forward-bias conditions (Fig. 11b). The thermally activated process related to trap-assisted tunneling would govern the current flow under reverse-bias conditions (Fig. 11d).

The results of this work thus indicate that the electrical properties of the *n*-GaN Schottky contact such as the barrier height, ideality factor, and reverse leakage current can be modulated significantly by changing the ZnO thickness. Furthermore, ZnO layers of different thicknesses can also be formed on one substrate by combining atomic layer etching (ALE) of ZnO.[50] Recently, GaN has been grown successfully by ALD at temperatures below 300°C using various substrates such as F-doped tin oxide glass,[51] Si,[52,53] sapphire,[54] and flexible polyethylene naphthalate (PEN).[55] ALD growth of GaN has even been reported to be possible

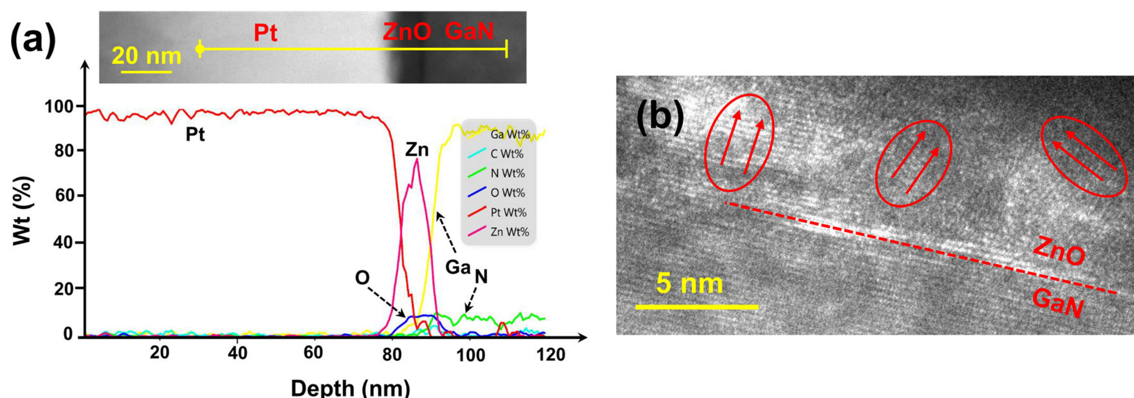

Fig. 10. (a) Atomic percent versus depth profiles measured from an EDS line scan and (b) cross-sectional STEM image at ZnO/GaN interface.

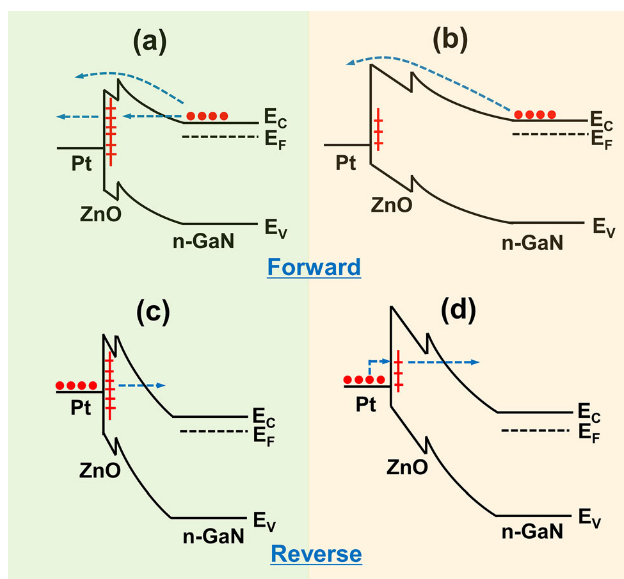

Fig. 11. Schematic energy band diagrams for (a, c) 5-nm- and (b, d) 20-nm-thick ZnO under forward- (a, b) and reverse-bias (c, d) conditions.

at lower temperatures such as 115°C[56] or room temperature.[57] Therefore, it is possible to grow both ZnO and GaN films on many kinds of substrate, including flexible plastic substrates. This will expand the applications of ZnO/GaN heterojunction devices.

CONCLUSIONS

ZnO films of two different thicknesses (5 nm and 20 nm) were grown on GaN single-crystal substrates by thermal ALD, and the electrical properties of n-GaN Schottky contacts modified by such ultrathin ZnO films were investigated. Compared with 5-nm-thick ZnO, a higher barrier height and lower ideality factor were observed for 20-nm-thick ZnO. Lateral barrier inhomogeneity with TE could explain the forward I–V characteristics observed for both samples. According to both the parallel conductance method and forward I–V data, a lower interface state density was observed for 20-nm-thick ZnO, indicating an improved interface quality.

ACKNOWLEDGMENTS

This study was supported by the Advanced Research Project funded by SeoulTech (Seoul National University of Science and Technology).

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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