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A Review on the Recent Advancements in Tin Oxide-Based Thin-Film Transistors for Large-Area Electronics

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Amorphous oxide semiconductors have gained significant attention in the past few decades and have emerged as a promising material for thin-film transistors (TFTs) because they offer high carrier mobility (> 10–50 cm^2/V s) and uniformity. In particular, amorphous indium-gallium-zinc-oxide (a-IGZO) has been widely employed as an active channel material in TFTs owing to its high mobility. However, indium-based TFTs suffer from stability problems under positive, negative, and illumination bias stress conditions, which limits their applications in flat-panel displays. Moreover, the limited supply of indium and growing demand for high-stability TFTs with better electrical performance has led to the introduction of tin oxide as a promising solution to replace indium in TFTs. This review provides an overview on the progress and recent developments in indium-free tin oxide-based TFTs for large-area electronics, with special emphasis on the sputtering technique. In addition, the source of the dual conductivity of tin oxide is addressed, which will be helpful in designing complementary metal oxide semiconductor devices. The instability problems and approaches to improve the electrical performance of tin oxide TFTs are also discussed.

Key words: Metal oxide semiconductors, thin-film transistors, amorphous oxide semiconductor, tin oxide, sputtering

INTRODUCTION

The advances in conventional thin-film transistors (TFT) have played a major role in the development of the electronics industry. However, the growing demand for electronics and optoelectronics with updated features, such as high carrier mobility, ultrahigh resolution, fast response, transparency, and flexibility, requires the enhancement of existing materials and the development of new ones to be used as active channel layer for TFTs. Despite the high carrier mobility (> 80 cm^2/V s) of conventional crystalline and polycrystalline silicon (poly-Si)-based TFTs, their several limitations, such as high processing temperature, need for laser processing and low band gap (1.1 eV), restrict their use in large-area applications.[1–3] In addition, their high processing temperature (> 450°C) and rigidity limits their application in flexible substrates, whereas the grain boundaries in poly-Si TFTs create non-uniformities that lead to carrier mobility variation and change in the response time, resulting in significant changes in image visualization, which is undesirable in display devices since each pixel is controlled by an individual TFT.[2] Investigations of hydrogenated amorphous silicon (a-Si:H) and organic TFTs helped in overcoming these drawbacks. The a-Si:H TFTs provide a high level of device uniformity; however, their carrier mobility (~ 0.5–1 cm^2/V s) is three orders of magnitude lower than that of crystalline silicon TFTs (~ 100 cm^2/V s) owing to the deterioration in the carrier transport path. Moreover, the switching speed of a-Si:H TFTs is relatively very low, and

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the deteriorations in the electrical properties of *a*-Si:H TFTs caused by the photo-illumination sensitivity affect device stability.[4] Organic TFTs are inexpensive compared to *a*-Si:H TFTs and can be fabricated at low temperature. However, they suffer from low carrier mobility and inferior potential bias stability, which limits their application in display devices.[1]

TFTs based on metal oxide semiconductors have gained considerable attention in the past few decades. They offer a promising solution for next-generation flat-panel displays (FPD) due to several advantages, such as high carrier mobility, low process temperature, wide variety of chemical composition, control of carrier density, compatibility with a wide range of substrates, and high transparency.[5–10] Compared with crystalline metal oxide semiconductors, the structure of amorphous oxide semiconductors (AOS) is extremely sensitive to deposition conditions, stoichiometry, and composition. This results in high uniformity, as well as tuneable optical and electrical properties, which are the key factors for display applications.[8–10] In particular, transparent amorphous oxide semiconductors (TAOS) offer impressive features comparable to crystalline semiconductors (c-SC), such as very high carrier mobility ($>$ 10–50 cm^2/V s).[11] Other advantages of TAOS include low-temperature fabrication, ionic bonding, and wide-range tunability of electrical and optical properties.[5] The display market forecast conducted by MarketsandMarkets in 2017 indicated that the transparent display market would grow from USD 408 million (in 2018) to USD 2591 million (in 2023), reaching the highest compound annual growth rate (CAGR) of 44.7%,[12] which confirms the promising future of TAOS in next-generation transparent display devices.

The introduction of Hosono's hypothesis in 1996 resulted in considerable research activity in AOS TFTs with multiple post-transition metal cations, such as indium, zinc, tin, and gallium. According to this hypothesis, metal oxides composed of heavy metal cations with an electronic configuration of $(n-1)\ d^{10}ns^0\ (n \geq 4)$ have remarkable transparency and carrier mobility in the amorphous state due to the overlapping of the ns orbitals (where n is the principal quantum number).[13] Nomura et al. explained this by the carrier transport path of covalent semiconductors, which is composed of strong directional sp^3 orbitals.[14] Therefore, any structural disorder can introduce variations in the electronic levels, resulting in low mobility. However, in AOS, the contribution of oxygen 2*p* orbitals in bonding is small, and hence there is a high possibility for direct overlapping of neighbouring metal ns orbitals, even in the amorphous phase, which results in high mobility.[14] The majority of AOS TFTs reported to date have employed zinc oxide (ZnO)- and indium oxide (In_2O_3)-based materials as active channel materials. In particular, indium-gallium-zinc oxide (IGZO) TFTs have been widely used due to their high carrier mobilities ($\sim$ 10 cm^2/V s) and high current ON/OFF ratios (approximately $I_{ON}/I_{OFF} > 10^7$).[5,6] Since the introduction of IGZO by Nomura et al. in 2004, research on IGZO has increased significantly. Since 2012, IGZO has been commercially used by leading FPD companies such as Sharp, LG, Razer, and Samsung.[8] However, indium is a scarce element, and its presence in the earth's crust is only 0.25 ppm. Thus, the expected depletion of indium represents a threat to FPD devices based on IGZO. A recent survey forecasted that the indium market is expected to grow at a CAGR of 9.5% between 2017 and 2024, which can cause tremendous rise in its price.[15] Moreover, *a*-IGZO TFTs have been reported to show instability under photo-illumination conditions, which remarkably shifts the threshold voltage and leads to negative bias stress instability.[9] Gallium in *a*-IGZO is acid-soluble and sensitive to wet etching, which leads to damage of the back-channel surface during photolithography processes.[16] Likewise, Zn is assumed to cause instability of the device performance since it forms weak bonds with the oxygen ions in ternary structure.[17,18] Therefore, there is an urgent need for the development of In- and Zn-free TAOS material to address the above-mentioned issues, meanwhile offering better electrical and optical properties.

Tin (Sn) is an abundant metal in the earth's crust, resulting in its being less expensive ($15.203/kg) compared to indium (In) ($\sim$ $750/kg).[19] The dual valency of tin (group 14) with +2 and +4 oxidation states causes tin oxide to exist in two stable states, i.e., tin monoxide (SnO) and tin dioxide (SnO_2), respectively. This enhances the wide-range tunability of electrical properties of the device. The electronic configuration of Sn^{4+} ($4d^{10}5s^2$) is similar to that of In^{3+} ($4d^{10}5s^0$).[20] The band structure of tin oxide (SnO_x) is similar to indium oxide, and the high bonding dissociation energy of Sn^{4+} is higher (Sn-O $\sim$ 531.8 kJ/mol) than that of In^{3+} (In-O $\sim$ 320.1 kJ/mol), Ga^{3+} (Ga-O $\sim$ 353.5 kJ/mol), and Zn^{2+}(Zn-O $\sim$ 284.1 kJ/mol).[21] Tin oxide is an intensively studied oxide material because it offers both high transparency and conductivity, which makes it unique among the elements of group 14. Moreover, SnO_x can provide both *n*-type and *p*-type conductivities by tuning the deposition conditions. Hence, SnO_x could be an alternative to IGZO to replace In and Zn in TFTs. This review tackles the development and characteristics of indium and zinc-free tin oxide (SnO_x)-based TAOS thin films as active channel materials in TFTs for FPD and complementary metal oxide semiconductor (CMOS) device applications.

HISTORICAL PERSPECTIVE OF TIN OXIDE TFTS

The concept of metal oxide semiconductor transistors emerged in the early 1930s. However, due to the lack of progress in vacuum technologies, it was not until the mid-1960s that a practical demonstration was achieved. In 1964, Klasens and Koelmans reported a tin dioxide-based TFT, as the first transparent oxide TFT.[22] In 1970, Aoki et al. reported a SnO_2 TFT, which exhibited poor electrical performance, including the negligible transfer curve and inability to turn off the device.[23] Both these TFTs showed transconductance of 0.3 m mho. Until 1996, no major works on tin oxide TFTs were published, which may be attributed to the emergence of *a*-Si-, poly-Si-, and organic semiconductor-based TFTs and to the poor electrical performance of the early tin oxide-based TFTs. In 1996, Prins et al. reported antimony-doped SnO_2 as a channel layer in transparent ferroelectric transistors.[24] The authors mentioned that they fabricated a fully transparent all-oxide TFT, which is noteworthy. Nevertheless, the TFT suffered from low switching ($I_{ON}/I_{OFF} \sim 10^2$) with a mobility of 5 cm^2/V s. In 2003, Wöllenstein et al. employed a SnO_2 TFT in a novel gas sensor device, which was an initiative for the SnO_x TFT-based gas sensors.[25] In 2004, Presley et al.[26] fabricated an amorphous SnO_2 TFT with a carrier mobility of 0.8 cm^2/V s and I_{ON}/I_{OFF} ratio of about 10^5. They reported that their device required very large turn-off voltage and attributed the low carrier mobility to the poor crystallinity. In 2008, Ou et al. demonstrated the fabrication of a complementary inverter by tuning the annealing temperature, which created a *p*-type conductivity in tin oxide thin films, with carrier mobility of 0.011 cm^2/V s and I_{ON}/I_{OFF} ratio $\sim 10^3$.[27] The first *p*-channel TFT with SnO as the channel layer material, which offered a carrier mobility and I_{ON}/I_{OFF} ratio of μ_{sat} = 0.7 cm^2/V s and $\sim 10^2$, respectively, was reported by Ogo et al. in 2009.[28] This work led to the growth of tin oxide TFTs for CMOS applications. In 2011, Nomura et al.[29] reported the fabrication of ambipolar TFT with polycrystalline SnO as an active channel layer material as well as a CMOS-like inverter by using two SnO ambipolar TFTs, which was the first work to demonstrate the possibility of fabricating an oxide-based complementary inverter based on a single channel material. In recent years, research in tin oxide-based TFTs has progressed rapidly and is discussed in the following sections.

ORIGIN OF THE *n*-TYPE AND *p*-TYPE CONDUCTIVITIES IN TIN OXIDE

Most oxide semiconductors show *n*-type conduction which limits their application in unipolar *n*-type TFTs, and hence *p*-type oxide semiconductor materials were investigated to extend their applications. In addition, *p*-type oxide semiconductors can be used in a wide range of applications such as CMOS circuits, active-matrix liquid-crystal displays (AMLCD) and flexible electronics.

SnO_2 is an *n*-type transparent semiconductor with a wide band gap of 3.6 eV, and it crystallizes into a tetragonal rutile structure (space group $P4_2/mnm$).[30–33] SnO_2 is the most stable state of tin oxide and is reported have a strong *n*-type conductivity due to the presence of intrinsic defects such as oxygen vacancies (V_O).[34,35] Kılıç et al. used first-principles calculations to prove that the *n*-type conductivity in undoped SnO_2 is governed by the shallow donor levels produced by tin interstitials (Sn_i) and V_O due to the multivalent nature of tin.[20] They also reported that Sn_i has a more significant effect on carrier mobility compared to V_O owing to some properties such as low formation energy, and donor level formation inside the conduction band which leads to instantaneous conductivity. These defects are attributed to the natural non-stoichiometry of SnO_2. Moreover, spherically symmetric ns orbitals of metal oxides result in a very low electron effective mass (m_e), which leads to high carrier mobility in *n*-type oxides, since low m_e causes uniformity in electron charge density distribution and decreases scattering.[36] SnO_2 has a very low electron effective mass (0.18 m_e) compared to *a*-IGZO (0.33 m_e),[37,38] which indicates that SnO_2 has a better mobility than *a*-IGZO.

SnO exists in a metastable state and exhibits *p*-type conduction.[39] The structure of SnO is layered in a Sn-O-Sn sequence similar to that of lead oxide (PbO), which has a tetrahedral coordination. SnO has a direct band gap of 2.5–3.0 eV and indirect band gap of 0.7 eV.[32,40]. Figure 1 shows the differences between the structures of SnO and SnO_2. It is hard to achieve a high hole mobility in *p*-type oxide materials because the 2*p* orbitals of the oxygen ions form a deep localized valence band maximum (VBM) and the hole transport paths are anisotropic due to hopping conduction.[41,42] Nevertheless, SnO is a promising *p*-type oxide semiconductor since its VBM is composed of O 2*p* hybridized orbitals.[42,43] The spherical Sn 5*s* orbitals and O 2*p* orbitals form a hybridized VBM which increases the hole mobility.[41] Figure 2 shows the band gaps of SnO_2 and SnO. Ogo et al. reported that the formation of hybridized orbitals in SnO was attributed to the pseudo-closed ns^2 orbital of Sn metal cations.[28]

The *p*-type conductivity of SnO was ascribed to the tin vacancies (V_{sn}) and oxygen interstitials (O_i).[43] Fortunato et al.[44] reported that V_{sn} plays a more important role in hole generation, compared to O_i, because the V_{sn} formation takes place easier than O_i. Togo et al.[45] confirmed this using first-principles calculations, and they concluded that O_i does not contribute to the conductivity. The formation of tetravalency (4+) in Sn atoms was attributed to the presence of interstitial oxygen atoms, since these O_i attract a lone pair of electrons from the nearest-neighbouring Sn atoms.[46] Figure 3 shows

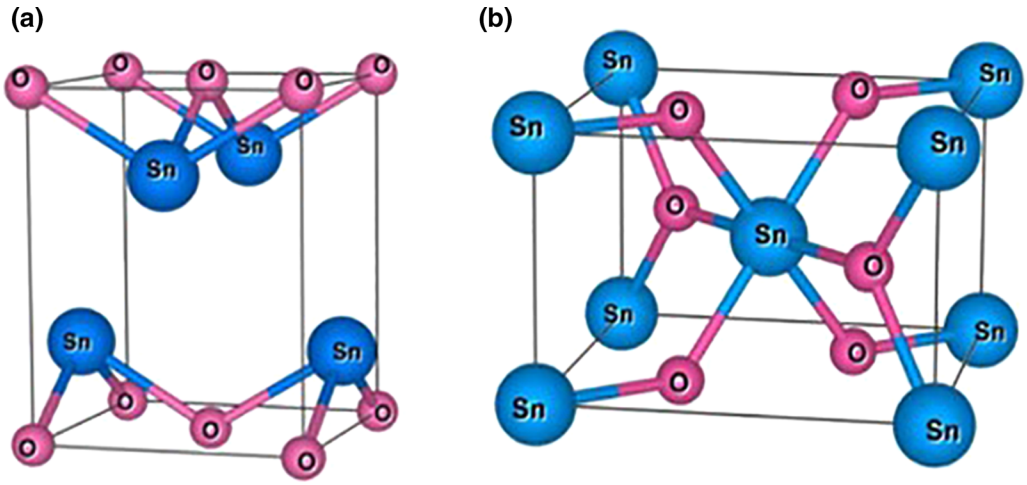

Fig. 1. Crystal structure of tin oxide (a) SnO, (b) SnO_2.

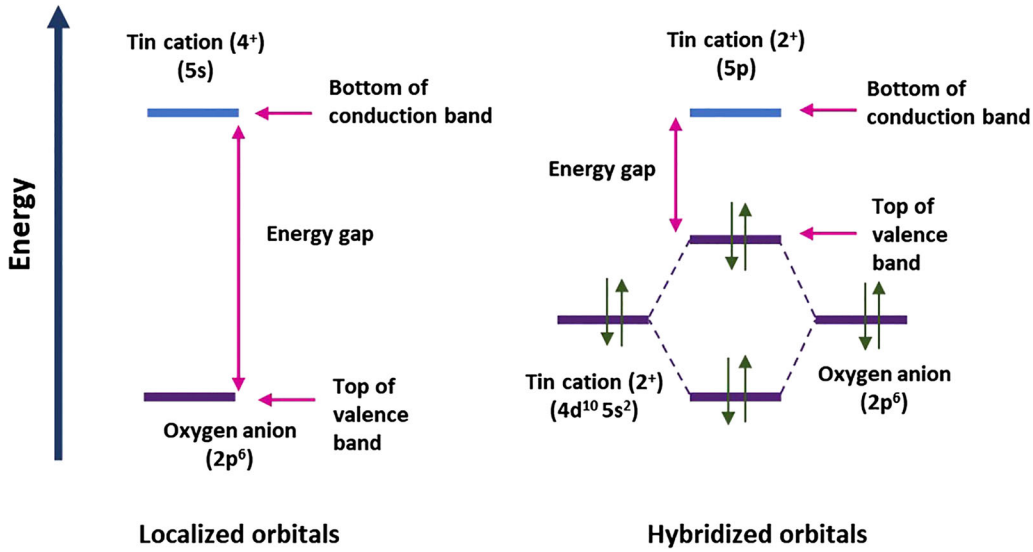

Fig. 2. Comparison between the band gaps of SnO_2 and SnO.

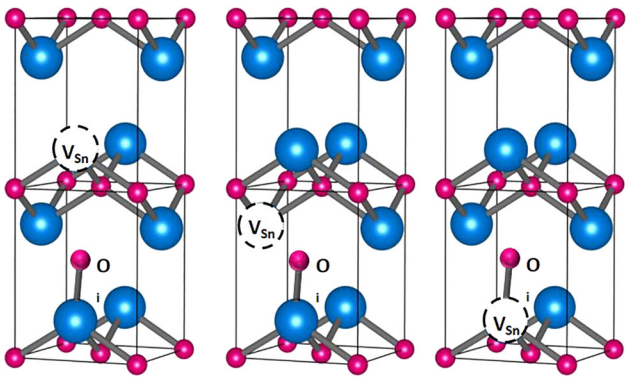

Fig. 3. Possible models containing V_{sn}–O_i pairs in SnO.

the possible models of SnO with V_{sn} and O_i. The Fermi levels (E_f) of SnO were found to be closer to the VBM, whereas, in the case of SnO_2, the band gap is below E_f, which further confirms the *p*-type conductivity in SnO.[41] In 2019, Barros et al. reported high hole mobility (μ_{sat} = 4.6 cm^2/V s) and a high I_{ON}/I_{OFF} ratio (7×10^4).[43]

GENERAL DEVICE STRUCTURE AND ELECTRICAL PARAMETERS OF TFTS

Typically, TFTs are fabricated in bottom-gate and top-gate configurations based on the position of the gate and source/drain electrodes with respect to the semiconductor layer, which has a coplanar or a staggered structure.[46,47] The overall design principle for a TFT is that the semiconducting layer should be in direct contact with the two electrodes (source/drain), and the third electrode (gate) should be separated by a dielectric layer. The gate modulates the conductivity of the semiconductor layer through the dielectric material, which is in accordance with the field effect principle. Figure 4 illustrates the structures commonly used for TFTs.

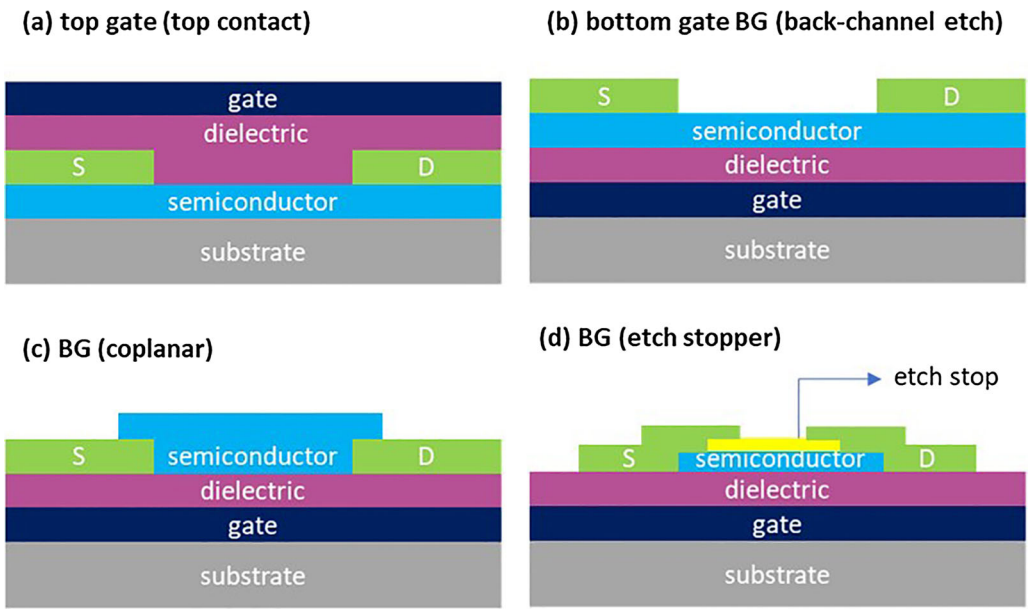

Fig. 4. Commonly used TFT configurations. (a) Top gate (top contact). (b) Bottom gate BG (back-channel etch). (c) Bottom gate (coplanar). (d) Bottom gate (etch stopper).

Generally, most of the SnO_x TFTs are fabricated in a bottom-gate (BG) configuration, which employs a staggered structure with a top contact (TC). A BG-TC configuration is commonly used, since it is an easily processable structure, in which only a few masks are required, and the substrate itself largely acts as a gate layer (e.g., heavily doped n^+ and p^+-Si wafer), which further reduces the deposition steps and cost of fabrication.[6,47,48] However, this structure shows some drawbacks, such as the changes in the TFT characteristics when the back-channel is exposed to ambience, and damage to the back-channel during patterning or etching of the source/drain contacts.[47,49] To address these issues, an appropriate passivation layer or etch stopper should be used.

In order to have a better understanding of the electrical characteristics which determine the TFT device performance, it is essential to have a clear idea about the device parameters, such as field effect mobility (μ_{FE}), subthreshold swing (S), and threshold voltage (V_{th}).[46,47] Mobility is the efficiency of carrier transport through an active channel, and it can be described by drain current (I_D) with respect to drain voltage (V_D) as follows:

$$I_D = \frac{W\mu C_i}{L}\left[(V_G - V_{th})V_D \frac{V_D^2}{2}\right] \quad (1)$$

where L is the active channel length; W is the active channel width; V_G is the gate voltage; C_i is the capacitance per unit area of the gate insulator. Equation (1) can be used to calculate the mobility. The threshold voltage (V_{th}) is defined as the minimum gate-source voltage (V_{GS}) required to create a conducting path between the source and drain.

Transconductance (g_m) is the rate of the change in I_D to the change in V_G, which is used to calculate the mobility.

$$g_m = \frac{\partial I_D}{\partial V_G} \quad (2)$$

In linear regimes (i.e., g_m at low V_D), mobility is defined as the linear mobility (μ_{lin}):

$$\mu_{lin} = \frac{Lg_m}{WC_iV_D} \quad (3)$$

In saturation regimes (i.e., $V_D \gg (V_G - V_{th})$, g_m at high V_D), saturation mobility (μ_{sat}) is defined by the following equation:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \quad (4)$$

Subthreshold swing is defined as the V_G required for one decade increase in I_D and can be calculated using the transfer characteristics as follows:

$$S = \frac{dV_{GS}}{d(\log_{10} V_D)} \quad (5)$$

S is useful in determining the switching speed of the TFT and the total trap density near the semiconductor/gate-dielectric interface.

The poor stability of the AOS TFTs under stress conditions is one of the major issues which decreases their performance and limits their application in display devices. A shift in threshold

voltage (ΔV_{th}) is created by the electrical and illumination stresses imposed on TFTs while operating in devices such as AMLCDs. A change in luminance of approximately 20% was reported in organic light-emitting diode (OLED) pixels, even at a ΔV_{th} of the driving transistor = 0.1 V.[50]

In order to examine the stability of the TFTs, accelerated operating tests, such as positive bias stress (PBS), positive bias temperature stress (PBTS), positive bias illumination stress (PBIS), negative bias stress (NBS), negative bias temperature stress (NBTS), and negative bias illumination stress (NBIS) tests, are typically performed. The electron–hole pairs generated by light and heat are transported to the gate surface and trapped in the gate-dielectric interface.[49] These charge traps in the gate-dielectric interface and the increase in the shallow donors in the channel result in the occurrence of ΔV_{th} in TFTs.[51] The stability of TFTs can be significantly enhanced by doping, since it can reduce the charge trap density.[50] The stability of TFTs can also be improved by using a suitable device structure, passivation layer, dielectric material, and thermal treatments.[52]

EMERGING APPLICATIONS OF SnO_x-BASED TFTS

Flat-Panel Display Devices

The AOS TFTs find their most dynamic application in display devices such as AMLCD and OLED displays. AMLCDs and OLEDs utilize TFTs for switching and operating the individual pixels. Typically, a simple pixel circuit for an active-matrix OLED (AMOLED) display requires two TFTs in which one acts as switching transistor (sends data to the pixel) and the other acts as a driving transistor (drives the current to the LED).[52,53] The OLED displays employing compensation circuits require additional TFTs as well as two capacitors. For small-sized AMOLED displays like smartphone screens, higher carrier mobility ($\sim$ 100 cm^2/V s) is required for fast operation within small pixel dimensions. The mobility requirement for large-sized AMOLED displays is about 30 cm^2/V s.[52] Furthermore, recent research has focused on completely transparent flexible TFTs for next-generation display devices. Studies have indicated that a tin oxide TFT can effectively satisfy the mobility requirements of the current display devices. The prominent research and development in tin oxides and their composite-based TFTs in the past few years has resulted in their near commercialisation in the display device industries.

CMOS-Like Inverters

CMOS inverters can be used for integrated circuit applications due to their low power consumption, high logic swing output, high noise margin, and high circuit integration density.[54] CMOS inverters comprises both *n*- and *p*-type TFTs to perform logic operations. As mentioned earlier, *n*-type oxide semiconductors are extensively studied and have shown exceptional electrical performance compared to their *p*-type counterparts. Initially CMOS inverters used the combination of different oxide/organic active channel materials for *p*-type TFTs, due to the lack of high-performance *p*-type oxide semiconductors.[55,56] The fabrication of completely oxide-based CMOS-like inverters requires the development of high-performance *p*-type oxide semiconductors. Moreover, oxide semiconductors operating in ambipolar mode are used extensively in CMOS-like inverters to minimize the fabrication and patterning processes and to produce compact circuit architectures. The fabrication constraints of oxide ambipolar transistors are the wide band gap and sub-gap states. SnO exhibits very good electrical performance as a *p*-type AOS and shows excellent ambipolar behaviour by effective conduction of both electrons and holes in a TFT. The low electron effective mass ($\sim$ 0.4 m_e), low hole effective mass ($\sim$ 0.6 m_h), and small fundamental band gap ($\sim$ 0.7 eV) contribute to the ambipolar behaviour of SnO.[57]

The first complete oxide-based CMOS inverters, which exhibited voltage gain of $\sim$ 11, incorporated tin oxide as a *p*-type and indium oxide as an *n*-type TFT.[56] Following this work, several CMOS inverters were fabricated with tin oxide as a *p*-channel TFT and IGZO/ZnO as an *n*-channel TFT.[54] In 2008, Ou et al. fabricated a completely tin oxide-based CMOS inverter by combining two tin oxide devices with different threshold voltages that attained output gain of 2.8.[27] Yabuta et al.[58] proposed a single-step fabrication of *n*-SnO_2/*p*-SnO channel complementary circuits using a SiO_x capping layer (Fig. 5). The capping layer controlled the incorporation of excess oxygen during annealing which protected the *p*-type SnO, and the portion without SiO_x capping served as *n*-channel SnO_2.

Nomura et al.[29] fabricated the first ambipolar SnO TFT and constructed a CMOS-like inverter using two ambipolar SnO TFTs (Fig. 6). They attributed the ambipolar behaviour of SnO to the reduction trap states caused by the decrease in the channel thickness ($\sim$ 15 nm). They obtained a maximum voltage of $\sim$ 2.5, and the *p*- and *n*-type SnO TFTs exhibited μ_{sat} of 0.8 and 5×10^{-4} cm^2/V s, respectively.[29]

Nayak et al. fabricated both *p*- and *n*-type channel TFTs by controlling the concentration of hydroxyl groups (OH groups) in the dielectric layer. They used solution-derived (SD) Al_2O_3 on a part of SnO thin film and atomic layer-deposited (ALD) Al_2O_3 on the other part (Fig. 7). The large number of OH groups in the SD Al_2O_3 film acted as an additional oxygen source during annealing, which resulted in

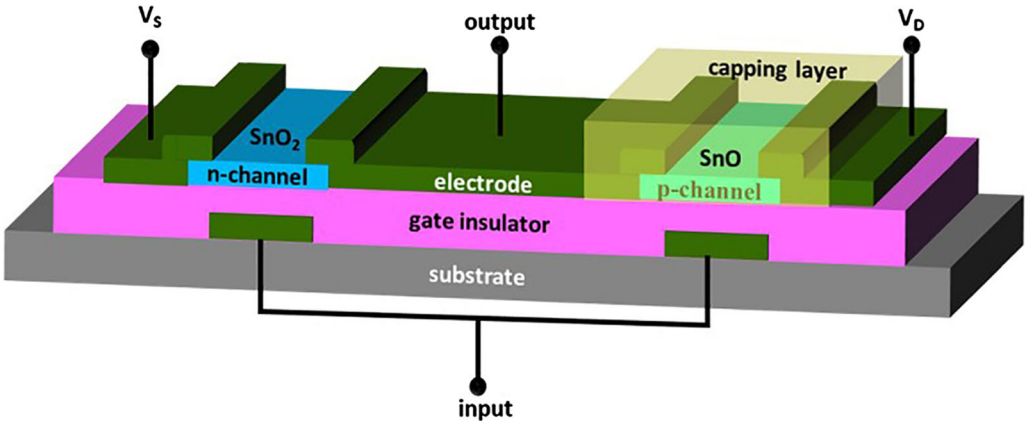

Fig. 5. Conceptual design of a SnO-based CMOS inverter.

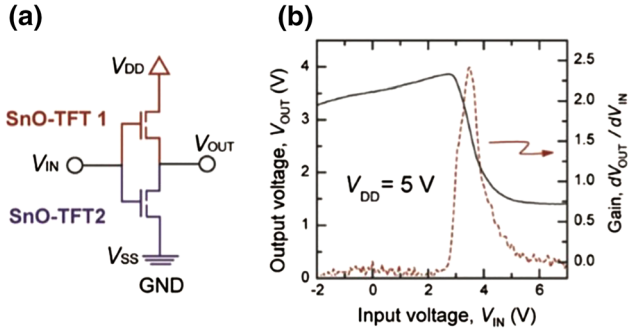

Fig. 6. (a) Circuit diagram for an inverter composed of two SnO ambipolar TFTs. (b) Inverter characteristics (in positive V_{DD} and positive V_{IN}) with supply voltage of $V_{DD} = \pm 5$ V. Reproduced with permission from,[29] Copyright 2011, John Wiley and Sons.

the conversion of SnO to SnO_2. However, due to the negligible OH content in the ALD Al_2O_3 film, the SnO phase was consistent.[59]

PROGRESS AND OPTIMIZATION OF SnO_x-BASED TFTS

In early tin oxide-based TFTs, the active channel layer was typically polycrystalline, with high carrier concentrations, and exhibited poor electrical performance such as low mobility and low ON/OFF ratio. The decrease in carrier mobility was attributed to the carrier scattering at the grain boundaries. The charge traps at the grain boundaries interrupted the movement of the charge carriers, which resulted in their decreased mobility. Qu et al. suggested that the formation of surface trap states in SnO_x TFT is attributable to the ambient adsorption of moisture and oxygen at the grain boundaries.[60] Moreover, the drop in the device performance and poor stability were attributed to the grain boundaries in crystalline SnO_x TFTs. For example, a decrease in the mobility of water-exposed SnO_x TFTs was attributed to the interaction between the hole charges and the polar water molecules at the grain boundaries, which increased the energy barrier for hole intergrain transport.[39,61] In recent years, several studies were carried out to rectify these issues that involve the utilization of a-SnO_x and shielding with a passivation layer. The major works in SnO_x-based TFTs are summarized in Table I.

As mentioned earlier, it is possible to enhance the carrier mobility in amorphous SnO_x TFTs due to the absence of grain boundaries, which agrees with the previous reports listed in Table I. In addition, the utilization of an amorphous active channel layer enhances uniformity and device stability. To address the stability issues and achieve high-performance amorphous SnO_x-based TFTs, several routes have been explored (i.e., doping, passivation, and deposition parameters), and the following section discusses the role of doping.

The Effect of Doping on the Tin Oxide Active Channel Layer

The amorphous phase can be obtained by mixing two or more cations with different ionic charges and sizes, which inhibits the crystallization process.[67] The free electrons generated by the oxygen vacancy defects result in high carrier concentration leading to large off current which requires large power consumption.[51,52] The incorporation of suitable dopants controls the V_O in AOS films.[67] Hence, doping is beneficial in attaining an amorphous phase, better stability, reduced carrier concentration, and low power consumption in AOS TFTs. Some of the dopants (Table II) used for SnO_x TFTs are discussed in this section as follows:

(1) Al-Sn-O

Notably, p-type conductivity was observed in aluminium-doped SnO_x TFTs. This can be attributed to the holes generated by the substitution of Al^{3+} ions in Sn^{4+} sites, with appropriate Al concentration

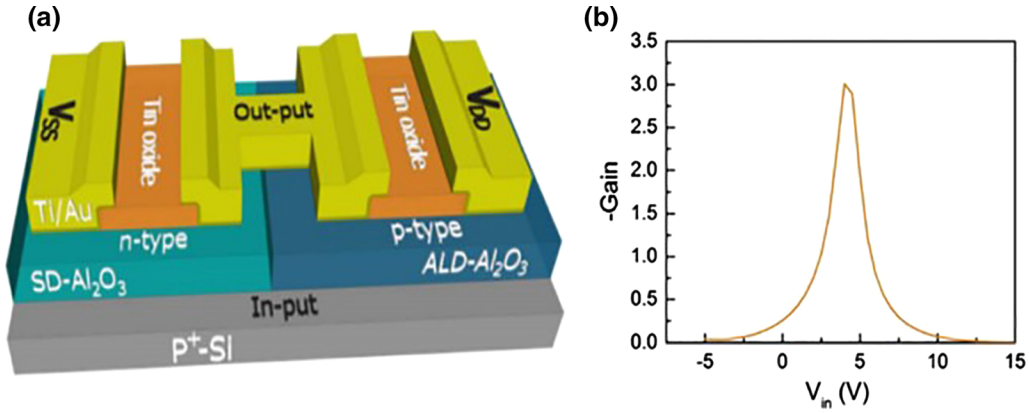

Fig. 7. (a) Conceptual CMOS inverter device structure and (b) gain characteristics of the CMOS inverter. Reprinted from[59] under the terms of the Creative Commons (CC BY-NC-ND 3.0) license.

Table I. The progress in SnO_x-based TFTs

Method	Channel	Phase/conductivity	Mobility μ (cm^2/V s)	ON/OFF ratio	Threshold voltage V_{th} (V)	Subthreshold swing SS (V/dec)	Refs.
Evaporation	SnO_2	*n*-type	g_m = 0.3 mA/V	–	–	–	22
Vacuum evaporation	SnO_2	*n*-type	g_m = 0.3 mA/V	–	–	–	23
PLD	Sb-SnO_2	Poly-cryst/*n*-type	5	10^2	–	–	24
RFMS	SnO_2	Cryst/*n*-type	0.8	10^5	−20	4	26
Reactive evaporation	SnO_2	Cryst/*p*-type	0.011	$\sim 10^3$	30.4	~ 2	27
PLD	SnO	Cryst/*p*-type	1.3	$\sim 10^2$	~ 5	7	28
RFMS	SnO	Poly-cryst/*p*-type	0.24	$\sim 10^2$	+30	–	58
RFMS	SnO	Poly-cryst/*p*-type	1.1–1.2	10^3	−5 to −12	–	44
PLD	SnO	Poly-cryst/*p*-type	0.81	10^5	–	–	29
DC reactive sputtering	SnO	Cryst/*p*-type	6.75	6×10^3	−1	7.63 to 10	62
PVD	SnO_2	Amorphous/*n*-type	147	2.3×10^7	0.27	0.11	63
RFMS	SnO	Cryst/*p*-type	4.13	6×10^2	14.6	–	34
	SnO_2	Cryst/*n*-type	16.0	10^7	3.0		
RFMS	SnO	Cryst/*p*-type	0.92	1.79×10^4	–	~ 16	64
Spin coating	SnO_2	Amorphous/*n*-type	0.23	10^6	6.8	–	65
ALD	SnO	Cryst/*p*-type	~1	2×10^6	–	1.8	66
RFMS	SnO	Cryst/*p*-type	4.6	$> 7 \times 10^4$	−10	–	43

PLD pulsed laser deposition; *RFMS* radio-frequency magnetron sputtering; *PVD* physical vapor deposition; *ALD* atomic layer deposition; *Cryst* crystalline; *poly-cryst* polycrystalline.

(> 5%).[68] The oxygen vacancies are suppressed by Al doping in SnO_x due to the strong oxidising property of Al.[68] Thus, the Al-doped SnO_x films showed an adequate oxygen content with low electron density, which resulted in the *p*-type conductivity.[68,69] Moreover, *n*-type behaviour was observed at low dopant concentrations (≤ 2.24%).[68] Lee et al. reported that Al-doped SnO_x TFTs showed an increased I_{ON}/I_{OFF} ratio ($\sim 8 \times 10^7$), high *p*-type mobility (2.27 cm^2/V s), high optical transmittance

Table II. Electrical properties of SnO TFTs with different dopants

Dopant	Dopant content	Phase/conductivity	Mobility μ_{FE} (cm^2/V s)	ON/OFF ratio	Threshold voltage V_{th} (V)	Subthreshold swing SS (V/decade)	Annealing temperature	Refs.
Al	2.2 at.%	Amorphous/*p*-type	2.27 ± 0.03	~ 8×10^7	~ 0	~ 0.68	150°C	68
Ag	3 at.%	Poly-cryst/*p*-type	1.2	2.2×10^3	−1.2	21.5	250°C	71
Si	SiO_2:SnO_2 = 5:95 wt.%	Amorphous/*n*-type	μ_{sat} = 4.2 ± 0.2	6.94×10^8	0.00	0.23	350°C	72
Si	SiO_2:SnO_2 = 5:95 wt.%	Amorphous/*n*-type	8.14	6.07×10^9	V_{on} = −1.2	0.21	~ 450°C	73
Ni	3.3 at.%	Amorphous/*n*-type	8.4	2.1×10^7	0.0 ± 0.4	0.8	300°C	75
Ga	Ga:Sn = 1:3 wt.%	Amorphous/*n*-type	25.6	10^8	−1.49	0.33	350°C	18
Ga	Ga:Sn = 1:3 wt.%	Amorphous/*n*-type	0.48	–	2.22	1.37	RT	78
Zr	1.57 at.%	Amorphous/*n*-type	1.04	7.42×10^5	V_{ON} = 1	0.78	200°C	79
Sb	Sb:SnO_2 = 2:100 wt.%	Poly-cryst/*n*-type	158	3×10^4	−1	0.2	RT	80
Hf	2.70 at.%	Amorphous/*n*-type	1.74	8.22×10^5	V_{ON} = −1	0.67	200°C	82
W	2.7 at.%	Amorphous/*n*-type	5	2.4×10^6	0.4	0.4	300°C	83
Bi	2.7 at.%	Amorphous/*n*-type	4.7	2.3×10^6	−3.9 V	1.3	300°C	84

(~ 97%), and stronger adhesion (to polyimide substrate of > 0.7 kgf/mm) than intrinsic SnO_x TFTs.[68]

(2) Ag-Sn-O

Pham et al. reported that silver-doped SnO TFTs exhibited *p*-type conductivity, and they observed the enhancement of hole mobility was attributed to Ag^+ ions, which replaced the Sn^{2+} ions in SnO films.[70] Nguyen et al. reported that introducing an optimal concentration of Ag atoms into the SnO_x lattice modified the stoichiometry of the oxide states, which led to the reduction of the Sn^{4+} state to the Sn^{2+} state.[71] The metallic Ag phase enhanced the carrier mobility (1.2 cm^2/V s) by increasing the metallic character of the valence band, which agrees with the behaviour observed in the presence of the metallic Sn phase. Owing to the degradation in the Sn^{4+} state, a significant reduction in the off current was also observed.[71] However, the electrical properties of the Ag-doped SnO_x TFTs deteriorated because of carrier scattering in the grain boundaries.[71] Figure 8 shows the comparison between the output characteristics of intrinsic and Ag-doped SnO_x TFTs.

(3) Si-Sn-O

Si-doped SnO_x (STO) films exhibited *n*-type conductivity and extensively reduced the oxygen vacancies within the SnO_x films.[72,73] Figure 9a shows the schematic structure of STO films. Liu et al. reported that incorporating an appropriate concentration of Si in SnO_x effectively suppressed the carrier concentration and resulted in an STO TFT (annealed at 350°C) with better carrier mobility (8.14 cm^2/V s) and high I_{ON}/I_{OFF} ratio (6.07×10^9).[73] Ning et al. showed that the STO films exhibited a significant tensile strength which reduced crystallization, widened the optical band gap (to 4.15 eV), enhanced the electrical performance, and minimised the defects in the film. The tensile strength of the STO films is extremely dependent on the annealing

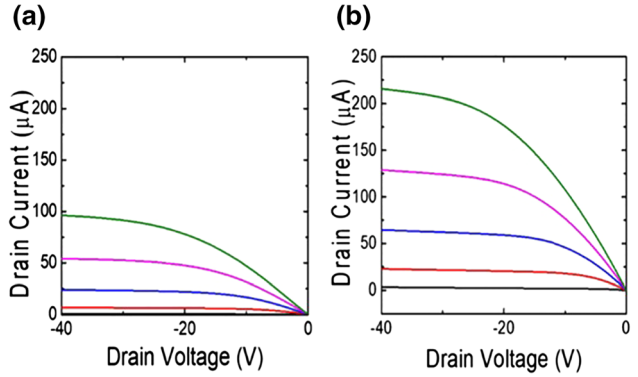

Fig. 8. Output characteristics of (a) SnO and (b) Ag-doped SnO TFTs. Reproduced with permission from,[71] Copyright 2018, American Vacuum Society.

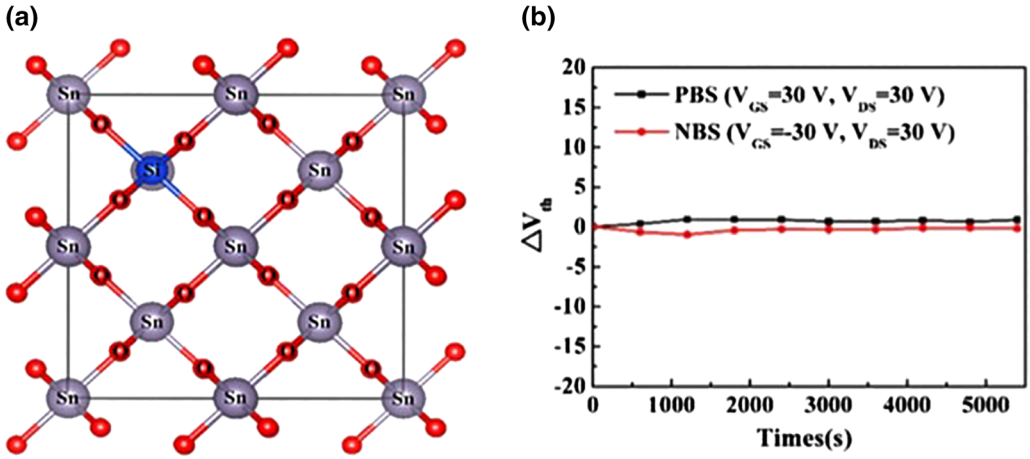

Fig. 9. (a) The schematic structure of STO films. Reprinted from[74] under the terms of the Creative Commons (CC BY 4.0) license. (b) Variations in ΔV_{th} over time (s) under PBS and NBS conditions of STO films. Reproduced with permission from,[73] Copyright 2016, IOP Publishing.

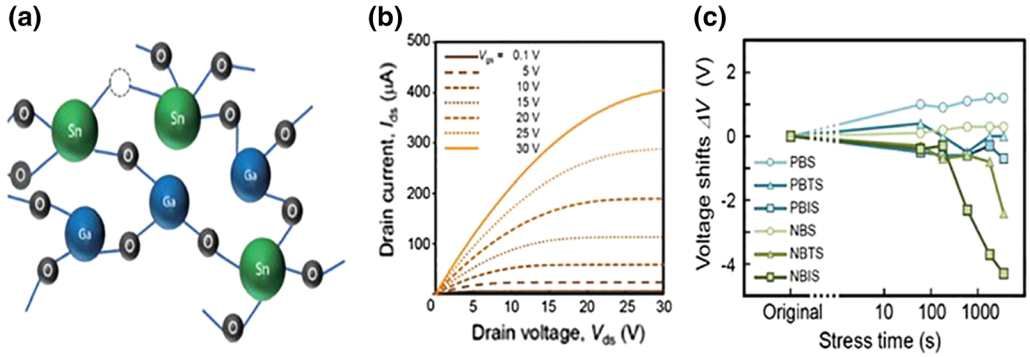

Fig. 10. (a) Schematic representations of the ionic bonding in an ideal Ga-Sn-O system. reproduced with permission from,[77] Copyright 2018, AIP Publishing. (b) Output characteristics of GTO TFT. (c) Results of various stress tests on the GTO TFT (stress conditions: PBS/PBIS = 20 V, PBTS = 20 V at 60°C, NBS/NBIS = −20 V, NBTS = −20 V at 60°C). (b, c) Reprinted from[18] under the terms of the Creative Commons (CC BY 4.0) license.

temperature.[74] Moreover, only a minimal variation in ΔV_{th} was observed in STO TFTs under PBS and NBS conditions (Fig. 9b), which indicates a very good bias stability of the device as a result of Si doping.[72,73]

(4) Ni-Sn-O

Ni doping significantly enhances the amorphous characteristics in SnO_x thin films due to the structural difference between SnO_x (rutile) and nickel oxide (face-centred cubic). In Ni-doped SnO_x (NTO) films, Ni atoms substitute the Sn atoms and compensate for the oxygen vacancy defects.[75] Since Ni atoms provide only two electrons (instead of four electrons by Sn atoms), Ni doping efficiently reduces the generation of free electrons and carrier concentration. Yang et al. reported that NTO TFTs offered low off current, better mobility (8.4 cm^2/V s), and high I_{ON}/I_{OFF} ratio (2.1×10^7). Nevertheless, the NTO TFTs showed a significant deterioration in stability under PBS and NBS conditions.[75]

(5) Ga-Sn-O

Ga-doped SnO_x (GTO) TFTs exhibited good carrier suppression by inhibiting the V_O in tin oxide, owing to the higher oxygen affinity of Ga compared to Sn.[17,18,76,77] Figure 10a shows the schematic structure of GTO films. Ga doping induces the amorphous phase formation while maintaining the structural integrity. It is noteworthy that the In^{3+} ions in IGZO and Sn^{4+} ions in GTO have the same electronic structure ($4p^6 4d^{10}$), since the 5*s* orbital serves as a path for current flow in both, which was expected to provide better electrical performance.[18,78] Matsuda et al. fabricated GTO TFTs with good carrier mobility (25.6 cm^2/V s) and I_{ON}/I_{OFF} ratio (10^8).[18]

However, Wang et al. reported the instability of GTO TFTs exhibited under NBIS and NBTS

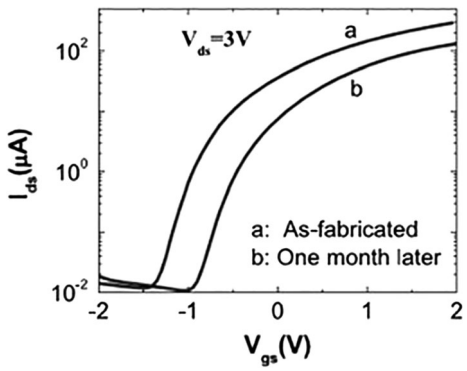

Fig. 11. The transfer characteristics (I_{ds}–V_{gs}) of the as-fabricated and 1-month-aged Sb-doped SnO_x TFT (in a semi-log graph). Reproduced with permission from,[80] Copyright 2009, IOP Publishing.

conditions (Fig. 10c) due to the charge traps at the channel-dielectric interface and the absorption of oxygen from the ambient air.[77] Recently, Ren et al. reported that the instability problems in GTO TFTs led to mobility degradation.[76] GTO TFTs fabricated at room temperature exhibited comparatively low mobility (0.48 cm^2/V s).[78] However, Ga is sensitive to the etching processes, and the reported results indicate that GTO TFTs fabricated without passivation were more prone to instability.

(6) Zr-Sn-O

Zirconium doping in SnO_x resulted in effective reduction of the deep trap states and improvement in the bias stability.[79] Han et al. indicated that incorporating Zr in SnO_x decreased the V_O and suppressed the carrier concentration as Zr promoted oxidation in SnO_x due to the higher binding energy of Zr-O (766.1 kJ/mol).[67,79] Zr-doped SnO_x TFTs exhibited low mobility (1.04 cm^2/V s); however, a fair decrease in the subthreshold swing (0.78 V/decade) and the turn-on voltage was observed.[79]

(7) Sb-Sn-O

Antimony doping improved the conductivity of the SnO_2 films, because each atom of Sb can donate one electron to the conduction band of SnO_2 as the outer shell electronic configuration of Sb and Sn are $5s^25p^3$ and $5s^25p^2$, respectively.[80,81] Sun et al. reported that Sb doping narrowed the barrier depletion region and increased the chances for electron tunnelling, resulting in an improved device performance.[80] Sabnis et al. reported that an increase in the Sb content beyond 10% resulted in non-conductivity due to the excessive impurity-induced disorders.[81] Room temperature-fabricated Sb-doped SnO_x with a 2:100 wt. ratio of Sb:Sn, which was reported by Sun et al., exhibited excellent mobility (158 cm^2/V s). They also tested the

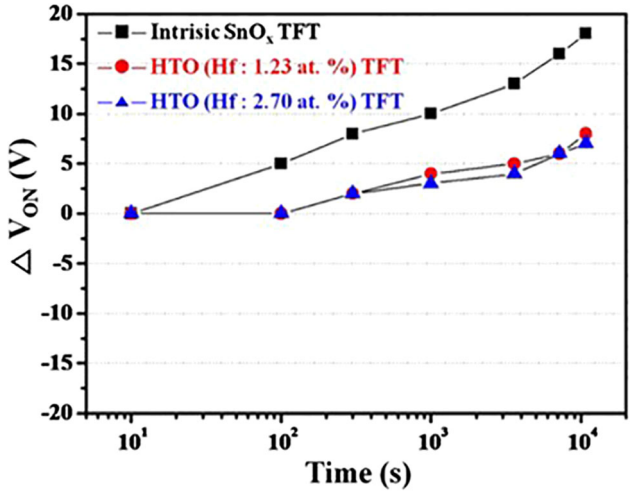

Fig. 12. Logarithmic dependence of the turn-on voltage shift (ΔV_{ON}) on the duration of gate bias stress. Reproduced with permission from,[50] Copyright 2012, Elsevier.

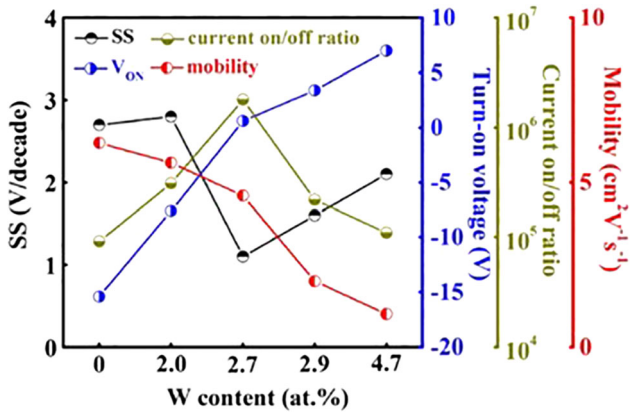

Fig. 13. Electrical characteristics of W-doped SnO_x TFT with different concentrations of the W dopant. Reproduced with permission from,[83] Copyright 2015, IOP Publishing.

impact of aging in Sb-doped SnO_x TFTs under ambient conditions, which resulted in the deterioration of their electrical performance (i.e., the carrier mobility shifted to 98.3 cm^2/V s) due to the adsorption of oxygen and water at the channel surface (Fig. 11).[80] Nevertheless, these results suggest that Sb doping is useful in the low-temperature fabrication of high-mobility SnO_x TFTs, and suitable encapsulation ensures a prolonged lifetime of the device.

(8) Hf-Sn-O

Hafnium ions are strong oxygen binders (801.7 kJ/mol), and hence V_O defects were controlled in Hf-doped SnO_x TFTs. Doping with Hf reduced the deep trap density in SnO_x as the electrons in the deep trap sites are thermally activated into the conduction band and driven

toward the electrodes by the addition of Hf in SnO_x.[50] Kim et al. and Han et al. showed that negligible ΔV_{ON} was observed in Hf-doped SnO_x TFTs compared to the intrinsic SnO_x TFTs (Fig. 12), and hence Hf plays a vital role in improving the PBS and NBTI stability of TFT by suppressing the deep trap states and total trap density.[50,82]

(9) W-Sn-O

Yang et al. reported that W doping efficiently suppressed the oxygen adsorption and increased the aging stability of SnO_x TFTs.[83] They also reported that tuning the turn-on current is possible by W doping since it reduced the S and increased I_{ON}/I_{OFF} ratio. W doping enhanced carrier suppression and inhibited crystallization. The reports indicated that W doping reduces the impurity phases in SnO_x. The doping concentration of W significantly affected the electrical properties of W-doped SnO_x TFTs (Fig. 13).[83] W-doped SnO_x TFTs displayed a comparatively low mobility (5 cm^2/V s) and I_{ON}/I_{OFF} ratio (2.4×10^6); however, a low off current and S (0.4 V/decade) were observed.[83]

(10) Bi-Sn-O

Doping bismuth was found to suppress the carrier concentration, improve the surface roughness, restrain the crystallization of SnO_x, and increases uniformity. However, the excess Bi content (> 4 wt.%) caused the mobility of Bi-doped SnO_x (BTO) TFT to deteriorate.[84] Yang et al. reported that when compared with intrinsic SnO_x TFT, BTO TFTs showed negligible variations in the PBS stability and large deterioration in the NBS stability, which can be minimized by using a suitable passivation layer. BTO TFTs with suitable Bi doping concentration (2.7 wt.%) exhibited a field effect mobility of 4.7 cm^2/V s and I_{ON}/I_{OFF} ratio of 2.3×10^6[84]

Based on these results (Table II), some points are recommended to improve the electrical performance and stability of the SnO_x TFTs. Choosing a suitable dopant plays a crucial role in solving the key issues in SnO_x TFTs such as high carrier concentration and instability under bias stress conditions. Previous reports suggest that the Lewis acid strength (L) and metal–oxygen (M–O) bonding strength are important parameters affecting the ability of the dopant to suppress the carriers by reducing the oxygen vacancy defects.[69] Dopants with large L and M–O bonding strength inhibit the ejection of oxygen atoms from the SnO_x film during the sputtering or annealing processes, leading to the effective reduction of the generation of free charge carriers from the oxygen vacancy defects.

In addition, the reported results indicate that the doping concentration plays a vital role in the electrical performance of the TFT. Particularly, in the case of dopants (Al and Ag) that induce the p-type conductivity, at dopant concentrations below the optimal value, n-type conductivity was observed irrespective of the deposition conditions. These deviations occur due to the insufficient dopant concentration in the SnO_x TFT that cannot enable holes to be the majority carriers. The electrical properties of the SnO_x TFT were also found to deteriorate when the doping content exceeded a specific ratio. Therefore, it is essential to explore the optimal doping level.

SUMMARY

A detailed review was carried out on the sputter-deposited SnO_x-based TFTs. Though SnO_x TFTs have been reported since 1964, the problems associated with the high carrier concentration and device uniformity have restricted their commercial use. However, the scarcity of indium in the earth's crust and the growing demand for high-performance TFTs resulted in the renaissance of SnO_x-based TFTs. Despite the progress in the past decades, the research on SnO_x-based TFTs still faces several problems, such as instability, grain boundary scattering, and high conductivity, that hinder the achievement of SnO_x-based TFTs with high electrical performance. This review addressed some of the approaches used to improve the stability and performance of these devices. The amorphization of SnO_x eliminates the carrier scattering and improves the uniformity of the TFTs. Sputter-deposited intrinsic a-SnO_x TFTs showed a very high mobility of μ_{FE} = 147 cm^2/V s and a high I_{ON}/I_{OFF} ratio of $> 10^7$, which evidences the opportunities of SnO_x TFTs in FPD applications and other circuit areas. The incorporation of various dopants, such as Al, Ag, Si, Ga, Ni, Zr, Hf, Sb, W, and Bi, in SnO_x TFTs and their impact on the electrical stability and mobility of the device was discussed. In particular, a low-temperature (150°C)-processed p-type Al-Sn-O_x TFT with a comparatively high mobility (2.27 cm^2/V s) and I_{ON}/I_{OFF} ratio (10^7) was competitive with other reports on p-type semiconductors. The effect of M–O bonding strength and Lewis acid strength of dopants was previously reported. This should be considered while choosing the dopants to improve the electrical performance of SnO_x TFTs. The dual-valence nature of Sn facilitates the development of both n-type and p-type active channels. The phase transition between n-type and p-type can be effectively achieved by fine tuning of the deposition parameters during sputtering. This shows the feasibility of fabricating SnO_x TFTs for CMOS applications. The limited supply and high manufacturing cost will restrict the usage of indium in the upcoming years. Since SnO_x does not suffer from these factors, SnO_x-based TFTs could significantly replace indium-based TFTs through careful consideration of the deposition parameters, selection of suitable dopants, utilization of appropriate passivation

layer, and optimizations, and would strongly impact the electronics industries.

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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