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Strained CdZnTe/CdTe Superlattices As Threading Dislocation Filters in Lattice Mismatched MBE Growth of CdTe on GaSb

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In this work, multiple sets of CdZnTe/CdTe strained-layer superlattices have been used as dislocation filtering layers for reducing the threading dislocations and improving the material quality of CdTe buffer layers grown by molecular beam epitaxy (MBE) on GaSb (211)B substrates. By incorporating a CdZnTe/CdTe superlattice filtering structure, a significant improvement in material quality has been achieved, with a low etch pit density of $\sim 1 \times 10^5$ cm^{-2} demonstrated for CdTe grown on GaSb, which is two orders of magnitude lower than previously reported values for CdTe grown directly on lattice mismatched substrates, and is comparable to values for state-of-the-art CdTe grown on lattice matched CdZnTe substrates. The filtering efficiency for each set of dislocation filtering layers has been determined to be approximately 70%. This approach provides a promising pathway towards achieving hetero-epitaxy of high quality HgCdTe on large-area lattice-mismatched alternative substrates with a low dislocation density for the fabrication of next generation infrared detectors with features of lower cost and larger array format size.

Key words: CdTe, CdZnTe, GaSb substrates, dislocation filters, etch pit density

INTRODUCTION

Recently, considerable attention has been devoted to the epitaxial growth of CdTe layers on alternative substrates such as Si,[1,2] Ge,[3,4] and GaAs,[5] to act as buffer layers for the subsequent growth of HgCdTe infrared materials and detector device structures. These studies on lattice mismatched hetero-epitaxial growth have been motivated by the potential for growing high quality HgCdTe infrared materials on large-area, cost-effective substrates for next generation HgCdTe infrared detectors and focal plane arrays (FPAs) with features of lower cost and larger array format size,[6,7] in comparison to current state-of-the-art HgCdTe infrared detectors grown on lattice matched CdZnTe substrates that are higher cost, lower crystal quality and smaller wafer size.[8] Although such an approach is attractive and presents great potential, the large lattice mismatch between (Hg)CdTe and these alternative substrates (19%, 14.3%, 14.4% and 6.1% lattice mismatch for Si, Ge, GaAs, and GaSb, respectively) inevitably generates misfit dislocations in the vicinity of the CdTe/substrate interface that form threading dislocations (TD) that propagate into the CdTe and subsequently grown HgCdTe epitaxial layers.[9,10] These defects will degrade the optical and electronic properties of the epitaxial device layers, and thus ultimately limit the detector performance and yield. Various approaches have been studied in order to reduce the TD density in CdTe and HgCdTe epitaxial layers grown on alternative substrates, including the use of a thick CdTe buffer layer, two-step growth, and various thermal annealing cycles, with significant progress being made resulting in an etch pit density (EPD) in HgCdTe of $\sim$ low-10^6 cm^{-2} to

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mid-10^6 cm^{-2}.[10] Although this EPD level is acceptable for mid-wave infrared detector fabrication, it is not suitable for long-wave infrared (LWIR) detector technologies due to the resulting high dark current.[11] Therefore, there is a strong incentive to develop new alternative substrates and new approaches in order to reduce the EPD in CdTe and HgCdTe materials to below mid-10^5 cm^{-2}, which is the upper limit for fabricating high performance LWIR HgCdTe infrared detectors.[11]

Most recently, GaSb substrates have been proposed as a new alternative to replace CdZnTe for growing high-quality HgCdTe/CdTe/GaSb.[12–14] In comparison to Si, Ge and GaAs, the mismacth in lattice constant and CTE (coefficient of thermal expansion) between HgCdTe and GaSb is much lower, which should result in a lower TD density in CdTe and HgCdTe epitaxial layers. Preliminary work has been undertaken to improve the quality of MBE grown CdTe on GaSb by inserting a nearly lattice-matched transitional Zn(Cd)Te layer between the GaSb substrate and the CdTe buffer layer,[12] which has led to an EPD of 1.4×10^5 cm^{-2} in the CdTe layer that is lower than values ranging from mid-10^5 cm^{-2} to mid-10^6 cm^{-2} reported on Si, Ge and GaAs substrates.[15,16] However, the Zn(Cd)Te transitional layer is specific to the GaSb substrate due to the unique feature that GaSb and ZnTe are nearly lattice-matched, and thus may not be applicable to the growth of CdTe on other alternative substrates. Therefore, it is essential that new TD reduction processes are developed in order to further reduce the EPD values in CdTe buffer layers grown on alternative substrates, including GaSb. Apart from reducing the generation of misfit and threading dislocations, another promising approach to reduce the EPD is to control the TD propagation direction. If the TDs propagate vertically, they will penetrate the CdTe buffer layer and result in a high EPD, whereas if the TDs propagate laterally, there will be a very low EPD at the CdTe surface. Theoretically, strained-layer superlattices can be used to deflect and control the TD propagation direction preferentially towards the growth plane, thus reducing the EPD in any overlaying epitaxial layers. Over 30 years of effort, this concept has been demonstrated successfully in the growth of III–V semiconductors on lattice mismatched substrates, in which the dislocation density was reduced from $\sim 10^9$ cm^{-2} to $\sim 10^5$ cm^{-2} for GaAs buffer layers grown on Si by incorporating InGaAs/GaAs strained-layer superlattices,[17] leading to high-performance InAs/GaAs quantum dot lasers.[18,19] Despite the five orders of magnitude decrease in dislocation density that has been claimed for a 13-μm-thick CZT buffer on GaAs(001) due to the insertion of a dislocation filtering layers (DFL) consisting of 15 periods of 250-nm-thick $Cd_{0.91}Zn_{0.09}Te$/CdTe,[20] there have been few further studies reported in the open literature, and the related superlattice-based DFL technique has yet to become commercially viable.[21–24] In this work, multiple sets of CdZnTe/CdTe superlattice-based layers have been studied as dislocation filters for reducing the TDs and thus improving the material quality of CdTe buffers grown on GaSb (211)B substrates. The demonstrated TD density of the uppermost CdTe layer has been effectively reduced from the low-10^7 cm^{-2} to the low-10^5 cm^{-2} range, and the dislocation filtering efficiency of an individual superlattice layer is estimated to be approximately 70%. This reduction in TD density is likely to be because each tensile-strained CdZnTe/CdTe superlattice layer enhances the lateral motion of TDs by applying an in-plane force, and thereby reducing the number that propagate to the uppermost CdTe layer.

EXPERIMENTAL DETAILS

CdTe buffer layers were grown on GaSb (211)B substrates (orientation angle $0° \pm 0.5°$) using a Riber 32P MBE system equipped with effusion cells of Zn, CdTe, and Te. Figure 1 shows the schematic sample structure of a CdTe buffer layer on GaSb including several sets of CdZnTe/CdTe superlattice-based DFL. In order to evaluate the in situ oxide desorption process of GaSb substrates prior to MBE growth, reflection high-energy electron diffraction (RHEED) was used to monitor the transition from a spotty RHEED pattern to a streaky pattern as the substrate temperature was raised. Oxide desorption from the GaSb substrate was undertaken by raising the substrate temperature to 520°C for 2 min without the protection of a background Sb flux. After oxide desorption, the substrates were cooled down to 280°C, and a 1850-nm-thick CdTe layer was grown at this temperature. Subsequently, four sets

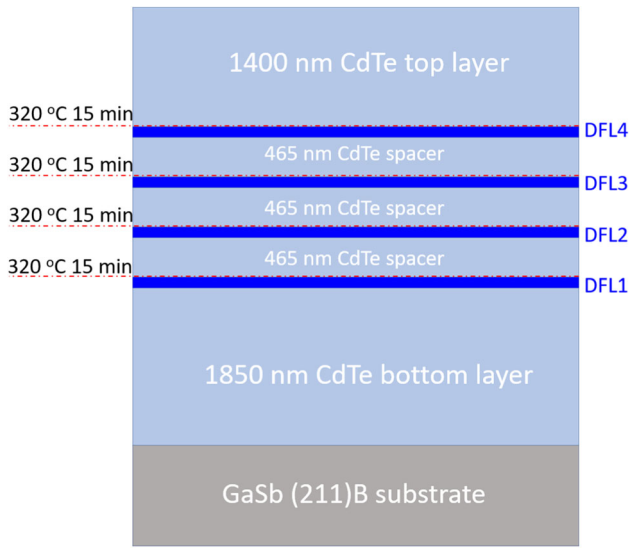

Fig. 1. Schematic sample structure for the MBE growth of a CdTe buffer layer on GaSb (211)B including several sets of strained CdZnTe/CdTe superlattice-based dislocation filtering layers (DFLs). Each DFL layer was 125 nm thick, and consisted of five periods of 12 nm $Cd_{0.85}Zn_{0.15}Te$/13 nm CdTe.

of CdZnTe/CdTe DFLs were grown at 285°C, separated by 465-nm-thick CdTe spacer layers grown at 280°C. Each set of CdZnTe/CdTe DFL consists of five periods of 12 nm CdZnTe/13 nm CdTe. In situ thermal annealing (320°C, 15 min) of each CdZnTe/CdTe DFL was also undertaken after each DFL growth in order to enhance the TD annihilation.[17] The sample growth was completed by growth a 1400 nm thick CdTe layer at 280°C. Note that the samples grown using this procedure have a total thickness of approximately 5145 nm. For comparison, a reference sample of a CdTe buffer layer with a thickness of 4900 nm was also grown at 280°C with the same CdTe and Te fluxes used for the DFL sample. A Philips X'pert MRD high-resolution X-ray diffractometer (HRXRD) equipped with a four-crystal Ge (220) monochromator was used to determine the structural parameters of the CdZnTe/CdTe DFLs, including Zn composition, thicknesses, and lattice strain. The CdTe surface morphology of the samples was evaluated using optical microscopy, atomic force microscopy (AFM), and scanning electron microscopy (SEM). The dislocation density in the samples was characterized via EPD measurements using a standard Everson etch and SEM imaging.[25]

RESULTS AND DISCUSSION

Figure 2 presents the results of HRXRD measurements on the CdTe buffer layers grown by incorporating the CdZnTe/CdTe DFLs. The strain relaxation of the CdZnTe/CdTe DFLs is determined to be less than 5% from the HRXRD reciprocal space mapping (RSM) measurements of asymmetric (333) and symmetric (422) planes, as shown in Fig. 2a and b. For the symmetric (422) RSM, the peak separation in the Q_x direction indicates the presence of lattice tilting which has been observed in numerous lattice mismatched epilayers grown on (211)-oriented substrates.[26–28] The tilt angle of the CdTe surface index deviation from (422) toward (511) around the $[0\bar{1}1]$ azimuth is calculated to be 0.8°. Figure 2c shows the HRXRD (422) ω-2θ rocking curves for the same CdTe buffer layer incorporating the CdZnTe/CdTe DFLs. The left-hand dominant peak with a full width at half maximum (FWHM) of around 120 arcsec corresponds to the CdTe layers, whereas the right-hand features consist of several interference fringes corresponding to the CdZnTe/CdTe DFLs, indicating that sharp CdZnTe/CdTe interfaces have been achieved. By fitting the experimental rocking curve data, the x value and thicknesses of the $Cd_{1-x}Zn_xTe$/CdTe layers were determined to be 0.15 and 12 nm/13 nm, respectively. It must be noted that in each set of DFL the thickness of the $Cd_{0.85}Zn_{0.15}Te$ layers, which have a 0.9% lattice mismatch to CdTe, was designed to be below the theoretical critical thickness of 28 nm in order to avoid lattice relaxation and the concomitant generation of new misfit dislocations and TDs.[29] In addition, the XRD FWHM for the 4900 nm thick CdTe reference sample was measured to be 116 arcsec, which is close to that of the CdTe sample that includes the DFLs. This suggests that any improvement in material quality of the CdTe buffer layer after introducing the DFLs used in this study cannot be evaluated by using the XRD FWHM values only, which is likely to be because the XRD FWHM of both samples is dominated by the quality of the initial CdTe grown directly on the GaSb substrate and before introducing the DFLs. Note that the XRD peak of the GaSb substrate is evident in Fig. 2, indicating that the XRD measurement samples the entire epitaxial layer as well as the GaSb substrate. In addition, the interference fringes from the DFLs also increase the XRD FWHM value. Despite the fact that similar growth conditions have been used, it should be noted that the XRD FWHM values found in this study are broader than those reported previously for MBE grown CdTe buffer layers on GaSb substrates without DFL ($\sim$ 70 arcsec). [6,7] This may be the result of enhanced oxide formation on the GaSb substrate surface due to long-time storage of the GaSb substrates used in this study, thus affecting the desorption efficiency of natural oxide on GaSb substrates and thus the resultant crystal quality of the grown CdTe layers.

Apart from XRD measurements, RHEED and AFM were also utilised to characterise and evaluate the MBE growth and material quality of the CdTe buffer layers, both with and without the incorporation of DFL. As evident from Fig. 3a and d, the spotty-like RHEED patterns during the MBE growth of the CdTe become streaky-like with the incorporation of CdZnTe/CdTe DFLs, indicating an improvement in material quality. Correspondingly, as shown in the AFM images in Fig. 3b and e the dark pit-like surface defects which are likely to have originated from the lattice mismatch and nonideal oxide desorption of the GaSb are significantly reduced in the presence of DFLs. The root mean squared (RMS) surface roughness of the uppermost CdTe layer including DFLs is measured to be 1.7 nm, which is significantly lower than the 3.8 nm measured on the CdTe-only reference sample. To evaluate the effect of the DFLs on the TD density of the CdTe grown, EPD measurements were undertaken by using a 60 s Everson etch on both types of samples, corresponding to a CdTe etch depth of less than 1.4 μm. From the SEM images shown in Fig. 3c and f, the EPD for the uppermost CdTe with DFLs was measured to be $\sim 1 \times 10^5$ cm^{-2}, which is approximately two orders of magnitude lower than that of the single-layer CdTe reference sample, with an EPD of $\sim 2 \times 10^7$ cm^{-2}. As discussed previously, this result can be attributed to the dislocation filtering effect of the strained CdZnTe/CdTe superlattice layers. In order to assess the filtering efficiency of individual CdZnTe/CdTe DFL, the sample with multiple DFLs

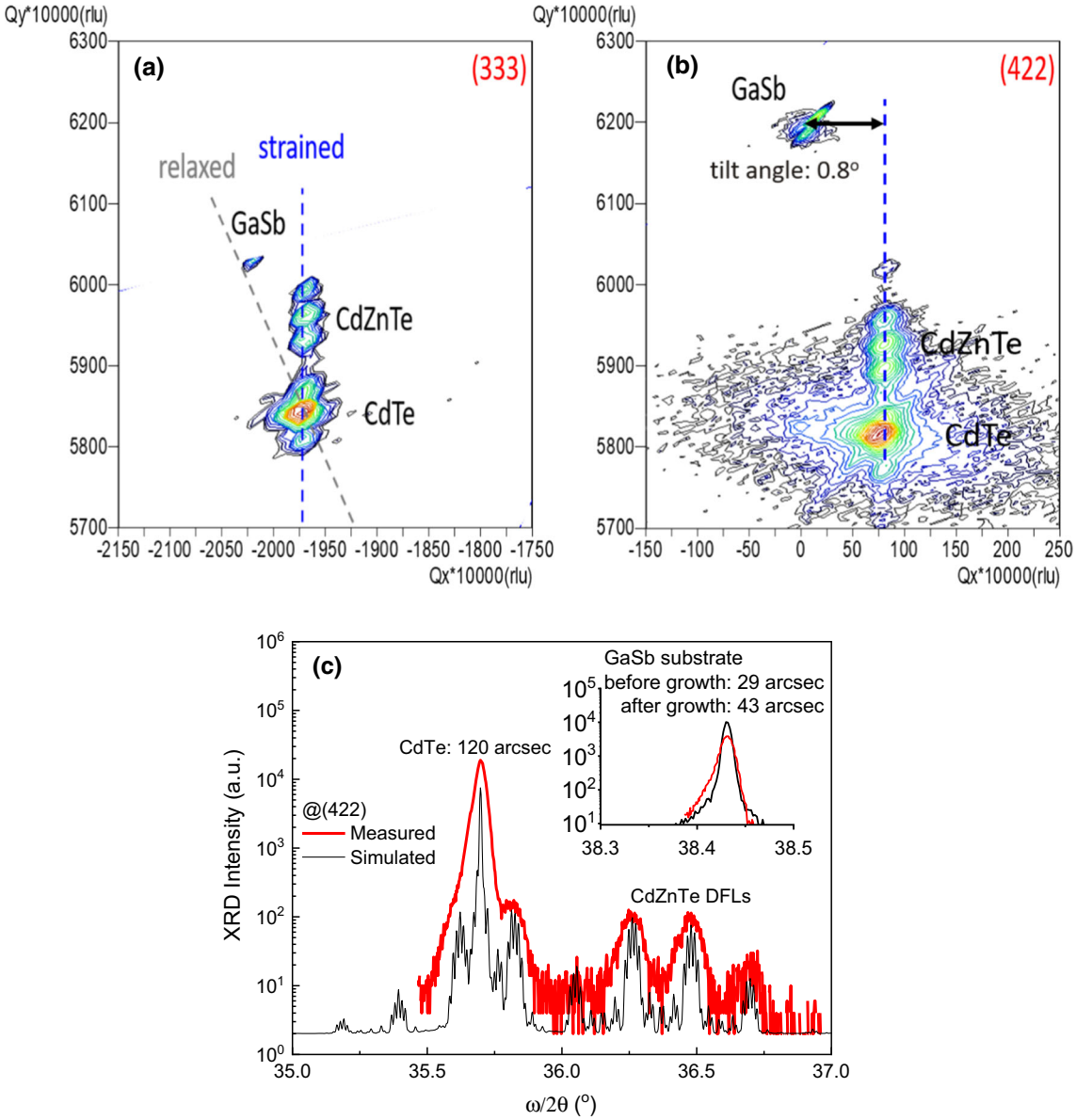

Fig. 2. HRXRD RSM maps for the (333) plane (a) and (422) plane (b) of the CdTe buffer layer grown on a GaSb (211)B substrate and incorporating the CdZnTe/CdTe superlattice layers as shown in Fig. 1. The vertical line represents reciprocal lattice points where the parallel lattice constant of the CdZnTe superlattice is equal to that of the CdTe layers: that is, a fully strained superlattice; (c) HRXRD (ω-2θ) measurements for the (422) plane of the CdTe buffer layer and the GaSb substrate (the inset).

was etched down to different depths, and SEM imaging was undertaken to determine the EPD values within the individual CdTe layers. Firstly, the sample was etched to a depth of approximately 2.6 μm using a 2 min etching time within a photoresist-free area. The etched surface thus corresponds to the mid-region of the CdTe layer (near the upper interface of the DFL2/CdTe) and is labelled "B" in the schematic sample structure shown in Fig. 4a. Figure 4c shows a representative magnified SEM image of surface "B", indicating that there are three main types of etch pit: (i) conventional triangular etch pits that originate from TDs that penetrate through the DFL region; (ii) quasi-etch pits that contribute the majority of pits, and are expected to have originated from TDs that have been diverted by the DFL layer and/or due to self-annihilation; and (iii) a small number of large area (3–5 μm diameter) TD clusters, which are likely to be caused by the non-ideal thermal desorption of oxides from the GaSb substrate surface prior to MBE growth, and penetrate through the entire buffer layer since they can be observed by optical microscopy before EPD etching. The total EPD is determined to be $\sim 5 \times 10^5$ cm^{-2} for surface "B", which is calculated by averaging the pit counts over five large-area SEM images.

After evaluating the EPD of surface "B" within the middle CdTe layer, the photoresist used for the first etch was removed, and both the unetched area

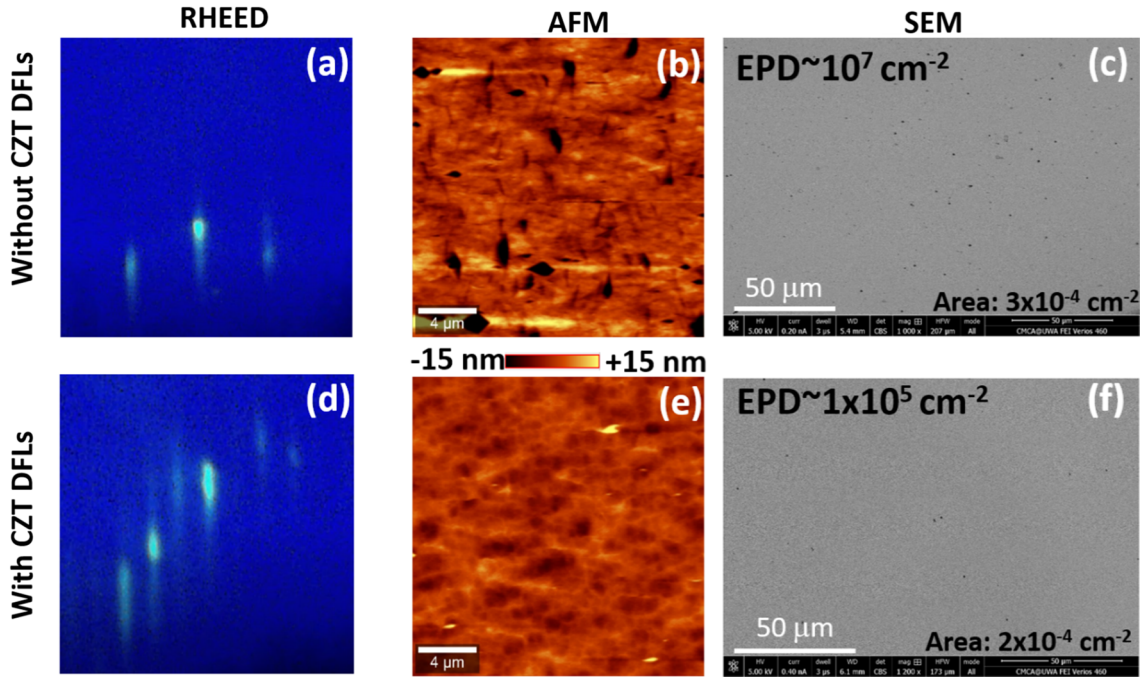

Fig. 3. RHEED patterns during MBE growth, AFM images, SEM images for EPD measurements of the uppermost CdTe surface. (a), (b) and (c) are for a 4900-nm-thick single CdTe layer, and (d), (e) and (f) are for a 5145-nm-thick CdTe buffer layer that includes the CdZnTe/CdTe DFLs.

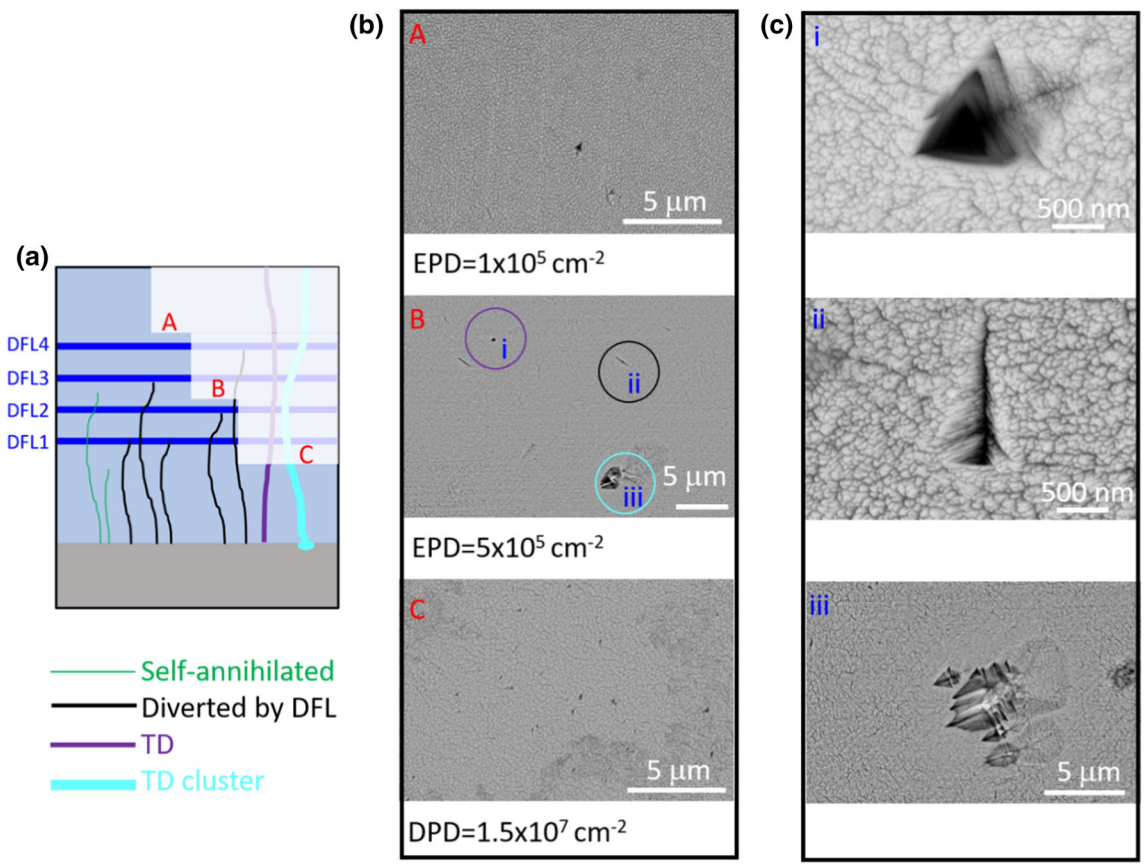

Fig. 4. (a) Schematic diagram of the CdTe buffer layer including four DFL structures used for EPD measurements at different etch depths within layers A, B, and C; (b) Representative SEM images of surfaces A, B and C after EPD etching; (c) magnified images of three different types of etch pits observed in the image "B" of (b).

and etched area were etched for a period of 60 s. This leads to the exposure of two etched surfaces with depths of 1.4 μm and 4.0 μm, which correspond to positions in the uppermost CdTe layer above the DFL region and a position in the bottom CdTe layer below the DFL region, and are labelled "A" and "C" in Fig. 4a, respectively. Figure 4b present the representative SEM images of surfaces "A" and "C", respectively, and similar types of etch pits are evident. The EPD of CdTe surface "A" (above the DFL region) is determined to be $\sim 1 \times 10^5$ cm^{-2}, while that of surface "C" (below the DFL region) is determined to be as high $\sim 1.5 \times 10^7$ cm^{-2}. In principle, the density of TD should reduce somewhat with increasing thickness of a single-layer CdTe buffer due to self-annihilation. However the efficiency of such a self-annihilation process is relatively low, and no significant EPD reduction with thickness is observed in the reference CdTe sample without incorporating DFLs. This suggests that the DFLs incorporated within the CdTe buffer layer act as effective filters for reducing the propagation of TDs to the uppermost CdTe layer. As indicated in Fig. 5a, the changes in EPD values by incorporating different sets of DFLs can be experimentally fitted by a power relationship: $\rho = \rho_0(1-\eta)^N$, where ρ is the EPD value of the CdTe layer after incorporating a certain number of DFLs, ρ_0 is the initial EPD of the bottom CdTe layer, N is the number of DFLs, and η is the filtering efficiency. The filtering efficiency η of each DFL can be determined to be $\sim 70\%$. These results are very promising, since they suggest that even lower EPD values can be achieved by further optimising the structural parameters of the DFL to increase the filtering efficiency, improving the structural parameters of the DFL and the growth conditions of the epitaxial layers through better thermal cleaning of the GaSb substrate surface, and/or by increasing the number of DFLs within the buffer layer.

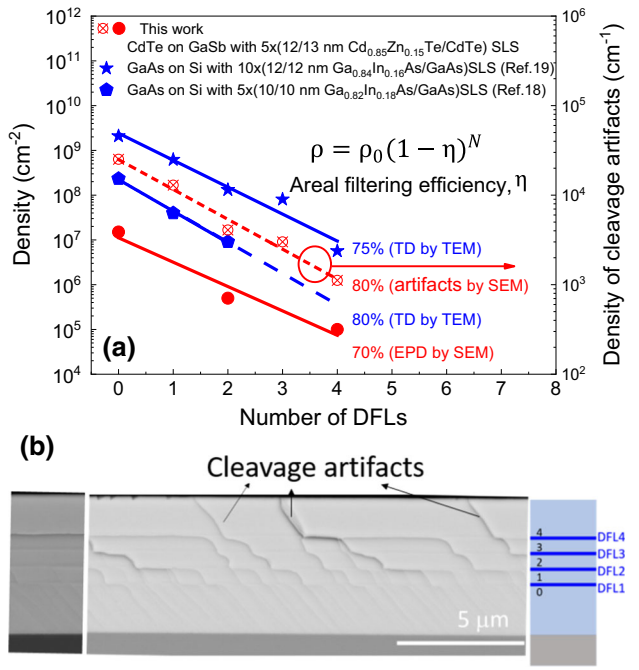

Fig. 5. (a) Dependence of defect density on the number of DFLs; (b) cross-sectional SEM image of the cleaved CdTe buffer layer with DFLs. The left side image with an optimal brightness/contrast shows visible interfaces between the DFLs and CdTe layers. Some cleavage artifacts extend all the way from the CdTe/GaSb interface to the top CdTe surface as indicates by arrows.

Apart from EPD measurements, another approach for studying the evolution of TDs is to undertake cross-sectional transmission electron microscopy (TEM) to evaluate the density of TDs, which has been reported previously for group III–V and IV semiconductors. Figure 5a also includes the evolution of TD density within GaAs buffer layers grown on Si after incorporating strained III–V GaInAs/GaAs superlattice DFLs as observed by TEM.[18,19] Although the absolute values of TD density are not directly comparable, the dislocation filtering efficiency can be deduced to be 80% for the two-sets-of-ten-period $In_{0.16}Ga_{0.84}As/GaAs$ (12 nm/12 nm) SLSs, and $\sim 75\%$ for the four-sets-of-five-period $In_{0.18}Ga_{0.82}As/GaAs$ (10 nm/10 nm) SLSs,[18,19] which are comparable to the $\sim 70\%$ dislocation filtering efficiency found in this study for the II–VI CdZnTe/CdTe superlattice DFLs.

In comparison to other semiconductors, TEM specimen preparation of CdTe and HgCdTe structures for TEM imaging is very challenging due to the fragile nature of the material. Instead of TEM, cross-sectional SEM imaging was undertaken in an attempt to observe the filtering effect of the CdZnTe/CdTe DFLs. Figure 5b presents a representative cross-sectional SEM image of a cleaved CdTe buffer layer with CdZnTe DFLs. The clear and sharp interfaces between the DFLs and the surrounding CdTe can be observed. Besides, the visible features on the cross-sectional surface are presumably cleavage artifacts, and it is noted the DFLs appear to act as barriers to the propagation of these artifacts. In principle, the cleavage proceeds from the backside of the substrate, and thus any cleavage artifacts should extend all the way from the CdTe/GaSb interface to the top CdTe surface as indicated by arrows in Fig. 5b. However, as shown in Fig. 5b, the number of cleavage artifacts appear to reduce after each DFL, and Fig. 5a presents the evolution of the artifact line density within the CdTe layer after each DFL, which can be experimentally fitted by a power relationship: $\rho_l = \rho_{l0}(1-\eta_l)^N$, where ρ_{l0} is the initial artifact line density of the bottom CdTe layer, N is the number of DFLs, and η_l represents the artifact line density filtering efficiency which is deduced to be $\sim 55\%$. The areal density filtering efficiency (η_a) for the growth plane can be calculated to be $\sim 80\%$ assuming $(1-\eta_a) = (1-\eta_l)^2$, which is similar to the value of EPD filtering efficiency obtained above, and to that of InGaAs/GaAs DFLs observed with TEM. Although the precise

relationship between TDs and the cleavage artifacts is not clear at this stage, it is possible that the artifacts originate from pre-existing crystalline defects during the cleavage process, and thus a higher TD density leads to a higher density of artifacts. This is analogous to the correlation between EPD and TD density, and suggests that the density of cleavage artifacts on the cross-sectional surface may be a useful monitor for characterising the evolution of TDs.

SUMMARY AND CONCLUSIONS

In summary, this study has demonstrated a dramatic improvement in material quality and corresponding EPD of CdTe buffer layers grown on lattice-mismatched GaSb (211)B substrates as a direct result of incorporating tensile-strained CdZnTe/CdTe superlattice-based DFLs. The CdZnTe/CdTe DFLs present a high dislocation filtering efficiency of $\sim 70\%$ for each individual layer. Using four individual DFLs, the resultant EPD in the uppermost CdTe layer is demonstrated to approach that of state-of-the-art CdZnTe substrates, thus promising a suitable pathway forwards growing LWIR HgCdTe on large-area substrates. More importantly, these results suggest that the beneficial effects of CdZnTe/CdTe DFLs is not limited to GaSb substrates, but may be applied to the growth of CdTe buffer layers on other alternative substrates such as Si, Ge and GaAs. Therefore, this work provides a feasible approach for growing high quality CdTe and HgCdTe materials on large-area alternative substrates for fabricating next generation HgCdTe infrared detectors and imaging FPAs with features of lower cost and larger array format size.

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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