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Investigation of Double-Gate Ferroelectric FET Based on Single-Layer MoS_2 with Consideration of Contact Resistance

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A ferroelectric field-effect transistor (Fe-FET) with two-dimensional MoS_2 as the channel material with and without contact resistance is explored and compared. A top-of-the-barrier model along with the ferroelectric model is used to investigate the device performance. The contact resistance can strongly affect the current–voltage characteristic. The Fe-FET with contact resistance requires a higher voltage to reach saturation. Increasing the ferroelectric thickness to a specified value decreases the output resistance, but further increase can compensate this, resulting in high output resistance. Increasing the ferroelectric thickness decreases the mean subthreshold swing in the upward and downward regime. This effect is greater for the downward regime, and the contact resistance can intensify it.

Key words: Transition-metal dichalcogenide, TMD, double-gate field-effect transistor, ferroelectric, Fe-FET, subthreshold swing

INTRODUCTION

Two-dimensional (2D) materials have attracted great attention as channel materials for future nanoscale electronics due to their perfect interfaces and lack of dangling bonds. Such 2D semiconductors have been proposed as channel materials for field-effect transistor (FET) devices.[1,2] Their single atom thickness maximizes the gate control over the channel potential, overcoming problems that occur in conventional FETs with short channel length.[3,4] One prototype of such 2D materials, viz. the transition-metal dichalcogenide (TMD) family, shows a wide range of electrical properties. Single-layer TMD materials have already shown good potential for use in nanoelectronic applications as an alternative to silicon.[5,6] Owing to their single atom thickness without dangling surface bonds, two-dimensional TMD devices can be scaled down further than Si-based transistors and show reduced short-channel effects.[7]

TMDs have a sizable electronic bandgap in the single layer, making such materials interesting for application as channel materials in next-generation 2D electronics.[8] Epitaxial growth of semiconducting TMDs has allowed progress towards very large-scale integration.[9,10] Several research groups have fabricated FETs using different TMD materials as MoS_2,[11–13] MoS_2,[14] $MoTe_2$,[15] WS_2,[16] and WSe_2.[17] In particular, MoS_2 has been widely studied in recent years as a promising channel material because of its ambient stability, appropriate bandgap, and moderate mobility.[5,7,18]

The good modulation of the gate voltage on an ultrathin body of MoS_2 allows the channel length of MoS_2 transistors to be scaled down to below 10 nm. The high effective mass, low dielectric constant, and large bandgap of MoS_2 minimize direct source–drain tunneling, while its ultrathin body enables better modulation of the gate voltage in short-channel transistors.[7,19] Nourbakhsh et al.[19] demonstrated an MoS_2 FET with a channel length of

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7.5 nm and a low off-current of 10 pA/μm, on/off current ratio of $>10^7$, and subthreshold swing (SS) of 120 mV/dec. The off-current and on/off current ratio are good results, whereas the SS is greater than in today's Si-based metal–oxide–semiconductor field-effect transistors (MOSFETs). The effects of contact resistance on the direct-current (DC) performance of FETs have been investigated, revealing that it limits the on-current and also increases the saturation voltage.[20]

The addition of a ferroelectric insulator to the gate oxide of a field-effect transistor has been widely explored, resulting in the ferroelectric field-effect transistor (Fe-FET). The Fe-FET has been suggested for nonvolatile memory and low-power logic applications. Ferroelectric insulators show negative capacitance, which can result in better control over the channel potential by the gate voltage. This negative capacitance also reduces the subthreshold swing to below 60 mV/dec, as reported for Fe-FETs.[6,15] This is achieved by including a layer of ferroelectric material in the gate oxide.[14,15] Such ferroelectric materials range from lead zirconium titanate (PZT) to complementary metal–oxide–semiconductor (CMOS)-compatible doped HfO_2.

The development of the CMOS-compatible zirconium-doped hafnium oxide (HZO) ferroelectric has enabled tremendous progress of Fe-FETs.[21,22] Zr-doped hafnium oxide films are ferroelectric oxides that can be grown using atomic layer deposition (ALD).[23,24] Zr-doped HfO_2 films exhibit the largest remanent polarization when the Hf:Zr ratio is 1:1.[25]

Fe-FETs with negative capacitance are very interesting for use in low-power electronic applications, whereas Si-based devices are rapidly approaching their physical limits.[26] The use of a 2D material in a conventional three-dimensional (3D) channel can also enhance the device performance by increasing the surface area to volume ratio, which results in a higher negative capacitance effect.[27] The combination of ferroelectric insulators and 2D materials has been reported in Fe-FETs[28–30] and negative-capacitance (NC)-FETs,[31–33] combining the benefits of both 2D semiconductors and the ferroelectric properties.

A tremendous improvement in the subthreshold swing has been reported for the Fe-FET compared with a FET using the same $MoSMoS_2$ channel.[34] Indeed, the subthreshold swing is approximately decreased by more than one order of magnitude in a 2D-FET with a ferroelectric oxide (SS = 8.5 mV/dec) compared with a 2D-FET (SS = 161 mV/dec) with conventional oxide.

A Fe-FET with single-layer MoS_2 as the channel material is studied herein. In "Methods" section, the methodology of the drain current calculation is discussed. The effects of the contact resistance on the voltage–current characteristic are investigated, as well as the performance of a modified Fe-FET with a ferroelectric layer in the oxide gate. These results are presented in "Result" section. Finally, concluding remarks are presented in "Conclusions" section.

METHODS

A schematic of the double-gate Fe-FET is shown in Fig. 1, where single-layer MoS_2 is used as the channel material. A metal–ferroelectric–metal–insulator (MFMI) structure is used for both sides of the channel. HfO_2 is used as the gate insulator, and the ferroelectric can be selected from among various materials.

The channel length of the FET is assumed to be 8 nm, namely smaller than the carrier mean free path of single-layer MoS_2.[35] We thus use a top-of-the-barrier model, that is, a ballistic analytical model, including a ferroelectric model to calculate the drain current of the Fe-FET. In the top-of-the-barrier model, the nonequilibrium and equilibrium electron densities are calculated using the density of states. The lowest and second lowest minimum in the conduction band of single-layer MoS_2 are the K and Q valley, respectively. The effective mass of the K valley is 0.47 m_0. The longitudinal and transverse effective mass of the Q valley are $1.14m_0$ and $0.54m_0$, respectively. The energy difference between these valleys is 195 meV.[8] Using the electron density value, the self-consistent potential at the top of the barrier along the channel is calculated. To determine the exact value of the carrier density and the self-consistent potential, they are calculated iteratively at the top of the barrier. The drain current density is calculated by differencing the fluxes from the source and drain contacts.

The metal contacts to the source and drain in the transition-metal dichalcogenide (TMDC) channel induce a contact resistance that strongly affects the performance of the FET and that is modeled as a resistance in series with the intrinsic resistance. Different values for the contact resistance are reported.[39–43] Here, we consider $R_C = 7.5 \times 10^{-5}$ Ω, which is the smallest reported value, because higher contact resistance degrades the performance.[19]

To consider the effects of the ferroelectric layer, the following equation can be used:

$$V_G = V_{IM} + V_{FE}, \quad (1)$$

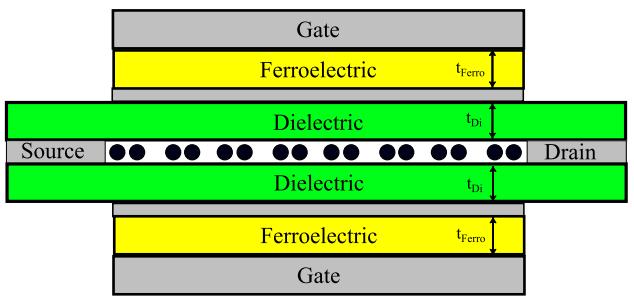

Fig. 1. Schematic of double-gate FET with single-layer MoS_2 as channel material using a metal–ferroelectric–metal–insulator (MFMI) structure for both gates.

Table I. Landau expansion coefficients of different materials

Material	α (m F^{-1})	β (m^2 F^{-1} C^{-2})	γ (m^9 F^{-1} C^{-4})	Ref.
HZO	-4.6×10^8	-1.3×10^8	9.9×10^{10}	36
BTO	-1×10^7	-8.9×10^8	4.5×10^{10}	37
PZT	-4.5×10^7	5.2×10^8	5.9×10^8	38

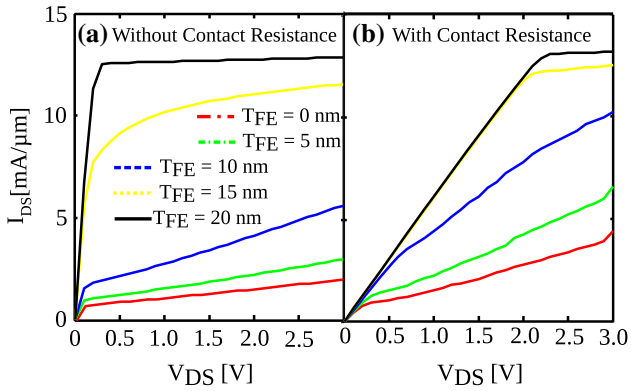

Fig. 2. Drain current as function of drain–source voltage for different ferroelectric thicknesses (a) without and (b) with contact resistance. V_{GS} = 0.8 V and contact resistance is 7.5×10^{-5} Ω m.

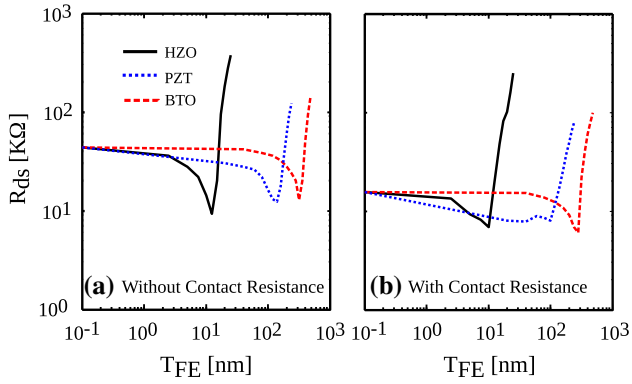

Fig. 3. Output resistance as function of ferroelectric thickness (a) without and (b) with contact resistance.

where V_G and V_{IM} are the gate voltage and internal metal voltage, respectively. V_{FE} is a ferroelectric voltage that can be calculated from the Landau–Khalatnikov equation as follows:[44]

$$V_{FE} = E_{FE} T_{FE}, \tag{2}$$

where T_{FE} is ferroelectric thickness and E_{FE} is:

$$E_{FE} = 2\alpha P_{FE} + 4\beta P_{FE}^3 + 6\gamma P_{FE}^5 + \rho \mathrm{d}P_{FE}/\mathrm{d}t, \tag{3}$$

with α, β, γ , and ρ being the ferroelectric material parameters. ρ represents the damping in the ferroelectric material and is neglected in the static analysis considered herein. Table I presents some common ferroelectrics and their parameters. Besides, P_{FE} is calculated as

$$P_{FE} = Q_{FE} - \epsilon_0 E_{FE} \approx Q_{FE}, \tag{4}$$

where Q_{FE} is the charge of the ferroelectric, which is $-qN_{eq}$, where N_{eq} is the obtained equilibrium electron density and q is the elementary charge. The top and back dielectric are 5-nm HfO_2 with dielectric constant of 23.[45]

RESULTS

Assuming a HZO ferroelectric layer, the drain current versus V_{DS} for different ferroelectric thicknesses is plotted in Fig. 2a and b without and with consideration of contact resistance, respectively. The drain current of the Fe-FET increases when using a ferroelectric layer in comparison with the conventional FET.

As seen from these results, in the case without contact resistance, I_{DS} saturates for about V_{DS} = 0.2 V with V_{GS} = 0.8V. However, a higher voltage is needed to saturate the drain current with contact resistance, because of the voltage dropped across the contact resistance. This saturation voltage is about 2 V when the contact resistance is about $R_C = 7.5 \times 10^{-5}$ Ω and the ferroelectric thickness is 20 nm.

After saturation, I_{DS} slowly increases with increasing V_{DS} due to the effects of the drain–source voltage on the channel potential via short-channel effects. One may expect the slope of the curve to increase as the channel length is shrunk, but when using a thick ferroelectric layer in the gate oxide, the slope of I_{DS} in the saturation regime decreases, resulting in the increasing output resistance. The output resistance is defined as the drain–source resistance in the saturation regime.

The output resistance of the Fe-FET with different ferroelectric materials reported in Table I is plotted in Fig. 3 as a function of the ferroelectric thickness. It is assumed that the contact resistance and channel width are 7.5×10^{-5} Ω and 50 nm, respectively. As seen from this figure, the use of 25-nm HZO as the ferroelectric layer increases the output resistance from 44 kΩ to 378 kΩ and from 16 kΩ to 250 kΩ for the cases without and with contact resistance, respectively. Because of the smaller ferroelectric parameters of BTO and PZT (Table I), they should be used with higher thickness. As seen from Fig. 3, the use of 240-nm PZT as the

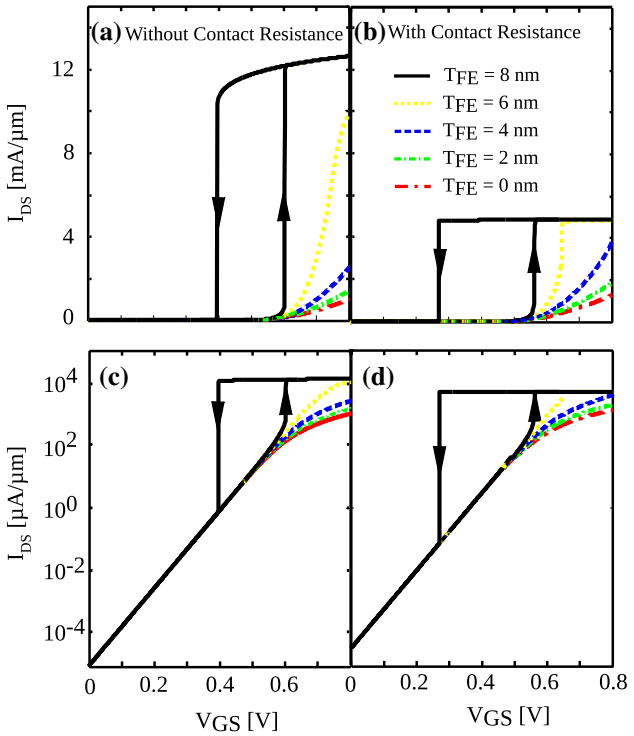

Fig. 4. I_{DS} plotted on a linear scale (a, b) or logarithmic scale (c, d) versus gate–source voltage for different ferroelectric thicknesses (a, c) without and (b, d) with contact resistance. V_{DS} is equal to 0.8 V, and the contact resistance is 7.5×10^{-5} Ω.

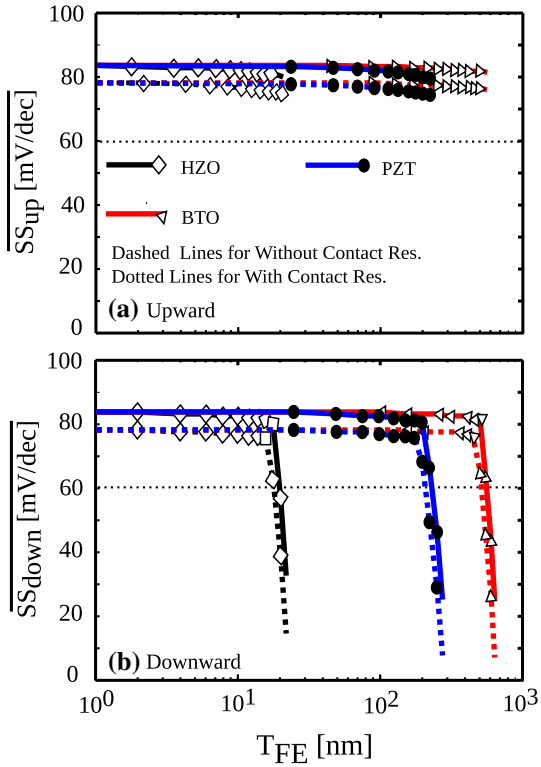

Fig. 5. Subthreshold slope for different materials as a function of ferroelectric thickness for (a) upward and (b) downward regime. Dashed and dotted lines indicate results without and with contact resistance, respectively. V_{DS} is equal to 0.8 V, and contact resistance is 7.5×10^{-5} Ω.

ferroelectric layer increases the output resistance from 44 kΩ to 124 kΩ.

Fixing V_{DS} at 0.8 V, the drain current versus gate voltage for different ferroelectric thicknesses is plotted in Fig. 4. HZO has been used as a ferroelectric layer. In the conventional FET (without a ferroelectric layer), no hysteresis is observed, whereas hysteresis is created and increases with increasing ferroelectric thickness. The creation of such hysteresis in the current–voltage characteristic of a Fe-FET has been reported in some literature reports.[46,47]

Note that the assumed contact resistance (7.5×10^{-5} Ω) limits the maximum on-current of the FET to below 5300 V_{DS}A/μm, i.e., $V_{DS}/2R_C$. As can be seen from this figure, assuming this contact resistance, the hysteresis of the drain current increases. As seen in Fig. 4, the subthreshold slope (SS) of the Fe-FET is dependent on the drain current and ferroelectric layer, creating a steep swing in I_{DS} versus the gate voltage. The mean subthreshold swing for both the upward and downward regimes ($\overline{SS_{up}}$ and $\overline{SS_{down}}$) can be calculated as

$$\overline{SS} = \frac{V_{GS,on} - V_{GS,off}}{\log_{10}(I_{DS,on}) - \log_{10}(I_{DS,off})}, \quad (5)$$

where $I_{DS,on}$ and $I_{DS,off}$ are the on- and off-current. The off-current is considered for $V_{GS,off} = 0$, while the on-current is defined as 10^2 μA/μm. $\overline{SS_{up}}$ and $\overline{SS_{down}}$ are calculated for the different ferroelectrics as a function of their thickness, and the results are plotted in Fig. 5. One can see that $\overline{SS_{up}}$ and $\overline{SS_{down}}$ decrease with increasing ferroelectric thickness, which is due to the negative capacitance of the ferroelectric layer.[47,48] This effect is drastic for $\overline{SS_{down}}$. The contact resistance decreases $\overline{SS_{up}}$ and $\overline{SS_{down}}$, and this effect becomes higher for a thicker ferroelectric layer. While the $\overline{SS_{up}}$ of the FET without a ferroelectric layer is 78 mV/dec, the use of 22-nm HZO as the ferroelectric layer decreases it to 74 mV/dec with consideration of contact resistance. The effect of the ferroelectric layer is approximately independent of the contact resistance. On the other hand, the $\overline{SS_{down}}$ for this Fe-FET is about 31 mV/dec and 13 mV/dec without and with contact resistance, respectively.

Note that there is a limitation on increasing the ferroelectric layer due to the creation of hysteresis in the drain current; For example, when using more than 25 nm of HZO as the ferroelectric layer, the step swing of the drain current in the downward regime occurs at negative gate–source voltage, meaning that such a Fe-FET cannot turn off with zero gate–source voltage.

CONCLUSIONS

A ferroelectric FET (Fe-FET) with single-layer MoS_2 as the channel is investigated. The DC performance with and without contact resistance is compared using a top-of-the-barrier model along with the ferroelectric model. The contact resistance can strongly affect the current–voltage characteristic. The Fe-FET with contact resistance requires a higher drain–source voltage to reach saturation. Increasing the ferroelectric thickness to a specified value decreases the output resistance, but a further increase in the ferroelectric thickness can compensate this and result in high output resistance. Increasing the ferroelectric thickness decreases the mean subthreshold swing in the upward and downward regimes. This effect is greater for the downward regime, and the contact resistance can intensify it.

REFERENCES

1. K. Novoselov, D. Jiang, F. Schedin, T. Booth, V. Khotkevich, S. Morozov, A. Geim, Proc. Natl. Acad. Sci. 102(30), 10451 (2005).
2. V. Podzorov, M. Gershenson, C. Kloc, R. Zeis, E. Bucher, Appl. Phys. Lett. 84(17), 3301 (2004).
3. Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, C. Hu, in *International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)*, pp. 919 (1999).
4. T. Skotnicki, J.A. Hutchby, T.J. King, H.S.P. Wong, F. Beouff, IEEE Circuits Devices Mag.
5. B. Radisavljevic, A. Radenovic, J. Brivio, i.V. Giacometti, A. Kis, Nat. Nanotechnol. **6**(3), 147 (2011).
6. I. Popov, G. Seifert, D. Tománek, Phys. Rev. Lett. 108(15), 156802 (2012).
7. S.B. Desai, S.R. Madhvapathy, A.B. Sachid, J.P. Llinas, Q. Wang, G.H. Ahn, G. Pitner, M.J. Kim, J. Bokor, C. Hu, H.S.P. Wong, A. Javey, Science 354(6308), 99 (2016).
8. M. Hosseini, M. Elahi, M. Pourfath, D. Esseni, IEEE Transactions on Electron Devices 62(10), 3192 (2015).
9. Q. Ji, Y. Zhang, T. Gao, Y. Zhang, D. Ma, M. Liu, Y. Chen, X. Qiao, P.H. Tan, M. Kan, J. Feng, Q. Sun, Z. Liu, Nano Letters 13(8), 3870 (2013).
10. A. Roy, H.C. Movva, B. Satpati, K. Kim, R. Dey, A. Rai, T. Pramanik, S. Guchhait, E. Tutuc, S.K. Banerjee, ACS Appl. Mater. Interfaces 8(11), 7396 (2016).
11. H. Qiu, L. Pan, Z. Yao, J. Li, Y. Shi, X. Wang, Appl. Phys. Lett. 100(12), 123104 (2012).
12. K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.Y. Kim, W.K. Hong, S. Hong, T. Lee, ACS nano 7(9), 7751 (2013).
13. Y.Y. Illarionov, G. Rzepa, M. Waltl, T. Knobloch, A. Grill, M.M. Furchi, T. Mueller, T. Grasser, 2D Mater. **3**(3), 035004 (2016).
14. S.R. Das, J. Kwon, A. Prakash, C.J. Delker, S. Das, D.B. Janes, Appl. Phys. Lett. 106(8), 083507 (2015).
15. Y.F. Lin, Y. Xu, S.T. Wang, S.L. Li, M. Yamamoto, A. Aparecido-Ferreira, W. Li, H. Sun, S. Nakaharai, W.B. Jian, K. Ueno, K. Tsukagoshi, Advanced Materials 26(20), 3263 (2014).
16. W. Sik Hwang, M. Remskar, R. Yan, V. Protasenko, K. Tahy, S. Doo Chae, P. Zhao, A. Konar, H. (Grace) Xing, A. Seabaugh, D. Jena, Applied Physics Letters **101**(1), 013107 (2012).
17. H. Fang, S. Chuang, T.C. Chang, K. Takei, T. Takahashi, A. Javey, Nano Lett. 12(7), 3788 (2012).
18. H. Wang, L. Yu, Y.H. Lee, Y. Shi, A. Hsu, M.L. Chin, L.J. Li, M. Dubey, J. Kong, T. Palacios, Nano Lett. 12(9), 4674 (2012).
19. A. Nourbakhsh, A. Zubair, R.N. Sajjad, A. Tavakkoli K. G., W. Chen, S. Fang, X. Ling, J. Kong, M.S. Dresselhaus, E. Kaxiras, K.K. Berggren, D. Antoniadis, T. Palacios, Nano Letters **16**(12), 7798 (2016).
20. M. Hosseini, H. Karami, Journal of Computational Electronics 17(4), 1603 (2018).
21. J. Müller, U. Schröder, T.S. Böscke, I. Müller, U. Böttger, L. Wilde, J. Sundqvist, M. Lemberger, P. Kücher, T. Mikolajick, L. Frey, Journal of Applied Physics 110(11), 114113 (2011).
22. D. Martin, J. Müller, T. Schenk, T.M. Arruda, A. Kumar, E. Strelcov, E. Yurchuk, S. Müller, D. Pohl, U. Schröder, S.V. Kalinin, T. Mikolajick, Advanced Materials 26(48), 8198 (2014).
23. J. Müller, T.S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, T. Mikolajick, Nano Lett. 12(8), 4318 (2012).
24. T. Böscke, J. Müller, D. Bräuhaus, U. Schröder, U. Böttger, Appl. Phys. Lett. 99(10), 102903 (2011).
25. M.H. Lee, S. Fan, C. Tang, P. Chen, Y. Chou, H. Chen, J. Kuo, M. Xie, S. Liu, M. Liao, C. Jong, K. Li, M. Chen, C.W. Liu, in *2016 IEEE International Electron Devices Meeting (IEDM)*, pp. 12.1.1 (2016).
26. M.H. Park, Y.H. Lee, H.J. Kim, Y.J. Kim, T. Moon, K.D. Kim, J. Müller, A. Kersch, U. Schroeder, T. Mikolajick, C.S. Hwang, Advanced Materials 27(11), 1811 (2015).
27. W. Cao, J. Kang, W. Liu, Y. Khatami, D. Sarkar, K. Banerjee, in *Solid-State Device Research Conference (ESSDERC), 2013 Proceedings of the European* (IEEE, 2013), pp. 37.
28. T. Kobayashi, N. Hori, T. Nakajima, T. Kawae, Appl. Phys. Lett. 108(13), 132903 (2016).
29. C. Ko, Y. Lee, Y. Chen, J. Suh, D. Fu, A. Suslu, S. Lee, J.D. Clarkson, H.S. Choe, S. Tongay, R. Ramesh, J. Wu, Advanced Materials 28(15), 2923 (2016).
30. Z. Lu, C. Serrao, A.I. Khan, L. You, J.C. Wong, Y. Ye, H. Zhu, X. Zhang, S. Salahuddin, Appl. Phys. Lett. 111(2), 023104 (2017).
31. A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, T. Palacios, Nanoscale 9(18), 6122 (2017).
32. X. Wang, Y. Chen, G. Wu, D. Li, L. Tu, S. Sun, H. Shen, T. Lin, Y. Xiao, M. Tang, W. Hu, L. Liao, P. Zhou, J. Sun, X. Meng, J. Chu, J. Wang, NPJ 2D Mater. Appl. **1**(1), 38 (2017).
33. M. Si, C.J. Su, C. Jiang, N.J. Conrad, H. Zhou, K.D. Maize, G. Qiu, C.T. Wu, A. Shakouri, M.A. Alam, P.D. Ye, Nat. Nanotechnol. 13(1), 24 (2018).
34. F.A. McGuire, Y.C. Lin, K. Price, G.B. Rayner, S. Khandelwal, S. Salahuddin, A.D. Franklin, Nano Lett. 17(8), 4801 (2017).
35. W. Li, Phys. Rev. B 92(7), 075405 (2015).
36. H. Ota, K. Fukuda, T. Ikegami, J. Hattori, H. Asai, S. Migita, A. Toriumi, in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 15.2.1 (2017).
37. S. Salahuddin, S. Datta, Nano letters 8(2), 405 (2008).
38. A. Jain, M.A. Alam, IEEE Transactions on Electron Devices 61(7), 2235 (2014).
39. H. Liu, A.T. Neal, P.D. Ye, ACS nano 6(10), 8563 (2012).
40. S. Kim, A. Konar, W.S. Hwang, J.H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.B. Yoo, J.Y. Choi, Y.W. Jin, S.Y. Lee, D. Jena, W. Choi, K. Kim, Nat. Commun. **3**, ncomms2018 (2012).
41. S. Das, H.Y. Chen, A.V. Penumatcha, J. Appenzeller, Nano Lett. 13(1), 100 (2012).
42. F. Giannazzo, G. Fisichella, A. Piazza, S. Di Franco, G. Greco, S. Agnello, F. Roccaforte, Beilstein journal of nanotechnology 8, 254 (2017).
43. R. Kappera, D. Voiry, S.E. Yalcin, B. Branch, G. Gupta, A.D. Mohite, M. Chhowalla, Nature materials 13(12), 1128 (2014).
44. T.K. Song, Journal of the Korean Physical Society 46(1), 5 (2005).
45. A. Konar, T. Fang, D. Jena, Phys. Rev. B 82(11), 115452 (2010).

46. X. Wang, C. Liu, Y. Chen, G. Wu, X. Yan, H. Huang, P. Wang, B. Tian, Z. Hong, Y. Wang, S. Sun, H. Shen, T. Lin, W. Hu, M. Tang, P. Zhou, J. Wang, J. Sun, X. Meng, J. Chu, Z. Li, 2D Mater. **4**(2), 025036 (2017).
47. S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry, S. Datta, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits 1, 43 (2015).
48. H. Agarwal, P. Kushwaha, Y.K. Lin, M.Y. Kao, Y.H. Liao, J.P. Duarte, S. Salahuddin, C. Hu, IEEE Electron Device Letters 39(8), 1254 (2018).