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Performance Analysis of a Charge Plasma Junctionless Nanotube Tunnel FET Including the Negative Capacitance Effect

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This paper presents the technique of using the negative capacitance phenomenon in a charge-plasma junctionless nanotube tunnel field effect transistor (CP-JLTFET). In recent decades, owing to the fundamental physics of the "Boltzmann tyranny," the rising power dissipation in nano-devices has become an issue in complementary metal oxide semiconductor (CMOS) technology. So, it has become important to introduce new techniques into the operation of FETs to avert such types of bottlenecks. Negative capacitance is an effective technique to reduce threshold voltage and subthreshold slope < 60 mV/decade. This phenomenon reduces the power supply voltage and minimizes the power dissipation. In this work, the performance of the device is analyzed using a ferroelectric capacitor [P(VDF-TrFE)], which generates a negative capacitance effect during the device operation. The device performance is investigated with and without using negative capacitance. The impacts of varying ferroelectric thickness on the device performance, like threshold voltage, polarized charge, transconductance, etc., are also analyzed.

Key words: Negative capacitance, charge plasma, junctionless TFET, nanotube

INTRODUCTION

The demand for low-power integrated circuits for various applications is growing rapidly. One of the novel techniques to conserve power is reducing the value of operating voltage, which requires minimal subthreshold swing (within a reduced input voltage range). To fulfill the need for low-powered devices, miniaturization of devices was undertaken. However, due to the continuous scaling of devices, it became difficult and challenging to follow Moore's law as silicon technology had reached its physical limit. Additionally, due to the transport mechanism (thermionic emission) of metal oxide semiconductor field effect transistors (MOSFETs), the subthreshold slope possesses a fundamental limit of 60 mV/decade, which further hinders the reductions in power consumption and operating voltage. So, in recent years, some techniques which have been used to deal with the abovementioned challenges include, firstly, finding a new structure to overcome the physical limitations of MOSFETs and, secondly, using a new channel material.[1] Tunnel FETs (TFETs),[2] nano-electromechanical FETs,[3] and impact-ionization FETs (I-MOSFETs)[4] are examples of a few proposed structures. In TFETs or I-MOSFETs, the value of the subthreshold slope is < 60 mV/decade due to avalanche multiplication or band-to-band tunneling (BTBT).

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Several recent technological developments can help in the enhancement of semiconductor devices such as metamaterials,[5] near-zero-index materials,[6] plasmonics,[7] metasurfaces,[8] graphene,[9] nanoparticles,[10] and negative capacitance.[11] The abovementioned technologies can help in optimizing semiconductor device performance due to their material properties. The controlled energy bandgap, low refractive index, charge oscillations over the material surface, high mobility, quantum wells, and ferroelectric domains are the possible properties of recent material-based technological advancements that can help in modernizing next-generation integrated circuits. Here, the negative capacitance is used as an enhancement technique to amplify the gate oxide capacitance and interface dynamic voltage to significantly improve the performance of the proposed device.

After considering various issues with conventional FET-based devices, such as short channel effects, high power dissipation, leakage issues, and a larger value of the subthreshold slope, the concept of negative capacitance (NC) was investigated by researchers. The aim of NC in ferroelectric materials is to serve as a step-up transformer and to amplify the variation of surface potential in FETs as a function of change in gate voltage. The NC effect is observed by a particular reversal mechanism of ferroelectric materials.[12] For the practical implementation of NC, a ferroelectric capacitor (C_{Fe}, operating in a negative capacitance region)[13] is combined in series with a positive capacitor capable of stabilizing the effect of NC. There are two separate electric polarization states of a C_{Fe}. The ferroelectric material aligns its internal electric dipoles in a specific direction after applying an external electric field to the ferroelectric capacitor. Due to this, the ferroelectric capacitor behaves like a normal capacitor (a capacitor having a positive capacitance value). The series connection between C_{Fe} and the MOS capacitor (C_{MOS}), due to the interconnection of the ferroelectric capacitor with the gate stack of the MOS transistor, increases the total capacitance value under the condition $C_{Fe} < 0$. By varying the gate bias in the gate stack of the MOS transistor, the series-connected structure causes sudden enhancement of the differential charge in the internal node. This is known as negative capacitance.[14] A negative-capacitance FET (NC-FET) is one of the investigated devices in which ferroelectric material uses its negative capacitance phenomenon to reduce the threshold voltage and to improve the device performance.[15] To obtain the same surface potential, the technique of using a negative capacitor in the gate stack makes the total capacitance larger than its traditional value, which in turn reduces the required bias voltage. The structures of an NCFET and MOSFET are similar; the only difference is that Fe material is used instead of the gate insulator. This Fe material creates a negative capacitance effect. This negative capacitance effect depends upon the ability to change the state of Fe material from its local minimum to a nonequilibrium state. In the nonequilibrium state, its capacitance is negative, but the stage is very unstable, and by adding series capacitance, it can be stabilized.[16] Due to this, the channel potential, on an internal node, can be adjusted more than the applied voltage. Another invention, the TFET, is considered as an efficient device for low-power applications due to its minimum subthreshold characteristics and I_{OFF} current. These characteristics of TFETs allow the reduction in power dissipation and supply voltage (V_{DD}).[17] The main drawback of a TFET is its low I_{ON} current which can be improved by using high-k dielectric materials,[18] halo doping,[19] III-V compounds,[20] and so on. Recently, Lee et al.[21] introduced an NC-TFET in which lead zirconate titanate (PZT) was used as the ferroelectric (FE) gate dielectric, and, due to its negative capacitance effect, the ON current was improved. It is experimentally examined that in comparison to single-gate or double-gate structures, FETs with a gate-all-around structure have better performance attributes.

In this work, a negative capacitance technique is applied by adding a ferroelectric capacitor in series with the shell gate of a charge-plasma junctionless nanotube tunnel field effect transistor (CP-JLTFET)[22] in which co-polymer poly(vinylidene fluoride-trifluoroethylene [P(VDF-TrFE)] is used as ferroelectric material. P(VDF-TrFE) is one of the most commonly used materials and is readily available in the market due to its high-quality polarization characteristics.[23] For investigating the beneficial impacts of NC of ferroelectric material on the device, such as transfer characteristic and subthreshold slope, the Landau–Khalatnikov (L–K) model and numerical simulation model are combined. The impact of using ferroelectric material is described in the subsequent section. With the simulated results (discussed in section III), it is found that the CP-JLTFET with a negative capacitance effect can achieve an optimized subthreshold slope value and reduced threshold voltage. The advantages of a CP-JLTFET with negative capacitance effects are low cost, fewer fabrication steps, high ON current, optimized subthreshold slope, reduced threshold voltage, and so on, which can be proved useful for low-power applications in the future.

DEVICE STRUCTURE AND SPECIFICATION

The device specifications are presented in Table I. The two-dimensional (2D) schematic structure of the device, without negative capacitance and with negative capacitance, is shown in Fig. 1. The device is based on a P-I-N structure where the source is P-type, the gate is light p-type, and the drain is n-type. The device is junctionless and is designed on a silicon nanotube using the charge plasma concept.

Table I. Parameters and specifications of a CP-JLTFET

Device parameters and specifications	Value
Channel length (nm)	50
Oxide thickness (nm)	1
Radius (nm)	5
Doping (cm^{-3})	1×10^{19}
Dielectric material	SiO_2
Work function of shell gate metal (eV)	4.5
Work function of core source metal (eV)	5.93
Material-dependent constants (Landau parameters)	
α (cm/F)	−1.8e11
β (cm^5/F/$Coul^2$)	5.8e22
Γ (cm^9/F/$Coul^4$)	0
Negative capacitance material	Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)]

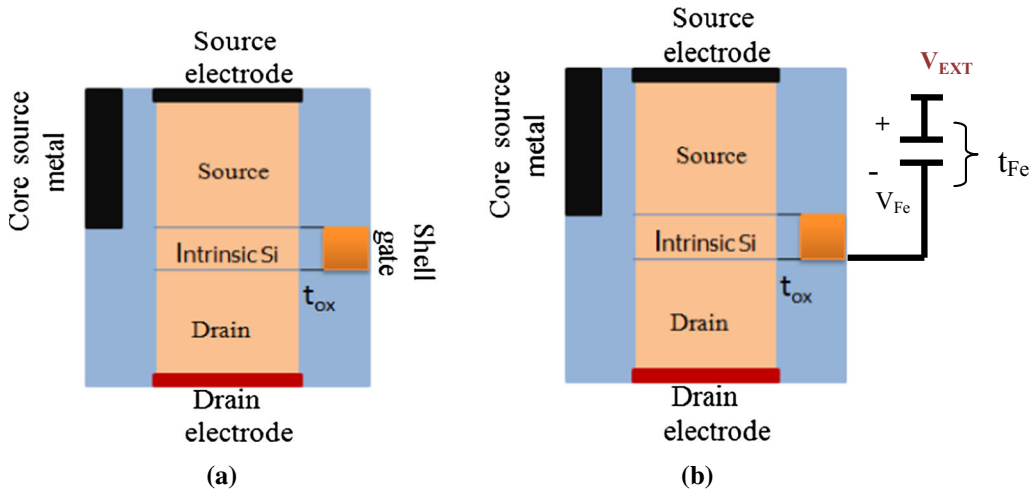

Fig. 1. (a) Schematic 2D cross-sectional structure of the CP-JLTFET without negative capacitance. (b) Schematic 2D cross-sectional structure of the CP-JLTFET with negative capacitance.

To produce a charge plasma effect, only a core part of the nanotube is used by inserting source metal, which in turn optimizes the fabrication process as well as area. Due to the charge plasma induction of positive charge carriers by the core source metal, the hole concentration is high in the source region. This phenomenon significantly reduces the minority charge carriers at the source side. On the other side, the electron concentration in the channel is lower due to the higher gate work function, and is constant in the drain side (in OFF state) due to uniform doping.

When gate bias is applied, the negative charge carriers increase and reduce the hole concentration within the channel to invert the region for better tunneling of charge carriers. Consequently, the drain current improves. The core source metal consists of platinum (work function = 5.93), and aluminum (work function = 4.5) is used to form the shell gate. In our work, an external ferroelectric capacitor is connected to the shell gate of the CP-JLTFET for a negative capacitance effect. Here, P(VDF-TrFE)[24] is used as the ferroelectric dielectric. During the performance analysis of the device (using the NC effect), the absolute value of ferroelectric capacitance and intrinsic gate capacitance should be close.[25] In order to achieve the NC effect, the series combination of C_{Fe} and C_{int} should be positive in the entire region of operation as the negative value of the total capacitance causes instability which results in hysteresis. For numerical simulation and calculation, the absolute temperature of the CP-JLTFET is kept at 300 K.

The L–K equation is used to describe the charge–voltage (Q–V_f) characteristics of the ferroelectric material, which is written as (1),

$$V_f = a_0 Q + b_0 Q^3 + c_0 Q^5 \quad (1)$$

where Q denotes the charge per unit area of the ferroelectric material, and coefficients a_0, b_0, and c_0 represent the Landau parameters a, b, and c of the ferroelectric material, respectively:

$$a_0 = 2t_f a,\ b_0 = 4t_f b,\ \text{and}\ c_0 = 6t_f c.$$

The various models used to design the CP-JLTFET are the Shockley–Read–Hall (SRH), Lombardi mobility, local band-to-band tunneling (BTBT) for tunneling of carriers, and auger recombination models. The working mechanism of the device is BTBT, and the Wentzel–Kramer–Brillouin[26] approximation is used for the evaluation of the numerical tunneling probability. A very fine mesh is created near the tunneling interface of the CP-JLTFET. The device is designed and simulated using the Silvaco Atlas tool[27] and the Landau–Khalatnikov model or L–K model.

SIMULATED RESULTS AND DISCUSSION

Figure 3 depicts the capacitance of the CP-JLTFET at low applied bias in which C_{gg}, C_{Fe}, and C_T denote the gate oxide capacitance, ferroelectric oxide capacitance, and total capacitance of the device, respectively. Here, C_{gg} is calculated as (C_{gs} + C_{gd}), and C_T is calculated as a series combination of C_{gg} and C_{Fe}. The simulated graph shows that the overall capacitance of the device improves at low bias because the negative differential capacitance of the ferroelectric oxide compensates for the positive capacitance of the device. This phenomenon in turn improves the total capacitance ($C_T = C_{gg} + C_{Fe}$) and increases the surface potential at low bias. Additionally, for the benefit of negative capacitance, the absolute values of C_{Fe} and C_{gg} need to be approximately close, and during the whole operation, the combination of both capacitances should remain positive as the negative value leads to instability. The graphs from Figs. 4, 5, 6, and 7 are simulated without using the negative capacitance effect and with using the negative capacitance effect. The simulation result (Fig. 4) of the transfer characteristic shows the reduced value of gate voltage in the presence of negative capacitance. The negative capacitance effect of the ferroelectric dielectric amplifies the gate voltage in the subthreshold and overdrive regions and reduces the threshold voltage, which in turn reduces the required gate voltage sustaining the same value of the ON current (10^{-6} A/μm). Figure 3 also proves the improved transfer characteristic of the device.

Figure 5a, b and c shows the simulated graph of the electron concentration, hole concentration, and potential of the CP-JLTFET. Due to the negative capacitance effect of the ferroelectric dielectric, the device attains a higher electron concentration at low bias. This phenomenon further leads to the generation of an electric current at low bias. It is due to the amplification of the internal voltage and reduction in threshold voltage by the ferroelectric dielectric (in the series-connected structure of capacitance) which increases the total capacitance at low voltage. This explanation also holds true for the hole concentration. The increasing electron concentration indicates the majority charge carriers, and the decreasing hole concentration indicates the minority charge carriers of the device. From Fig. 5c, it is seen that the surface potential of the CP-JLTFET is steeper after using negative capacitance. The reason behind this phenomenon is the amplification of internal voltage (in ON state) due to negative capacitance. As the surface potential is directly linked with gate voltage, the internal voltage amplification allows the surface potential to attain higher value at low bias. These graphs also prove the improved transfer characteristic of the device shown in Fig. 4. The simulated graphs (Fig. 6) depict the electric field, recombination rate, and transconductance of the device. The results show that in the presence of negative capacitance, the device attains the optimized value of the electric field (Fig. 6a) at low V_{GS}. This phenomenon causes more tunneling of the charge carrier, at low bias, through the barrier, which further enhances the drain current also. Again, Fig. 6b shows a similar result for the recombination rate. The recombination rate depends upon the value of the electric field at a point in the tunneling path. The quantized energy and momentum remain conserved during the process of recombination. The decreasing recombination rate denotes the electrons recombine with holes in the conduction band, and that the number of electrons remaining in the valence band is less. That is why the recombination rate decreases with the decreasing number of electrons available for recombination. The transconductance behavior of the CP-JLTFET is shown in Fig. 6c. Transconductance is the performance parameter of any device [such as an FET or a bipolar junction transistor (BJT)]. The larger value of transconductance leads to greater gain (amplification) of the device. The transconductance is defined as the "change in output current to the change in applied voltage," which can be expressed as (2)

$$\text{Transconductance}\,(g_m) = \mathrm{d}I_D/\mathrm{d}V_{GS}\,\text{at constant}\,V_{DS} \tag{2}$$

As the ferroelectric dielectric has a negative capacitance ($C_{Fe} < 0$) value, the total capacitance of the device increases abruptly before the applied voltage, and, consequently, the device shows a better transconductance characteristic (10^{-6} S/μm) at low bias.

The simulated graph in Fig. 7 shows the electron quasi-Fermi level and hole quasi-Fermi level of the device. The term quasi-Fermi level is used for the Fermi level which describes the concentration of electrons and holes at any point when they are not in an equilibrium state. The reasons for the displacement from the equilibrium state could be the application of an external voltage or by exposure to light, which changes the concentration of electrons in the conduction band and valence band. As discussed in the above results, due to the negative capacitance effect of the ferroelectric dielectric, the

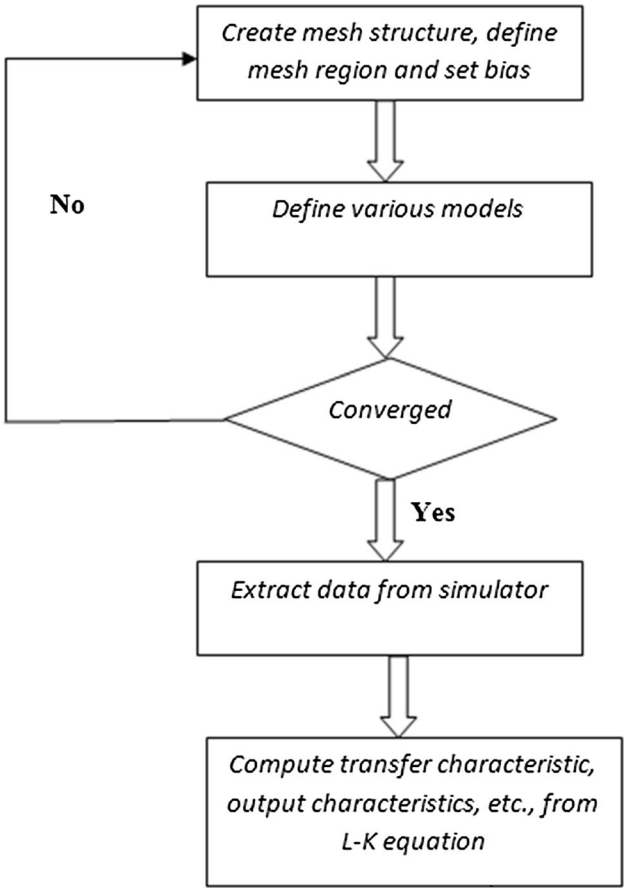

Fig. 2. Process flow for the simulation of negative capacitance in the CP-JLTFET.

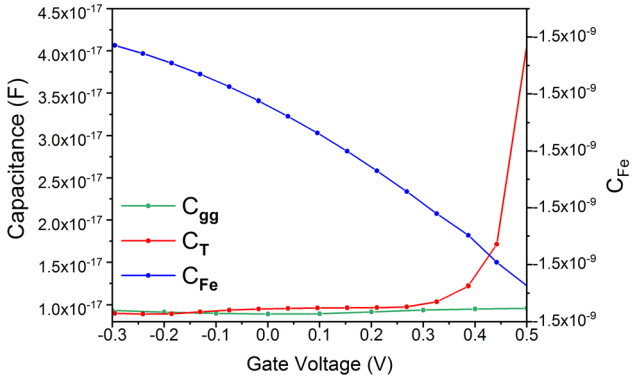

Fig. 3. Capacitance of the CP-JLTFET at V_{GS} = 1.3 V.

shift in threshold voltage also gives the optimized value of the quasi-Fermi level of both carriers at low bias. Now, it can be summarized from simulated graphs (Figs. 1, 2, 3, 4, 5, 6, and 7) that the negative capacitance effect leads to the improved threshold voltage and subthreshold slope at low bias without compromising the other characteristics, such as carrier concentration, potential, and electric field, of the device. In Fig. 8, the effect of varying ferroelectric thickness on the polarized charge is

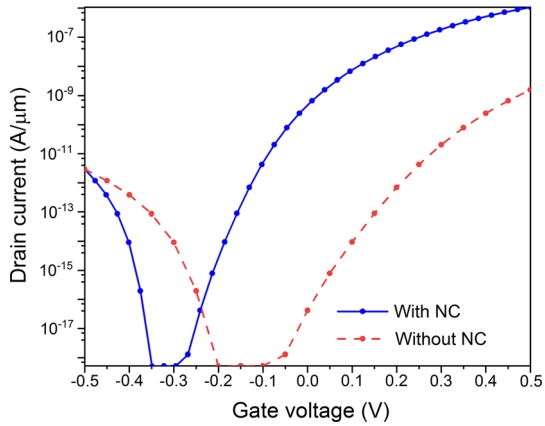

Fig. 4. Transfer characteristic of the CP-JLTFET with and without the negative capacitance effect at V_{GS} = 0.5 V.

shown. The term 'polarized charge' means that the centers of positive and negative charges are separated from each other. The graph shows that as the thickness of the ferroelectric decreases, the polarized charge increases. It is due to the inverse relationship between t_{Fe} and polarized charges. For better device performance, a lower polarized charge is required. So, we must keep the optimum value of t_{Fe} to obtain a lower polarized charge. The plot of threshold voltage and subthreshold slope with varying thickness of the ferroelectric dielectric is shown in Fig. 9a. For any FET, reducing the threshold voltage is an effective technique to minimize the power dissipation of the device. The graph shows the importance of tuning t_{Fe} to obtain the optimized value of threshold voltage and subthreshold slope. It is known that a lower value of t_{Fe} requires a higher value of threshold voltage (0.85 V), while the larger value of t_{Fe} needs lower threshold voltage (0.65 V) to start any operation. On the other hand, the subthreshold slope denotes the switching speed of a FET transistor, which is also known as Boltzmann tyranny.[8]

Mathematically, the subthreshold slope is expressed as (3)

$$SS = \frac{\partial VG}{\partial \Phi s}\frac{K_B T}{q}\ln 10 \qquad (3)$$

As in the above equation, the second term is constant (60 mV/decade at 300 K), so the negative capacitance works on optimizing the first term. The graph shows a better subthreshold slope (~ 35 mV/decade) of the device for the higher value of t_{Fe}. It means that the switching speed of the device can be improved in the presence of negative capacitance with an optimized value of t_{Fe}. From Fig. 5c, it can be observed that the negative capacitance amplifies the internal voltage and provides a higher surface potential at low bias. In this way, it also minimizes the subthreshold slope of the device. Figure 9b

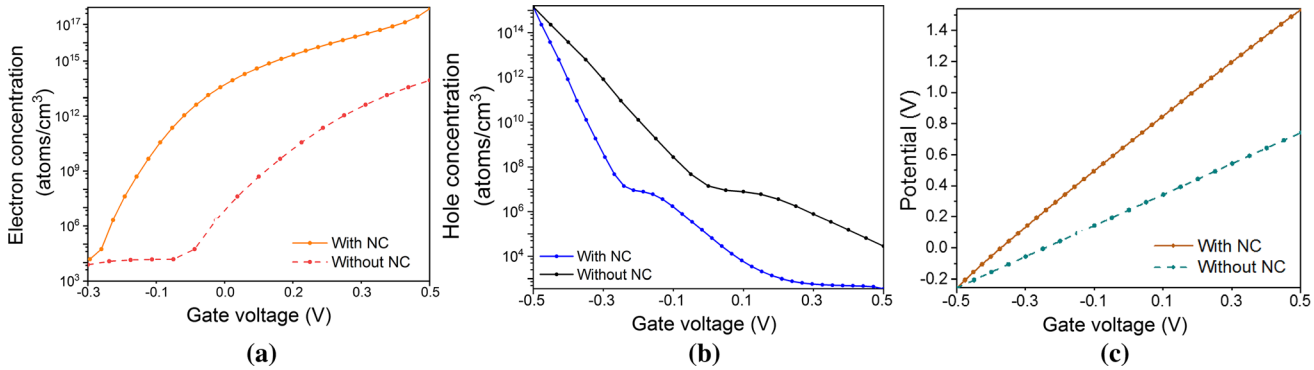

Fig. 5. (a) Electron concentration, (b) hole concentration, and (c) potential of the CP-JLTFET with and without the negative capacitance effect at V_{GS} = 0.5 V.

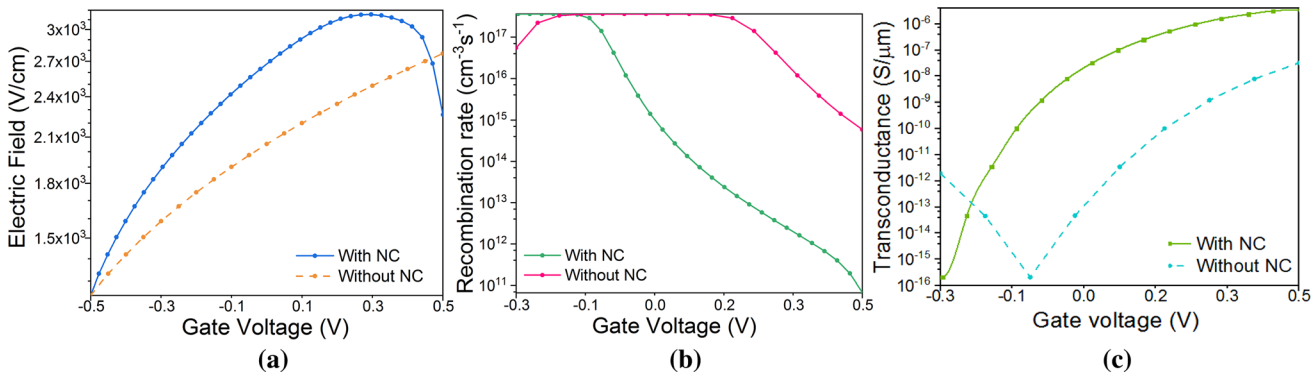

Fig. 6. (a) Electric field, (b) recombination rate, and (c) transconductance of the CP-JLTFET with and without the negative capacitance effect at V_{GS} = 0.5 V.

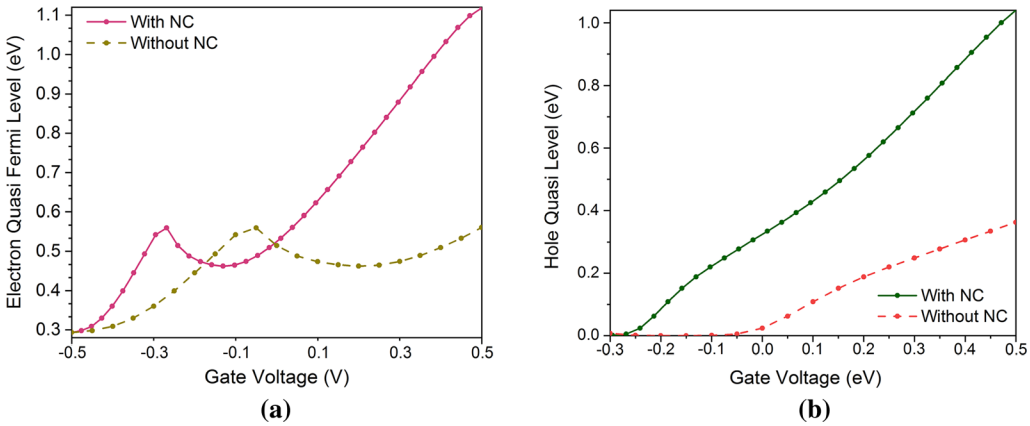

Fig. 7. (a) Electron quasi-Fermi level and (b) hole quasi-Fermi level of the CP-JLTFET with and without the negative capacitance effect at V_{GS} = 0.5 V.

shows the effect of varying ferroelectric thickness on the applied voltage. The graph shows that the voltage has a negligible change up to a certain range of ferroelectric thickness (till 10^{-5}cm), and after that, with the increment in the ferroelectric thickness, there is a drop in the voltage. In other words, when the values of t_{Fe} are converted into nanometers, it is observed that in nanoscale, the value of t_{Fe} is constant, while beyond nanoscale, a drop can be seen in the value of t_{Fe}. Figure 9c shows the maximum transconductance obtained for different thicknesses of the ferroelectric dielectric. It is found that for low t_{Fe}, a lower value of transconductance is obtained, while for the higher value of t_{Fe}, an increased value of transconductance is obtained. It can be concluded from Fig. 9a that to obtain the low threshold voltage/subthreshold slope and the increased value of transconductance, the thickness of the ferroelectric dielectric should be large enough to efficiently amplify the voltage.

The effects of varying the thickness of the ferroelectric dielectric on the device performance are shown in Figs. 10, 11, and 12. The importance of tuning the ferroelectric thickness is studied in this section. The graphs are simulated using negative capacitance as well as without using negative capacitance. In Fig. 10a, the electron concentration of the device is simulated. The results show that the device attains the same amount of electron concentration with and without negative capacitance. Additionally, it is also noted that with the increasing thickness of the ferroelectric, in the presence of negative capacitance, the value of threshold voltage also starts to reduce. It is due to that the larger value of t_{Fe} which shifts the threshold voltage to the left and generates the same electron concentration at lower gate voltage. The same explanation holds true for the electric field (refer to Fig. 10b) also. These two graphs also justify the obtained transfer characteristic graph (Fig. 10c). The lower threshold voltage due to the larger ferroelectric thickness leads to the generation of an electric field and electron concentration at low bias which further boosts the drain current at a low bias (refer to the related graphs discussed above). On the other hand, the lesser value of ferroelectric thickness requires a high threshold voltage. The transconductance behavior of the device with and without using negative capacitance is also discussed in Fig. 6c. Here, in Fig. 11a and b, the effect of varying ferroelectric thickness on the transconductance behavior of the device is shown.

The transconductance characteristic is shown in both log and the linear scale. The results reveal that the larger value of t_{Fe} leads to an optimized value of transconductance at a low threshold voltage.

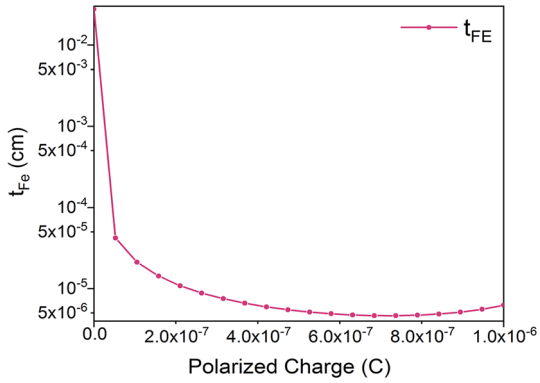

Fig. 8. Thickness of ferroelectric material as a function of polarized charge.

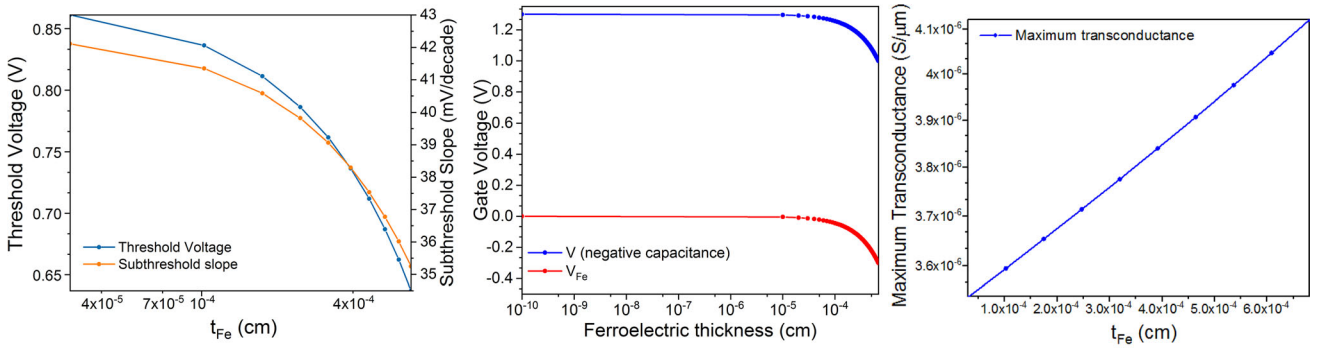

Fig. 9. (a) Threshold voltage and subthreshold slope, (b) gate voltage, and (c) maximum transconductance of the CP-JLTFET with varying ferroelectric oxide thickness [P(VDF-TrFE)].

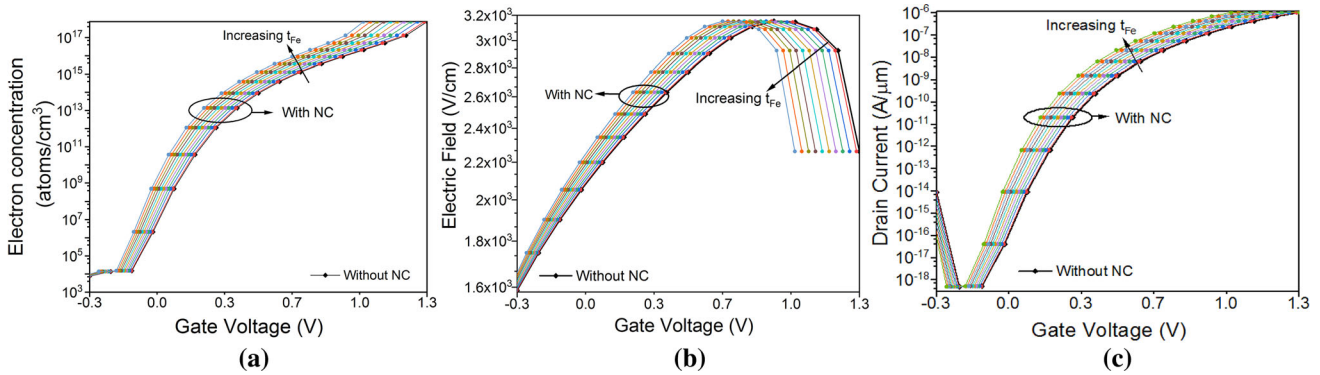

Fig. 10. (a) Electron concentration, (b) electric field, and (c) transfer characteristic of the CP-JLTFET for varying ferroelectric oxide thickness (t_{Fe}) at V_{GS} = 1.3 V.

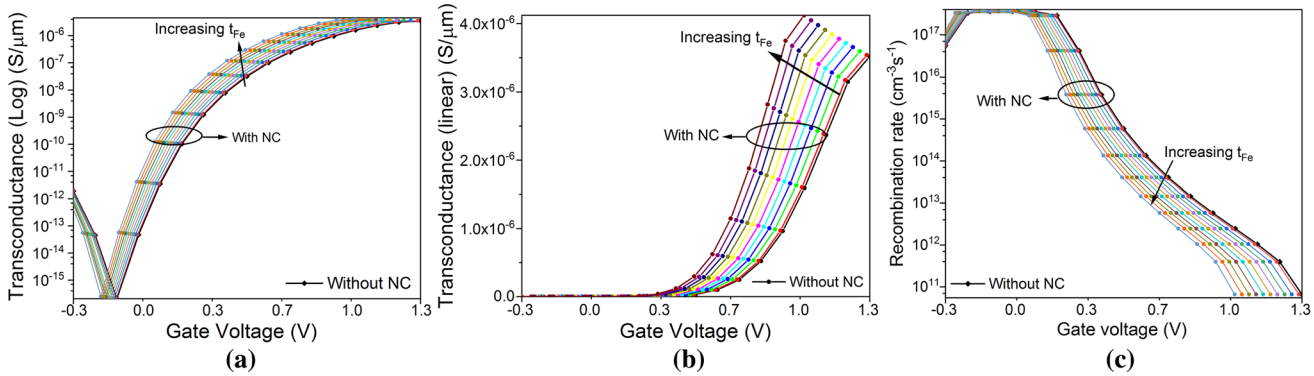

Fig. 11. (a) Transconductance (log), (b) transconductance (linear), and (c) recombination rate of the CP-JLTFET for varying ferroelectric oxide thickness (t_{Fe}) at V_{GS} = 1.3 V.

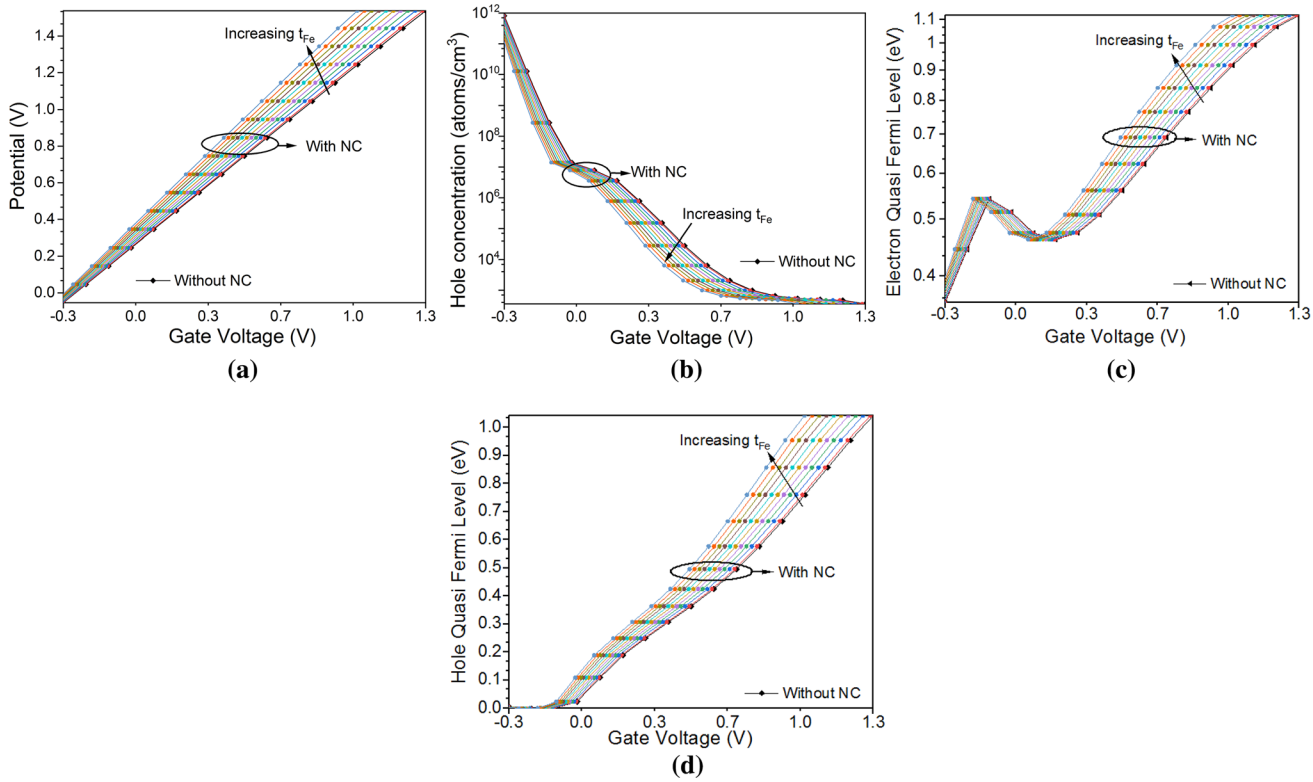

Fig. 12. (a) Potential, (b) hole concentration, (c) electron quasi-Fermi level, and (d) hole quasi-Fermi level of the CP-JLTFET for varying ferroelectric oxide thickness (t_{Fe}) at V_{GS} = 1.3 V.

Figure 11c depicts that for a larger value of t_{Fe}, the device attains the optimized value of recombination rate at a low bias (also refer to Fig. 6b). Meanwhile, for the lesser value of t_{Fe}, the device requires a higher value of gate voltage to obtain the same recombination rate. Similarly, in the simulated graphs of Fig. 12, it is found that the device shows better characteristics (potential, hole concentration, electron quasi-Fermi level, and hole quasi-Fermi level) for a higher value of t_{Fe}. It is because the greater ferroelectric thickness (in negative capacitance) reduces the threshold voltage and subthreshold slope and shows the improved characteristics of the device. According to the rule, the higher value of t_{Fe} leads to hysteresis, while for low values of t_{Fe}, the step-up voltage conversion capability of the devices vanishes.

That is why it is important to tune the thickness of the ferroelectric material so that the amplification of the voltage can be done properly with minimum hysteresis. In summary, it can be said that to obtain low threshold voltage and reduced subthreshold slope without compromising the other characteristics of the device, it is important to use the optimized thickness of the ferroelectric dielectric. Figure 13 shows the simulated and experimental hysteresis curves of the ferroelectric material [P(VDF-TrFE)]. This characteristic is obtained using (4)

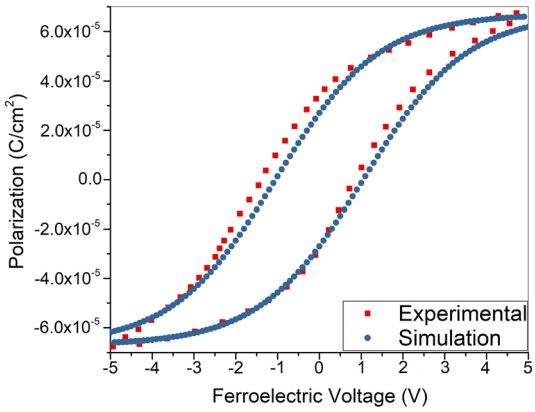

Fig. 13. Simulated and experimental curve of polarization and ferroelectric voltage of a ferroelectric capacitor.

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \quad (4)$$

According to Landau's theory, a ferroelectric material has a nonlinear C–V relation in which the negative capacitance phenomenon exists in a certain range of charge and voltage. The same theory is also applicable here. The simulated hysteresis curve shows the larger value of saturation polarization (P_s) and the optimized values of remnant polarization (PR) and coercive field (E_c). It is due to the better phase transition of P(VDF-TrFE). During the phase transition, there is a sudden increment in the charges tied by P(VDF-TrFE)'s original polarization, which further accelerates another charge change in the internal electrode.[14] In this way, the series connection of the capacitor with the shell gate can improve the subthreshold slope of the device.

CONCLUSION

In the paper, the performance of a CP-JLTFET has been analyzed with and without a negative capacitance effect. The benefits of the proposed structure include: less fabrication complexity, less area, low cost, reduction of stray charges (due to core part of the nanotube), and less noise without sacrificing the ON current of the device. In our work, the effects of varying ferroelectric thickness on the device performance are observed and analyzed. From the simulated graphs, it is found that the negative capacitance phenomenon of the ferroelectric dielectric minimizes the threshold voltage and reduces the subthreshold slope (> 60 mV/decade) of the device without compromising the drain current. Additionally, with the increasing t_{Fe}, a drop in the voltage is also seen. This study shows the improved device characteristics, such as carrier concentration, potential, and quasi-Fermi level, at low bias in the presence of the negative capacitance effect. It is also determined from the simulated graph that for better performance analysis of the device, the thickness of the ferroelectric dielectric should be properly tuned. It means that the thickness of the ferroelectric dielectric should be neither very small nor very large. In this way, a complete investigation has been done to analyze the performance of the device. The investigation shows that a CP-JLTFET with a negative capacitance effect can be used for sensing applications and other low-power application devices.

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