



The Aromatic Thermosetting Copolyester for Schottky Diode Applications in a Wide Temperature Range

İKRAM ORAK,^{1,6} ZAKIR CALDIRAN,² METE BAKIR,³ OSMAN S. CIFCI,⁴
and ADEM KOCYIGIT⁵

1.—Vocational School of Health Services, Bingöl University, 12000 Bingöl, Turkey. 2.—Department of Electric and Energy, Ardahan Technical Sciences V.H.S., Ardahan University, 75000 Ardahan, Turkey. 3.—Department of Material Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA. 4.—Department of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA. 5.—Department of Electrical Electronic Engineering, Engineering Faculty, Iğdir University, 76000 Iğdir, Turkey. 6.—e-mail: ikramorak@gmail.com

The aromatic thermosetting copolyester (ATSP) was deposited on *p*-Si substrates by the spin coating method, and the thickness of thin film layer was about 50 nm. It was employed to fabricate metal-polymer-semiconductor (MPS) heterojunctions as interfacial layers between metal contact and *p* type Si. The morphological properties of the Al/ATSP/*p*-Si heterojunctions were investigated by Scanning Electron Microscope (SEM) and an Atomic Force Microscope. The electrical characteristics of the heterojunctions were analyzed within a wide temperature range between 100 K and 500 K and frequency range. The current–voltage–temperature (*I–V–T*) characteristics of the MPS heterojunctions were explained by the Thermionic Emission (TE) theory and Norde function. Critical electrical parameters including leakage current (I_0), barrier height (Φ_b) and ideality factor (n) and series resistance (R_s) were calculated by *I–V–T* characteristics in dark conditions. The value of n and Φ_b was obtained as 2.56 and 0.78 eV at 300 K. The n and Φ_b values were obtained as strong function of the temperature depending on barrier inhomogeneity. The temperature dependent rectification ratios of the Al/ATSP/*p*-Si heterojunctions were calculated and discussed in the details considering effective operating temperatures. The capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) characteristics were measured at 300 K. To obtain Fermi energy (E_F), donor concentration (N_a), maximum electric field (E_m), Φ_b and interface states (N_{ss}), were performed on the bases of voltage and frequency at 300 K. From the electrical analysis results, it is proposed that the MPS device can be employed in electronic devices at low and high temperatures.

Key words: Aromatic thermosetting copolyester, metal-polymer-semiconductor (MPS), thermionic emission theory, Norde function, ATSP

INTRODUCTION

Over the years, metal-oxide-semiconductors (MOS), metal-insulator-semiconductors (MIS) and metal-polymer-semiconductors (MPS) have been commonly used for such as diode, capacitors, solar cells, thin film transistors and electronic technologies.^{1–3} During the past decade, polymer Schottky

diodes (SDs) and their electronic devices applications have been extensively investigated.^{4–8} Especially, organic and polymer semiconductors are used in all photonic, plasmonic and electronic devices.^{9,10} They have some advantages such as low cost, useful, easy fabrication and being flexible.^{11–13} Especially, aromatic thermosetting copolyester (ATSP) has been used in many research areas including electrical conductivity, membranes, and electromagnetic shielding.¹⁴ Moreover, due to its high-performance polymer morphology, it has been investigated for three-dimensional networks and the physical properties.¹⁵ On the other hand, ATSP can be used in silicon-based microelectronics applications and micro-electromechanical systems.¹⁶ Because of the thermal and mechanical performance, the ATSP can also be employed in low and high temperature applications. In addition to these features, it has been used as an interfacial layer in some electronic devices such as diodes and photodiodes.³

The goal of this study is to exhibit that ATSP can be utilized in Schottky diodes for a wide range temperature. The electrical characteristics of ATSP/*p*-Si Schottky diodes were investigated under different temperatures. The effects of ATSP between the metal and semiconductor were characterized in the wide range temperatures from 100 K to 500 K with 50 K steps. The electrical characteristics of the ATSP/*p*-Si Schottky diode such as n , Φ_b and R_s were examined from the I - V measurements. Furthermore, the C - G - V characteristics were also analyzed at various frequencies of 10 kHz to 1.6 MHz at 300 K.

EXPERIMENTAL DETAILS

In the present study, a one side polished *p*-type Si (100) wafer was used for fabrication of ATSP/*p*-Si. The wafer thickness and resistivity were 325 ± 25 and μm 10 Ω -cm, respectively. Before the other steps, the silicon wafer is sliced into symmetrical pieces as $2.0 \times 2.0 \text{ cm}^2$ with a diamond pen. Firstly, the pieces were cleaned with deionized (DI) water (resistivity 18 M Ω cm) using an ultrasonic bath for 10 min. Then, the pieces were cleaned with the RCA cleaning procedure (i.e., a 10 min boil in $\text{NH}_3 + \text{H}_2\text{O}_2 + 6\text{H}_2\text{O}$ followed by a 10 min boil in $\text{HCl} + \text{H}_2\text{O}_2 + 6\text{H}_2\text{O}$) with the final cleaning step diluted HF for 30 s, and then rinsed by ultrasonic vibration in DI water for 10 min and dried by high-purity nitrogen gas. An Al metal material at 100 nm thickness was evaporated using a sputtering system on the back side of the *p*-Si for the ohmic contact. Stock solutions of ATSP (0.005 g/ml) were prepared in THF (tetrahydrofuran). The ATSP solution was directly coated on the front surface of the *p*-Si substrate with spin coating which was rotated 2000 rpm for 30 s then cured at 300°C in argon atmosphere. Additionally, more information about the preparation process can be found in our previous

studies.^{3,17} The aluminum metal contacts have been sputtered by a sputter system via a hole array mask on the front sample surface of the ATSP/*p*-Si. The thickness measurements were obtained by a Dektak surface profilometer as 50 nm. This measurement was repeated five times. The details of thickness measurements were given in our previous articles.³ The standard deviation is about ± 3 nm in the our systems. The SEM and AFM images were taken by Hitachi S-4800 and Asylum Research MFP-3D. The I - V measurements of the Schottky diode have been performed using a Keithley 2400 Picoammeter/Voltage Sourcemeter for a wide range of temperatures. The C - V and G - V characterizations were taken from a HP model 4192A LF impedance analyzer at room temperature at various frequencies. Figure 1 shows schematic illustration and measurements setup of the Al/ATSP/*p*-Si Schottky diode. This configuration depicts the classical MPS structure. The thickness of the Al Schottky contact is about 100 nm.

RESULTS AND DISCUSSION

The 2D and 3D AFM images of the ATSP thin interlayer at $3 \mu\text{m}^2$ surface areas are shown in Fig. 2a and b, respectively. The surface of the ATSP is homogenous for the surface areas of $3 \mu\text{m}^2$. The RMS value of the ATSP surface was measured to be 1.25 nm. The result highlighted that the ATSP has a very proper and homogenous surface for Schottky diodes as an interfacial layer.

Figure 3a and b exhibit the SEM images of the Al contacts on the ATSP and ATSP thin film layer, respectively. While the Fig. 3a confirmed the deposition of Al contact on the ATSP, Fig. 3b revealed the homogenous thin film surface of the ATSP. The homogenous thin film surface imparts that ATSP is a promising candidate for MPS structures.¹⁸

The I - V characteristics of the Al/ATSP/*p*-Si Schottky diode were analyzed in the wide temperature range of 100–500 K steps by 50 K by helium cryostat and power supply. The important Schottky diode characteristics parameters, n and Φ_b , can be

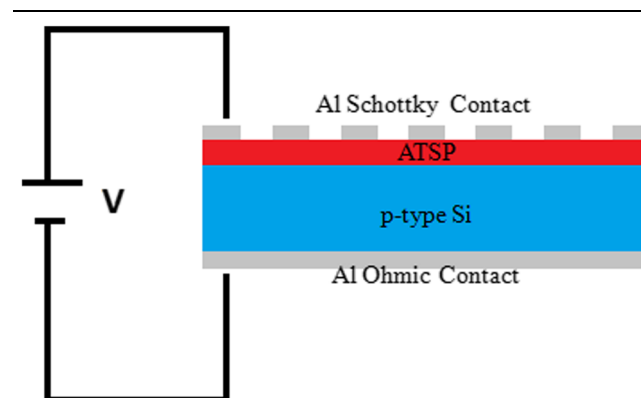


Fig. 1. The schematic representation and of Al/ATSP/*p*-Si Schottky diode used in measurements.

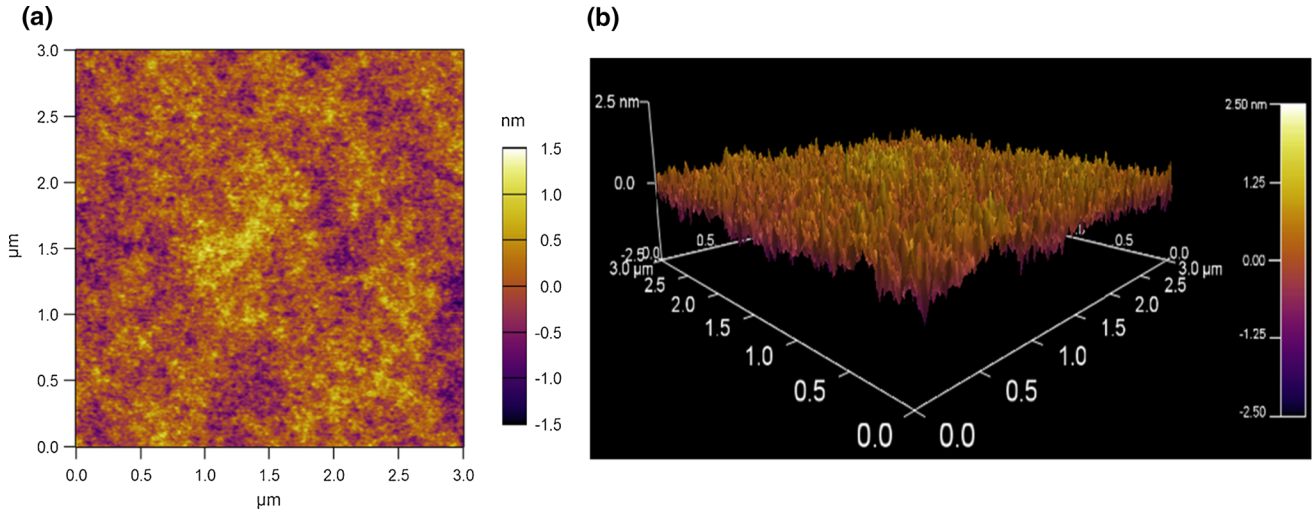


Fig. 2. The 2D and 3D images of the ATSP thin film layer.

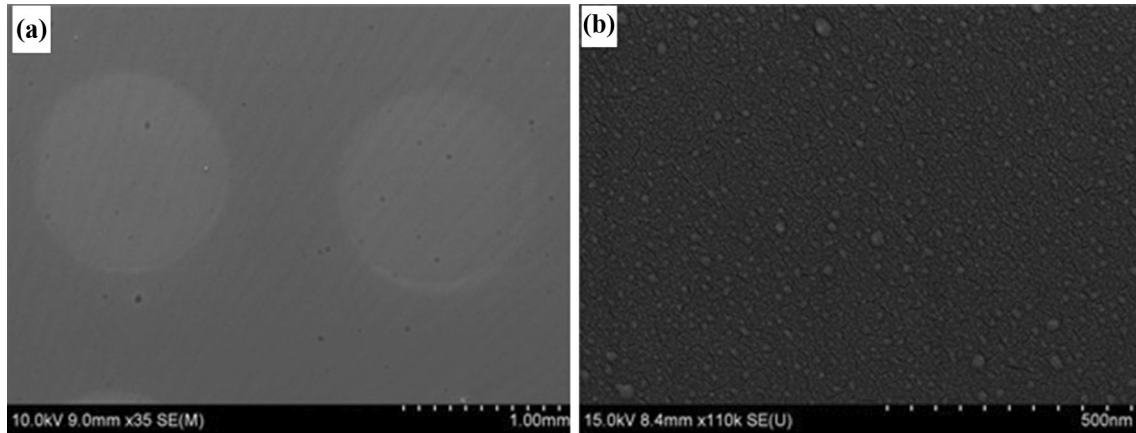


Fig. 3. The SEM images of (a) the metallic Al contacts on the ATSP, (b) ATSP thin film layer.

determined by the $\ln I$ versus V plots using standard thermionic emission theory (TE) for $\geq 3kT/q$. The diode current expression is explained according to the TE theory as follows^{19–21}

$$I = I_0 \exp\left(\frac{qV}{nkT}\right) \left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \quad (1)$$

where q is the effective electronic charge, k is the Boltzmann constant, V is the bias voltage, n Φ_b is the ideality factor and the barrier height, respectively. I_0 is the saturation current derived from the straight line intercept of $\ln I$ at $V = 0$ and is given by,

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right), \quad (2)$$

where A is the diode contact area ($7.85 \times 10^{-3} \text{ cm}^2$), A^* is the effective Richardson constant of $32 \text{ A cm}^{-2} \text{ K}^{-2}$ for p -type Si,^{19,22} T is the instant temperature, Φ_b is the zero-bias barrier height (BH), which can be calculated from the following this equation,

$$\Phi_b = \frac{kT}{q} \ln(AA^*T^2/I_0). \quad (3)$$

Moreover, the intercept of the linear regime at semi-log I - V plot is used to calculate the n values by the ideal TE model using the following equation,

$$n = \frac{q}{kT} \left(\frac{dV}{d \ln I}\right). \quad (4)$$

The semilog-bias current voltage characteristics of the Al/ATSP/ p -Si Schottky diode are shown in Fig. 4 for the temperature range of 100–500 K. The Al/ATSP/ p -Si Schottky diode exhibited excellent rectification behavior, and the current decreased periodically with decreasing temperature in the reverse bias region. The diode parameters of the Al/ATSP/ p -Si Schottky diode were calculated from I - V measurements by the TE model. The calculated experimental values of Φ_b and n are 0.78 eV and 2.56 at 300 K, and other values of Φ_b and n with

leakage current at various temperatures are listed in Table I.

According to Table I, the I_0 and Φ_b values usually increased with increasing temperature, but n values decreased towards room temperature and then increased. The changes at the diode parameters with changing temperature can be attributed to barrier inhomogeneity.²³ The value of n is greater than the expected value at room temperature. This is attributed to some crucial interface states, native oxide or polymer ATSP layers and series resistance occurred between metal and semiconductor surface.^{24–31}

The Φ_b values were increased from 0.26 eV to 1.15 eV with increasing temperature from 100 K to 500 K, respectively. It is clearly known that the

temperature dependence of the Φ_b is not understood regarding the reported low temperature of the Φ_b or band gap (E_g).²⁵ As the temperature increases, a lot of electrons have adequate energy to overlap the higher barrier. So, Φ_b increases with increasing temperature and applied bias voltage.²⁶

Rectification ratio (RR) is a parameter related to the characteristic and quality of the diodes. As can be seen in Fig. 5, the RR was affected with temperature on the Al/ATSP/*p*-Si Schottky diode. As shown in the figure, the RR values decreased with increasing temperature. This result shows that the ATSP interface layer can provide higher RR values at lower temperatures.

The values of n were calculated from the $\ln(I)-V$ plot for each temperature in the voltage range of

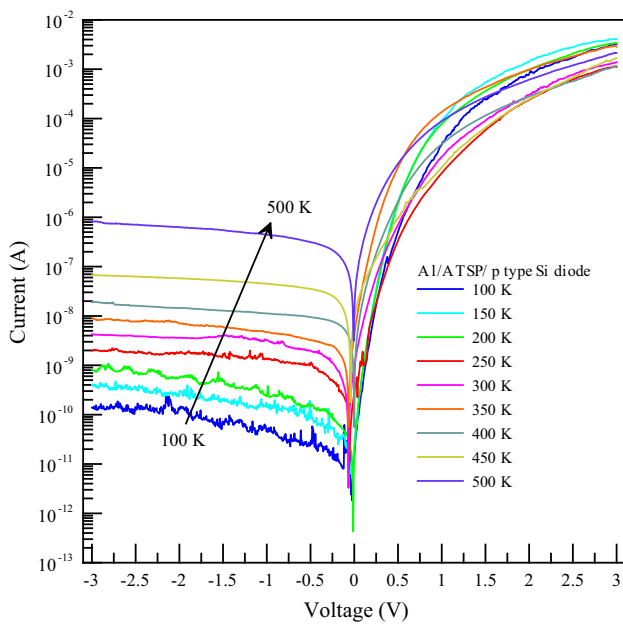


Fig. 4. The temperature-dependent forward and reverse bias semi-log I - V characteristics of Al/ATSP/*p*-Si Schottky diode in the range of 100–500 K

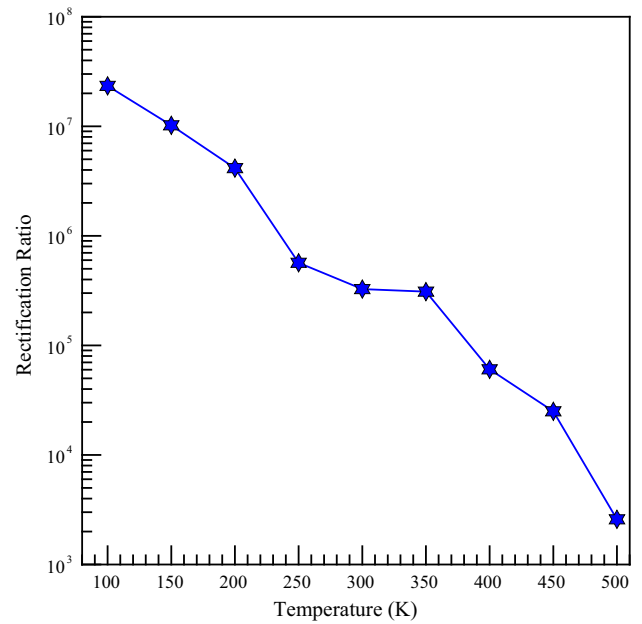


Fig. 5. The RR characteristics of the Al/ATSP/*p*-Si Schottky diode from 100 K to 500 K

Table I. Some electrical characteristics of Al/ATSP/*p*-Si Schottky diodes

Temperature (K)	Thermoionic emission theory			Norde function	
	I_0 (leakage current) A	Φ_b (Barrier height) eV	n (ideality factor)	Φ_b (Barrier height) eV	R_s (Series resistance)(Ohm)
100	1.07×10^{-10}	0.26	5.79	0.26	1.7×10^7
150	1.60×10^{-10}	0.40	3.58	0.39	3.3×10^7
200	1.64×10^{-10}	0.54	2.79	0.56	2.2×10^7
250	6.19×10^{-10}	0.66	3.43	0.67	1.9×10^7
300	1.63×10^{-9}	0.78	2.56	0.78	6.9×10^7
350	8.72×10^{-9}	0.87	1.88	0.93	4.1×10^5
400	1.00×10^{-8}	1.00	2.49	1.05	1.8×10^7
450	2.13×10^{-8}	1.10	3.33	1.11	1.2×10^6
500	1.63×10^{-7}	1.15	2.35	1.69	1.7×10^5

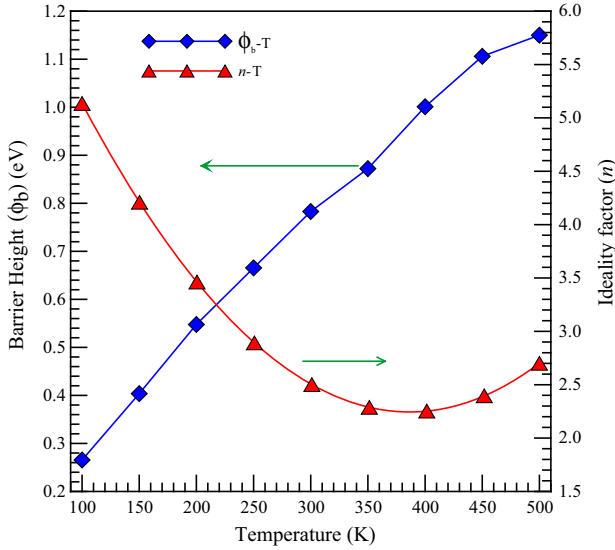


Fig. 6. The temperature dependence of the values of barrier height and ideality factor.

0.05–0.2 V. The temperature dependent profiles of the n and Φ_b values of the Al/ATSP/ p -Si Schottky diode are shown in Fig. 6. The n values were found to be from 5.79 to 1.88 at different temperatures.

According to previous research, the n values increased with decreasing temperature^{32–35} but in this case, the n values decreased. Normally, n is equal to 1 in an ideal diode. However, n values usually are larger than unity for non-ideal diodes depending on interface states, barrier inhomogeneities and interfacial native oxide or polymer layers.^{19,36–39} In this study, the n values were determined different values under various temperature measurements. While the n value is 5.79 at 100 K, 2.35 at 500 K and 2.56 at room temperature. The smallest ideality factor value is 1.88 at 350 K. According to these results, the ATSP layers can be used in diode applications at low and high temperatures.

The current transport mechanism (CTM) can be examined from the nkT versus kT plot. Figure 7 shows the nkT versus kT plot of the Al/ATSP/ p Si Schottky diode at 100–500 K temperature range. There are two lines such as the red line and blue line in Fig. 7. The ideality factor should be “1” (red line) for ideal Schottky diodes but the experimental result is the blue line. The two lines are not parallel. The experimental and theoretical analysis support that the CTM is not only inspected by TE theory but also checked by thermionic field emission (TFE) mechanism for a Schottky diode.⁴⁰

The other method for calculation of the R_s and Φ_b is Norde’s method and given by following equation^{41,42}:

$$F(V) = \frac{V}{q} - \frac{kT}{q} \ln\left(\frac{I(V)}{AA^*T^2}\right), \quad (5)$$

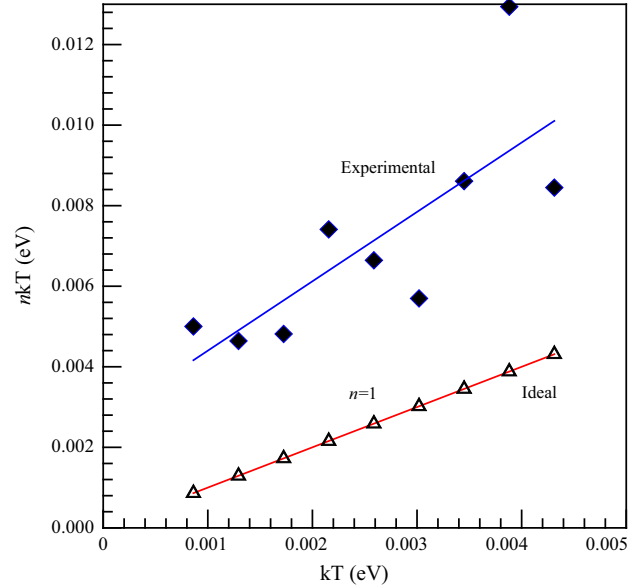


Fig. 7. The nkT versus kT graph of the Al/ATSP/ p type Si Schottky diode.

where γ is a integer greater than the determined n value. I is current. R_s and Φ_b values can be extracted as from the below equations:

$$\Phi_b = F(V) + \frac{V_0}{q} - \frac{kT}{q}, \quad (6)$$

$$R_s = \frac{kT(-n)}{qI}. \quad (7)$$

When the minimum of F versus V plot is examined. The value of Φ_b can be calculated from Eq. (6), where $F(V_0)$ is the minimum point of $F(V)$ and V_0 is the corresponding voltage. Figure 8 displays the $F(V)$ - V plots of the Al/ATSP/ p Si Schottky diode for various temperatures, and the calculated Φ_b and R_s values are listed for wide range temperatures from 100 K to 500 K. As can be seen in Table I, the values of the Φ_b are not the same, when they are compared to the value obtained from the forward bias $\ln I$ - V and Norde’s method. According to Norde’s method results, the values of the Φ_b decreased from 1.69 eV to 0.26 eV with decreasing temperature. The values of R_s increased with decreasing temperature. The higher R_s values can be attributed that the electron carriers decreased with decreasing temperature.⁴³

Due to space charge injection on interface layer at higher forward-bias voltage, this behavior can be attributed to the decrease of the exponentially increasing rate in current.^{44–46}

The other electrical characterization of the Al/ATSP/ p Si Schottky diode is Capacitance–Conductance–Voltage measurements. The capacitance–voltage (C - V) plots of the Al/ATSP/ p Si Schottky diode are indicated in Fig. 9 for changing frequency from 10 kHz to 1600 kHz. The capacitance values

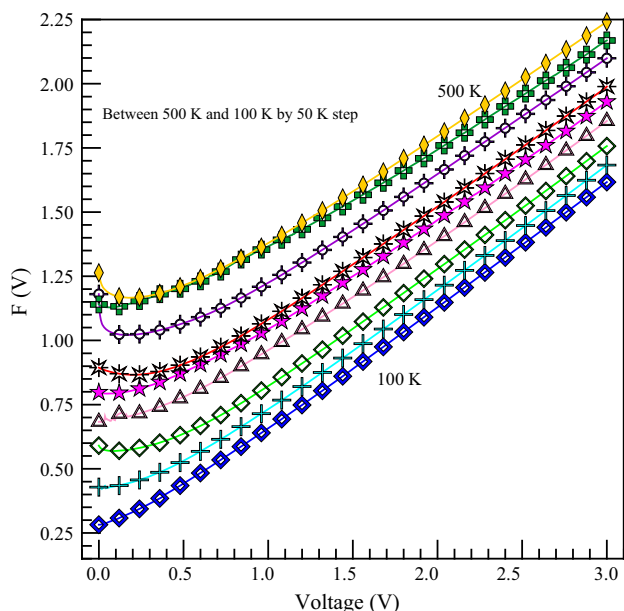


Fig. 8. Norde plot of the Al/ATSP/p-Si Schottky diode as a function of temperature.

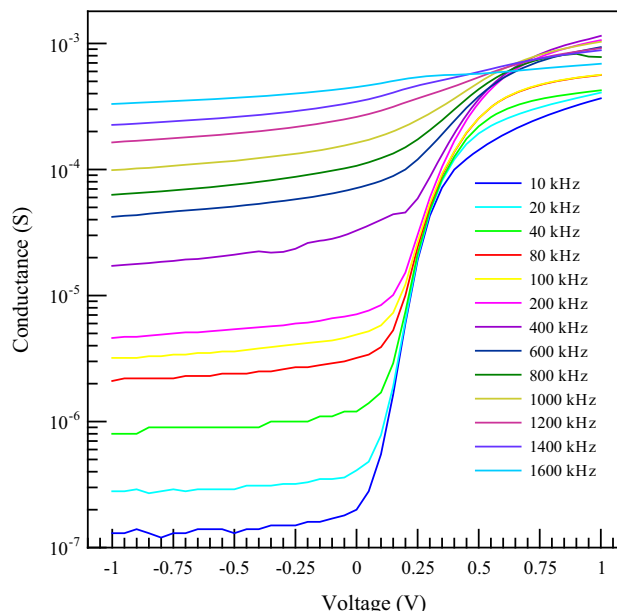


Fig. 10. The $G-V$ characteristic of the Al/ATSP/p-Si Schottky Diode.

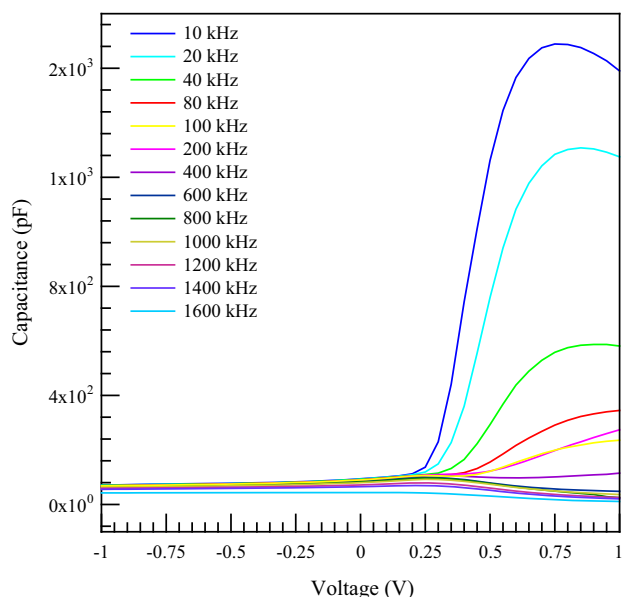


Fig. 9. The $C-V$ characteristic of the Al/ATSP/p-Si Schottky Diode.

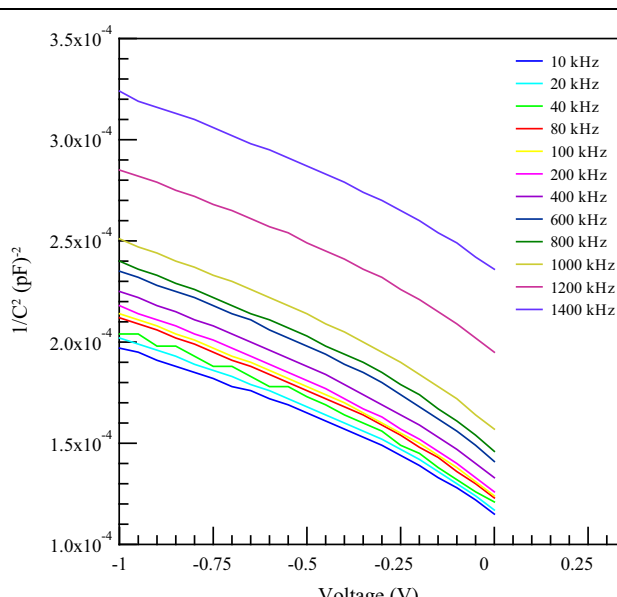


Fig. 11. The $C^{-2}-V$ characteristic of the Al/ATSP/p-Si Schottky Diode.

decreased with increasing frequency and are shown as peaks at the accumulation region. The capacitance values did not change until 0.2 V. After this voltage value, the capacitance values increased with increasing voltage. For each frequency, the capacitance measurements have maximum peaks. These peak positions shifted towards the depletion region. Due to the N_{ss} and R_s effect, doping concentration and the magnitude of polarization decrease cannot follow the ac signal at higher frequency.⁴⁷⁻⁴⁹ So, the capacitance peaks decreased at higher frequencies.

Figure 10 shows the conductance-voltage ($G-V$) plot of the Al/ATSP/p-Si Schottky diode for various frequency and applied voltage at 300 K. The G

values increased from -1.0 V to 1.0 V at each frequency, as can be seen in Fig. 10. Furthermore, the value of G decreased with decreasing frequency at applied bias voltage. The conductance values of the device did not alter in any region such as inversion and depletion region at low frequency. It can be said to be the opposite of this situation at high frequency. This change in conductance is attributed to interface states.^{50,51}

Fermi energy (E_F), donor concentration (N_a), maximum electric field (E_m), Φ_b and interface states (N_{ss}) were calculated by using $C-G-V$ data. For

Table II. The electrical parameters of Al/ATSP/p-Si Schottky diode for various frequencies

f (kHz)	N_a (cm^{-3}) (10^{15})	V_d (V)	E_F (eV)	$\Delta\Phi_b$ (eV)	Φ_b (eV)	E_m (V/m) (10^4)	N_{ss} ($\text{eV}^{-1} \text{cm}^{-2}$)	R_s (Ω)
10	2.426	0.305	0.175	0.0131	0.467	1.437	5.06×10^9	986.9
20	2.347	0.345	0.176	0.0135	0.508	1.510	5.07×10^9	965.5
40	2.318	0.355	0.176	0.0135	0.518	1.525	7.60×10^9	1461.0
80	2.230	0.375	0.177	0.0135	0.539	1.518	10.1×10^9	1150.2
100	2.204	0.385	0.177	0.0136	0.549	1.531	12.4×10^9	1176.9
200	2.155	0.386	0.178	0.0136	0.550	1.535	18.1×10^9	481.6
400	2.147	0.465	0.178	0.0143	0.629	1.694	20.6×10^9	471.9
600	2.136	0.555	0.178	0.0149	0.719	1.854	30.1×10^9	648.3
800	2.140	0.625	0.178	0.0154	0.788	1.975	34.1×10^9	616.1
1000	2.124	0.726	0.178	0.0160	0.888	2.125	42.1×10^9	635.5
1200	2.204	1.225	0.177	0.0185	1.385	2.835	56.1×10^9	597.1
1400	2.269	1.726	0.176	0.0203	1.882	3.424	65.7×10^9	693.7

these calculations, the C^{-2} - V graphs are plotted and given in Fig. 11.

The calculated electrical parameters were tabulated in Table II. The values of the N_{ss} changing are calculated with following formula^{5,51,52}:

$$N_{ss} = \frac{2}{qA} \frac{(G_m/\omega)_{\max}}{((G_m/\omega)_{\max}/C_{0x})^2 + (1 - C_m/C_{0x})^2}, \quad (8)$$

where A is contact area and ω is angular frequency. C_m and G_m represent measured capacitance and conductance, C_{0x} is oxide capacitance for the accumulation region.

According to Table II, N_a decreased with increasing frequency and the other electrical parameters of the device such as V_d , E_F , Φ_b and E_m increased with increasing frequency. Although there were no serious changes, the value of N_{ss} increased with increasing frequency. This can be attributed to the conductivity of the device.⁵³ The value of R_s can be obtained from the C^{-2} - V plot and calculated following formula⁵⁴:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}. \quad (9)$$

The values of R_s increased with increasing frequency up to 100 kHz. The value of R_s exhibited a maximum peak at 100 kHz. Beyond this frequency, the value of R_s decreased with increasing frequency because of the interface state.⁵⁵

CONCLUSION

The Al/ATSP/p-Si MPS type Schottky diode was fabricated using ATSP organic interfacial materials. The AFM and SEM images were confirmed effective and with a homogenous ATSP interfacial layer. The I - V measurements were used to calculate some basic electrical parameters at various temperatures. The n and Φ_b values were calculated based on the TE theory and Norde method. The I - V characteristics of the device revealed that the Al/ATSP/p-Si

device behaved close to ideal device performance at high temperature. In addition to I - V characteristics, the capacitance and conductance measurements were taken to better understand the electrical properties of ATSP interfacial layer at various frequencies. The capacitance values of the Al/ATSP/p-Si Schottky diode increased with decreasing temperature. On the other hand, the interface states increased with increasing frequency. The electrical analysis results highlighted that the ATSP interfacial layer can be used in space technologies and electronic devices due to its endurance in the wide range temperature changes.

REFERENCES

1. R.T. Tung, *Appl. Phys. Lett.* 58, 2821 (1991).
2. J. Osvald and E. Burian, *Solid-State Electron.* 42, 191 (1998).
3. O.S. Cifci, M. Bakir, J.L. Meyer, and A. Kocyigit, *Mater. Sci. Semicond. Process.* 74, 175 (2018).
4. L.W. Lim, F. Aziz, F.F. Muhammad, A. Supangat, and K. Sulaiman, *Synth. Met.* 221, 169 (2016).
5. C. Tozlu and A. Mutlu, *Synth. Met.* 211, 99 (2016).
6. F. Yakuphanoglu and B.F. Şenkal, *J. Phys. Chem. C* 111, 1840 (2007).
7. H. Wang, J.-H. Hsu, G. Yang, and C. Yu, *Adv. Mater.* 28, 9545 (2016).
8. P. Ghorai, A. Dey, P. Brandão, J. Ortega-Castro, A. Bauza, A. Frontera, P.P. Ray, and A. Saha, *Dalton Trans.* 46, 13531 (2017).
9. K. S. Kang, Y. Chen, H. K. Lim, K. Y. Cho, K. J. Han, and J. Kim, *Thin Solid Films* (2009).
10. Ö. Tüzün Özmen and E. Yağlıoğlu, *Mater. Sci. Semicond. Process.* 26, 448 (2014).
11. C.H. Chang, C.J. Hsu, and C.C. Wu, *Org. Electron. Phys. Mater. Appl.* 48, 35 (2017).
12. A. Valletta, M. Rapisarda, S. Calvi, G. Fortunato, M. Frasca, G. Maira, A. Ciccazzo, and L. Mariucci, *Org. Electron. Phys. Mater. Appl.* 41, 345 (2017).
13. Y. Cho, P.J. Jeon, J.S. Kim, and S. Im, *Org. Electron. Phys. Mater. Appl.* 40, 24 (2017).
14. A. Sutrisno, *R. Soc. Chem.* 8, 4946 (2018).
15. D. Frich, K. Goranov, L. Schneggenburger, and J. Economy, *Macromolecules* 9297, 7734 (1996).
16. A. Kocyigit, M. Bakir, O.S. Cifci, B. Enders, I. Jasiuk, and M.H. Nayfeh, *Eur. Polym. J.* 103, 351 (2018).
17. M. Bakir, J.L. Meyer, J. Economy, and I. Jasiuk, *Polymer* 123, 311 (2017).

18. M.E. Aydin, F. Yakuphanoglu, J.H. Eom, and D.H. Hwang, *Phys. B* 387, 239 (2007).
19. Simon M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, 1979).
20. W. R. Rhoderick EH, *Metal–Semiconductor contacts*, 2nd ed. (Oxford, Caledron, 1998).
21. Ş. Karataş, Ş. Altındal, A. Türüt, and A. Özmen, *Appl. Surf. Sci.* 217, 250 (2003).
22. M. Cakar, Y. Organer, and A. Turut, *Synth. Met.* 126, 213 (2002).
23. V.R. Reddy, M.S.P. Reddy, A.A. Kumar, and C.J. Choi, *Thin Solid Films* 520, 5715 (2012).
24. I.S. Yahia, A.A.M. Farag, F. Yakuphanoglu, and W.A. Farooq, *Synth. Met.* 161, 881 (2011).
25. O. Çiçek, H. Uslu Tecimer, S. O. Tan, H. Tecimer, I. Orak, and S. Altındal, *Compos. Part B Eng.* 113, 14 (2017).
26. A. B. Selçuk, S. Bilge Ocak, F. G. Aras, and E. Oz Orhan, *J. Electron. Mater.* 43, 3263 (2014).
27. T. Tunç and M. Gökçen, *J. Compos. Mater.* 46, 2843 (2012).
28. M. Yıldırım and A. Kocyigit, *J. Alloy. Compd.* 768, 1064 (2018).
29. O.S. Cifci, A. Kocyigit, and P. Sun, *Superlattices Microstruct.* 120, 492 (2018).
30. L.D. Rao and V.R. Reddy, *AIP Conf. Proc.* 120020, 120020 (2016).
31. L.W. Lim, F. Aziz, F.F. Muhammad, A. Supangat, and K. Sulaiman, *Synth. Met.* 221, 169 (2016).
32. M. Das, J. Datta, A. Dey, S. Halder, S. Sil, and P. Pratim, *Mater. Lett.* 204, 184 (2017).
33. K. Moraki, S. Bengi, S. Zeyrek, M.M. Bulbul, and S. Altındal, *J. Mater. Sci. Mater. Electron.* 28, 3987 (2017).
34. I. Jyothi, V. Janardhanam, H. Hong, and C. Choi, *Mater. Sci. Semicond. Process.* 39, 390 (2015).
35. Ş. Karataş, Ş. Altındal, A. Turut, and M. Cakar, *Phys. B* 392, 43 (2007).
36. V. Rajagopal Reddy, D. Sri Silpa, H.-J. Yun, and C.-J. Choi, *Superlattices Microstruct.* 71, 134 (2014).
37. Ş. Aydoğan, K. Çınar, H. Asil, C. Coşkun, and A. Türüt, *J. Alloy. Compd.* 476, 913 (2009).
38. F. Yakuphanoglu, Y. Caglar, M. Caglar, and S. Ilican, *Mater. Sci. Semicond. Process.* 13, 137 (2010).
39. S. Sharma and C. Periasamy, *Superlattices Microstruct.* 73, 12 (2014).
40. A. Guzel, S. Duman, N. Yildirim, and A. Turut, *J. Electron. Mater.* 45, 2808 (2016).
41. K.E. Bohlin, *J. Appl. Phys.* 60, 1223 (1986).
42. H. Norde, *J. Appl. Phys.* 50, 5052 (1979).
43. A. Karabulut, I. Orak, S. Canlı, N. Yildırım, and A. Türüt, *Phys. B* 550, 68 (2018).
44. A.M. Cowley and S.M. Sze, *J. Appl. Phys.* 36, 3212 (1965).
45. Y. Zhu, Y. Ishimaru, N. Takahashi, and M. Shimizu, *IEEE Trans. Electron Devices* 45, 2032 (1998).
46. Ş. Karataş, N. Yildirim, and A. Türüt, *Superlattices Microstruct.* 64, 483 (2013).
47. D. Korucu, A. Turut, and R. Turan, *Mater. Sci. Semicond. Process.* 16, 344 (2013).
48. T. Asar and S. Özçelik, *J. Alloy. Compd.* 628, 442 (2015).
49. H. Dogan, N. Yildırım, İ. Orak, S. Elagöz, and A. Turut, *Phys. B* 457, 48 (2015).
50. H.G. Çetinkaya, Ö. Sevgili, and Ş. Altındal, *Phys. B* 560, 91 (2019).
51. A. Kocyigit, M. Yildırım, A. Sarılmaz, and F. Ozel, *J. Alloy. Compd.* 780, 186 (2019).
52. Ç. Bilkın, Ş. Altındal, and Y. Azizian-Kalandaragh, *Phys. B* 515, 28 (2017).
53. I. Taşcıoğlu, M. Soylu, Ş. Altındal, A.A. Al-Ghamdi, and F. Yakuphanoglu, *J. Alloy. Compd.* 541, 462 (2012).
54. E. H. N. J. R. Brews, *MOS (Metal Oxide Semiconductors) Physics and Technology by E. H. Nicollian and J. R. Brews* (1982).
55. A. Duangrawa, N. Promros, A. Nopparuchikun, P. Onsee, S. Teakchaicum, and P. Sittimart, *J. Nanosci. Nanotechnol.* 18, 1841 (2017).

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.