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High Performance Organic Thin Film Transistors Using Pentacene-Based Rare-Earth Oxide Bilayer Gate Dielectric

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High-k dielectrics, neodymium oxide (Nd_2O_3) and lanthanum oxide (La_2O_3) are regarded as useful materials to reduce the operating voltage of organic thin film transistors (OTFTs). However, the high-k dielectrics often have the drawback of high interface trap density leading to high leakage current and low carrier mobility. Here, a bilayer La_2O_3/Nd_2O_3 gate dielectric for OTFTs is employed to address the issues. A top contact pentacene-based organic thin film transistor is exhibiting a variation in carrier mobility as the thickness of Nd_2O_3 changes from 100 nm to 175 nm. Compared to the pentacene thin film transistor with solely 118 nm thick La_2O_3 gate dielectric, the OTFTs with the bilayer La_2O_3/Nd_2O_3 (118 nm/150 nm) gate dielectric improves the threshold voltage from − 0.42 V to − 1.1 and V, the carrier mobility from 0.54 cm^2/Vs to 1.08 cm^2/Vs. These bilayer devices produced the current on–off ratio of 2.4×10^5 and the subthreshold slope of 0.5 V/decade. The OTFT device exhibits good stability under a low voltage bias-stress effect. The OTFTs are investigated in the atomic force microscope to understand the dielectric–pentacene interface to verify the improved OTFT parameters. The morphology and structure of the La_2O_3/Nd_2O_3 bilayer dielectric films are studied using a field emission scanning electron microscope and x-ray diffraction techniques.

Key words: Bilayer dielectric, rare earth oxides, bilayer thickness, carrier mobility, bias-stress, organic thin film transistors

INTRODUCTION

Organic thin film transistors (OTFTs) have gained rapid interest in the recent years in the development of low-cost electronic applications including RF-ID technologies, sensors, light-emitting diodes (LEDs), liquid crystal/OLED display backplane circuitry and integrated optoelectronic devices.[1–3] The performance parameters that characterize OTFTs, e.g., the carrier mobility (μ), current on/off ratio (I_{on}/I_{off}) and threshold voltage (V_T) were significantly improved in recent years.[4] Achieving considerable carrier mobility and low threshold voltage are the main focal points in the development of OTFTs.[5–8] OTFT with a small threshold voltage enables wearable electronics powered by a battery for low power consumption.[9,10]

The performance of OTFTs is affected by the gate dielectric surface morphology. The rough dielectric surface leads to high trap density resulting in low carrier mobility in the OTFT. A high-quality OTFT is achievable by improving the surface roughness of the gate dielectric.[11–13] The low threshold voltage is a desired property of OTFTs. There are many approaches to reduce threshold voltage and to improve the performance of pentacene OTFT with high-k inorganic dielectric materials.[14–16] HfO_2, La_2O_3, Nd_2O_3, TiO_2, SiO_2 are some commonly used high-k inorganic dielectric materials.[16–20] Rare earth oxide materials, La_2O_3, and Nd_2O_3 (k value of 27 and 11) are not explored much as bilayer dielectrics in pentacene OTFT. These oxide materials have a higher k value than those of HfO_2–SiO_2, but these are ignored as bilayer dielectrics in

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OTFTs compared to organic–organic and inorganic–organic bilayer dielectrics. We have recently reported an inorganic–organic bilayer approach with Nd_2O_3 and cross-linked PVA to achieve a high performing pentacene-based OTFT.[16] In the present study, La_2O_3/Nd_2O_3 bilayer gate dielectrics are employed to fabricate pentacene-based OTFTs. Effect of thickness variation of the Nd_2O_3 gate dielectrics is studied to obtain a low-voltage OTFT. Moreover, we have examined the stability of the devices under low voltage bias-stress for extended hours (h).

EXPERIMENTAL

Device Fabrication

In this work, we have used a top-contact bottom-gate device geometry for all the devices. The Corning Eagle 2000 glass substrate is cleaned ultrasonically with acetone, deionized water and dried with a hot air gun and used for fabrication of the OTFTs. The OTFT structure is presented in Fig. 1.

The device fabrication started with the deposition of patterned Aluminium (Al) with a thickness of 100 nm as a gate electrode on the glass substrate. A layer of 118 nm thick La_2O_3 (MW = 325.81 g/mol) and layers of variable thickness (100 nm, 150 nm and 175 nm) of Nd_2O_3 (MW = 336.48 g/mol) are deposited by a vacuum deposition method on the top of Al layer, respectively. The oxides are properly degassed in vacuum for a long time prior to deposition. A layer of Pentacene (Aldrich, 99.9% purity) of 45 nm thickness is thermally deposited over the gate dielectric bilayer at a rate of 0.6–0.8 Å s^{-1} and a substrate temperature of 27°C under high vacuum of 0.79×10^{-6} kPa. The substrate temperature is kept at 27°C during deposition because at that temperature the best polycrystalline thin films of pentacene can be grown.[21,22] Finally, 80 nm thick gold (Au), used as a source/drain electrode, is thermally deposited on top of pentacene at a rate of 0.5 Å s^{-1} with a shadow mask of defined channel length (L) and channel width (W) of 50 μm and 1000 μm, respectively. All the layer thicknesses are measured using a thickness profilometer. The prepared OTFT structures are annealed in vacuum at 100°C for 5 h.

RESULTS AND DISCUSSION

Device Measurements and Characterization

A source meter (2400SMU) was used to measure the electrical characteristics of the pentacene devices prepared in the present work. The ambient atmosphere was used to characterize all the electrical parameters. Metal-insulator-metal (MIM) capacitors were fabricated on the glass substrate using single dielectric La_2O_3 and La_2O_3/Nd_2O_3 bilayer dielectric with 100 nm, 150 nm and 175 nm Nd_2O_3 thicknesses to illustrate the effect of Nd_2O_3 layer over the La_2O_3 gate dielectric.

Figure 2 represents the current density–electric field (J–E) characteristics of the MIM structure. The capacitance and leakage current was measured for the MIM configuration. The single La_2O_3 layer exhibited a high leakage current whereas addition of Nd_2O_3 layer of thickness 150 nm over La_2O_3 layer resulted in a significant reduction of leakage current($< 10^{-7}$A/cm^2).

Figure 3 represents the typical transistor output characteristics in the operating range of 0 V to − 10 V. The figure indicates good linear/saturation behavior for all the devices. The transfer curves are drawn at the saturation regime with the drain-source voltage (V_D) of − 7 V (Fig. 4).

From the $I_D^{1/2}$ versus V_G curves, we estimated the threshold voltage (V_T) of the devices by extending the linear portion of the graph to the V_G axis. The threshold voltage is dependent on the interface quality of the semiconductor/dielectric interface, and if the gate dielectric roughness is high, the threshold voltage is also high and vice-versa.[23] The bilayer OTFTs (118–150 nm) exhibited threshold voltage of − 1.1 V, while the single layer La_2O_3 (118 nm–0 nm) showed − 0.42 V. The low threshold

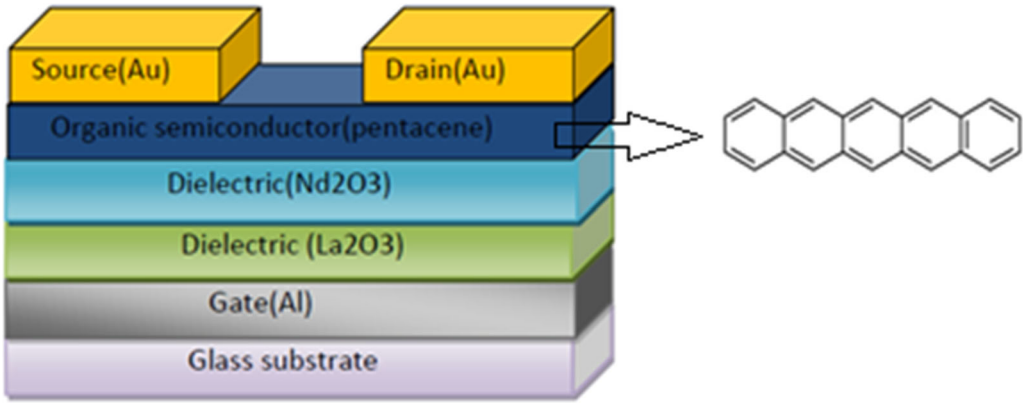

Fig. 1. OTFT device structure with top-contact bottom-gate geometry.

voltage in case of the bilayer device may be due to the Nd_2O_3 layer deposited over the La_2O_3 layer that leads to a much smoother surface and low traps in the bilayer device. The various parameters evaluated in this work are shown in Table I.

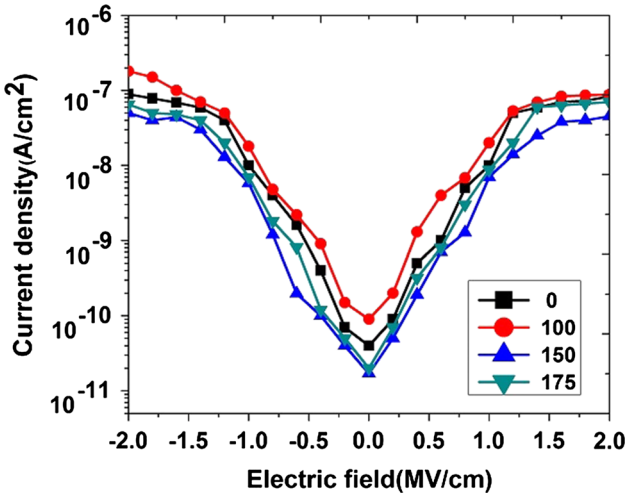

Fig. 2. Current density (J) versus electric field (E) of (118 nm) La_2O_3/(0 nm, 100 nm, 150 nm, 175 nm) Nd_2O_3 bilayer dielectric.

First, we calculated the device mobility in the saturation regime using the I_D expression[8] in Eq. 1.

$$I_{DS} = \frac{W\mu C_i}{2L}(V_G - V_T)^2, \quad (1)$$

where C_i is the capacitance per unit area of the bilayer dielectrics. The total C_i for the bilayer dielectrics is described as two capacitances in series

$$\frac{1}{C_i} = \frac{1}{C_1} + \frac{1}{C_2}, \quad (2)$$

where C_1 and C_2 are the capacitances per unit area of the La_2O_3 and Nd_2O_3 layers. The C_i value for the La_2O_3/Nd_2O_3(150 nm) bilayer was found to be 28.45 nF/cm^2 which is the highest among all devices. The carrier mobility tends to increase with a high value of capacitance of the dielectric layers.[24,25]

Thickness variation (0 nm, 100 nm, 150 nm, 175 nm) of the Nd_2O_3 layer was considered to optimize the carrier mobility. The device with La_2O_3(118 nm)/Nd_2O_3(150 nm) exhibited carrier mobility of 1.08 cm^2/Vs which is highest among all the devices. The single layer La_2O_3(118 nm–0) showed low carrier mobility of 0.54 cm^2/Vs. The mobility of the devices increased with the increase

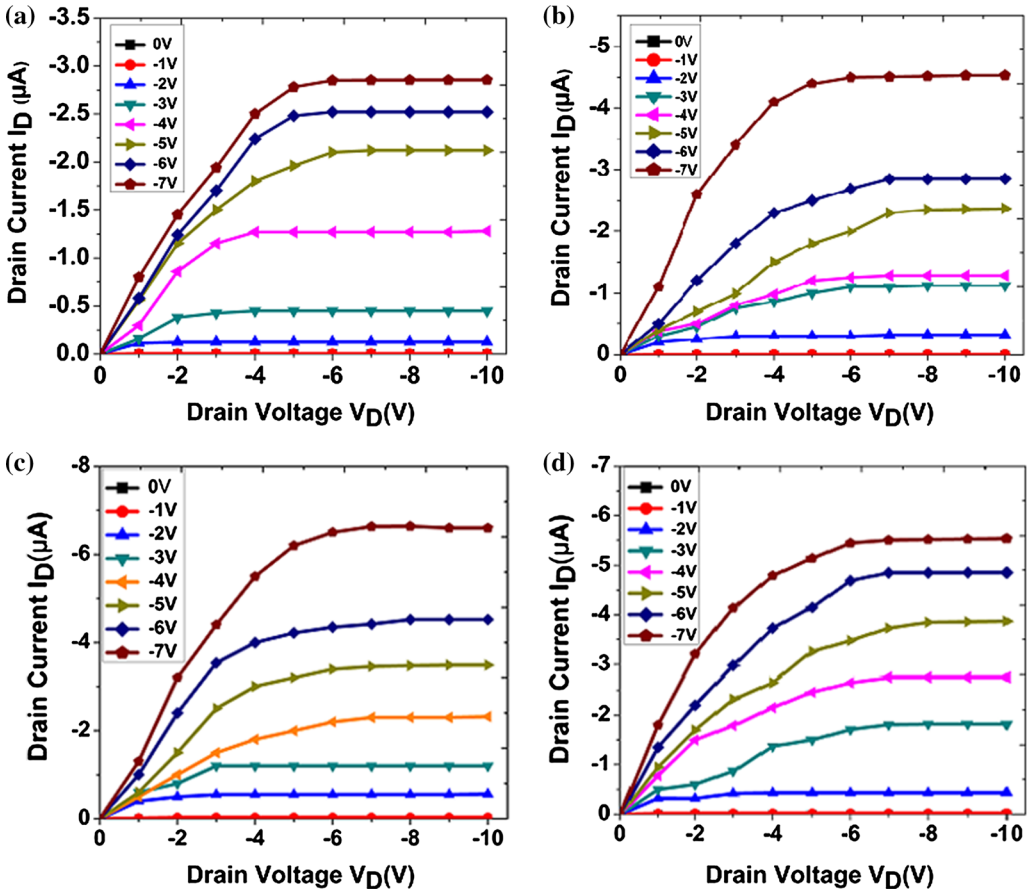

Fig. 3. (a–d) I_D versus V_D graphs of (118 nm) La_2O_3/(100 nm, 150 nm, 175 nm) Nd_2O_3 bilayer dielectric for V_G = 0 to − 7 V.

in thickness of the Nd_2O_3 layer (0–150 nm). Further increase in thickness of the Nd_2O_3 layer did not produce appreciable improvement in mobility (Table I). The increase in carrier mobility of the bilayer device is due to the deposition of the layer of Nd_2O_3 over the hydrophilic surface of La_2O_3 and the latter being prone to moisture attack can easily make large traps in the device. Fewer traps in the device influence mobility.[28] The top surface chemical activity of La_2O_3 is well reported in the literature.[26,27] In the atomic force microscopic (AFM) studies, the bare La_2O_3 surface appeared non-uniform. The root-mean-square (RMS) roughness of the first layer was calculated to be 1.82 nm (Fig. 5a) while that of the second layer produced a much smoother surface with RMS roughness of 0.94 nm (Fig. 5b). Table II represents a comparison of the carrier mobility obtained with the pentacene device in the present work with the published literature. The findings are found superior to those reported earlier (Table II).

We determined the subthreshold slope (S) from the transfer characteristics by using Eq. 3[8]:

$$S = \left[\frac{\mathrm{d}(\log I_\mathrm{D})}{\mathrm{d}V_\mathrm{G}}\right]^{-1}. \quad (3)$$

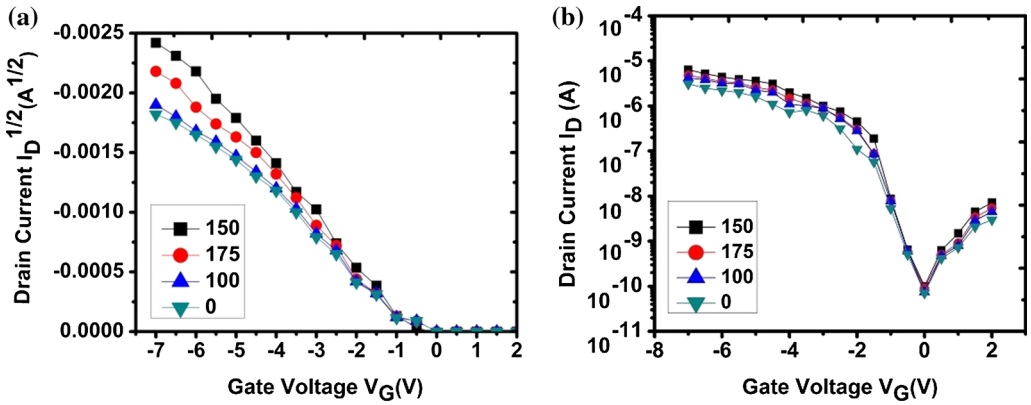

Fig. 4. (a–b) Transfer curves of the (118 nm) La_2O_3/(0 nm, 100 nm, 150 nm, 175 nm) Nd_2O_3 OTFT devices at $V_{DS} = -7$ V.

Table I. The summary of the device conditions and electrical performance of the pentacene-based OTFTs with bilayer dielectrics

La_2O_3/Nd_2O_3 (nm)	μ (cm^2/Vs)	V_T (V)	$I_{on/off}$	S (V/decade)
118–0	0.54 ± 0.09	− 0.42	1.8×10^4	0.62
118–100	0.69 ± 0.12	− 0.32	1.2×10^4	0.7
118–150	1.08 ± 0.16	− 1.1	2.4×10^5	0.5
118–175	0.62 ± 0.15	− 0.5	7.4×10^4	1.4

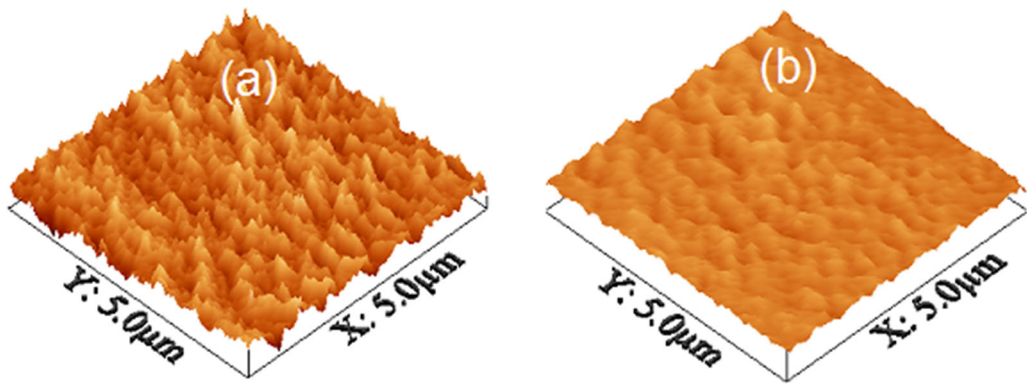

Fig. 5. (a, b) AFM images of pentacene over (a) La_2O_3 single dielectric(118 nm–0), (b) La_2O_3/Nd_2O_3(118–150 nm) bilayer dielectric.

Table II. Comparison of the results of the present work with the previously reported pentacene-based OTFTs with rare earth oxides dielectrics

Dielectric	Mobility [μ (cm^2/Vs)]	Threshold voltage [V_T (V)]	Current on–off ratio [$I_{on/off}$]	Subthreshold slope [S (V/decade)]	References
Nd_2O_3	0.13	− 2.2	1.7×10^4	–	36
Nd_2O_3	0.5	− 3.5	10^6	1.2	37
La_2O_3	0.02	− 1.8	3×10^4	0.3	38
La_2O_3	0.00065	2	–	2	39
ZnO/La_2O_3	0.58	4	10^6	1	40
HfO_2	0.22	− 1.25	10^3	0.59	41
La_2O_3/Nd_2O_3	1.08	− 1.1	2.4×10^5	0.5	Present work

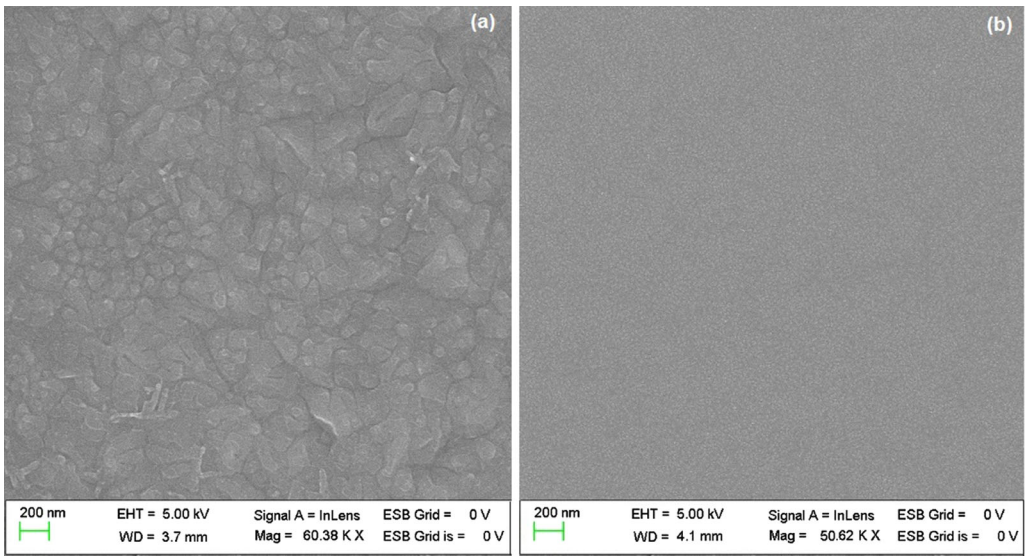

Fig. 6. (a, b) FE-SEM images of pentacene over (a) La_2O_3 single dielectric (118 nm–0), (b) La_2O_3/Nd_2O_3(118–150 nm) bilayer dielectric.

The subthreshold slope (S) for the device with (118–150 nm) thickness was found to be 0.5 V/decade which is the lowest among all the devices.Equation 4 calculates the current on-off ratio[8] of the devices

$$\frac{I_{on}}{I_{off}} = \frac{C_i \mu (V_G - V_T)^2}{\sigma d V_D}, \quad (4)$$

where σ is the conductivity, d is the channel thickness of the bilayer gate dielectric, V_D is the drain-source voltage and μ is the carrier mobility, respectively. The current on–off ratio obtained for the combination (118–150 nm) is 2.4×10^5 which is the highest among all devices (Table II). Depositing Nd_2O_3 of thickness 150 nm layer over La_2O_3 improves this value.

The field emission scanning electron micrographs (FE-SEM) of pentacene over the single and the bilayer dielectrics are shown in Fig. 6a and b. The bilayer device produced a smooth surface, and the single layer device produced a relatively rough surface. This may be attributed to the deposition of the Nd_2O_3 layer on the La_2O_3 layer that provides a smoother surface. The smooth surface may be assumed to have low surface energy and, so, the pentacene film on the La_2O_3/Nd_2O_3 bilayer has low surface energy compared to the La_2O_3 layer.[29] The single layer La_2O_3 and La_2O_3/Nd_2O_3 bilayer gate dielectric OTFTs were further analyzed by AFM technique. The observation of the pentacene surface over single La_2O_3 and La_2O_3/Nd_2O_3 bilayer dielectric surface in AFM complements the SEM micrographs. The smooth surface of the dielectric layer leads to low leakage current which, in turn, enhances the carrier mobility of the device. We have recently reported Nd_2O_3-crosslinked PVA bilayer dielectric OTFT with a similar observation in AFM.[16] Thus, it can be concluded that the smooth surface of the bilayer device reduces the leakage current and enhances the carrier mobility.[16,30]

Figure 7 presents the x-ray diffraction (XRD) image of the pentacene on the bilayer. The peak

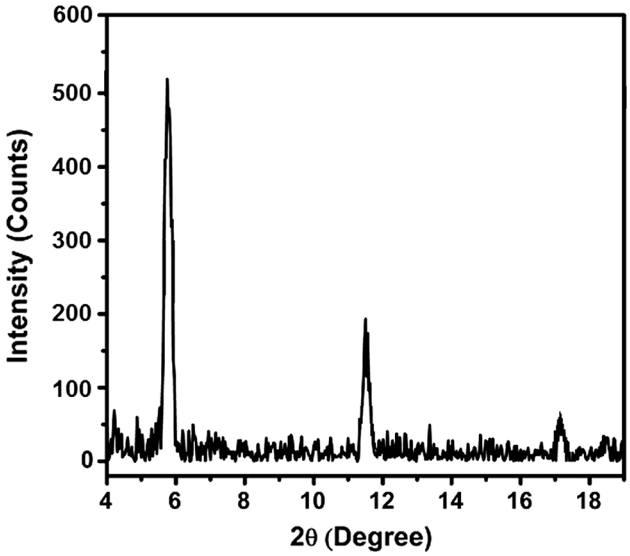

Fig. 7. XRD image of pentacene over La_2O_3/Nd_2O_3dielectric.

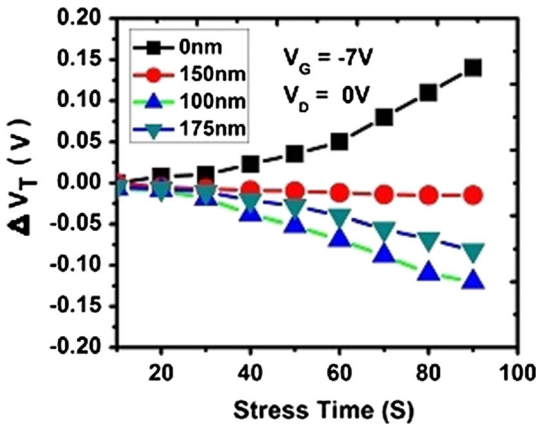

Fig. 8. Threshold voltage shift (ΔV_T) versus stress time (s) at $V_G = -7$ V, $V_D = 0$ V for (118 nm) La_2O_3/(0 nm, 100 nm, 150 nm, 175 nm) Nd_2O_3 OTFT devices.

intensity at a 2θ value of 5.70 represents the crystalline nature of the pentacene.

We have studied the stability of all the devices under low voltage bias-stress for 48 h. The bias-stress effect is mostly due to the trapping of carriers from the gate bias-induced conduction channel into less mobile electronic states. These trap states may be located within the semiconductor, at the semiconductor/dielectric interface or in the gate dielectric. The large shift in threshold voltage (ΔV_T) is found for longer stress time as more carriers are trapped.[31]

Figure 8 indicates the shift in threshold voltage at $V_G = -7$ V and $V_D = 0$ V. The applied negative gate-bias stress resulted in the shift of V_T towards more negative values for the (118 nm) La_2O_3/(100 nm, 175 nm) Nd_2O_3 devices, while the shift of V_T was towards positive values for the 118 nm La_2O_3 layer only. The threshold voltage of the bilayer device with La_2O_3(118 nm)/Nd_2O_3(150 nm) under low voltage bias-stress decreased by only 2% compared to 35% in the case of the single layer dielectric device. All other electrical parameters did not change against the bias-stress for the bilayer device, while all the key electrical parameters for the single layer dielectric changed against the bias-stress. The threshold voltage shift (ΔV_T) due to applied gate bias-stress voltages follow the stretched exponential relation (Eq. 5).

$$\Delta V_T(t) = [V_T(\infty) - V_T(0)]\left[1 - \exp\left(\frac{t}{\tau}\right)^{\beta}\right], \qquad (5)$$

where $V_T(0)$ is the threshold voltage in the unbiased state, $V_T(\infty)$ is the threshold voltage at $t \rightarrow \infty$, τ is the characteristics trapping time of the carriers, and β is the stretched exponential parameter.

These results suggest that the charge trapping at the interface of the gate dielectrics is the dominant factor for the instability of the devices. The negative V_T shift due to the negative gate-bias stress indicates the decrease of mobile holes in the channel via the charge trapping in the gate insulator and semiconductor.[32–34] Our works are in good agreement with the reported literature.[34,35]

The performance of the device described above is analyzed by comparing its OTFT parameters with those reported previously (Table II). It is observed from the table that the bilayer dielectric system presented here is exhibiting superior performance than is the single inorganic layer and other bilayer devices, respectively.

CONCLUSION

Pentacene-based rare earth oxide bilayer dielectric OTFTs were fabricated, and the device performance was evaluated. The superior electrical performance was obtained for the OTFT with a La_2O_3/Nd_2O_3(118 nm/150 nm) bilayer dielectric. This device can operate below -10 V with a sufficient on/off current ratio of 10^5, subthreshold of 0.5 V/decade, a threshold voltage of -1.1 V and carrier mobility of 1.08 cm^2/Vs. The OTFT device exhibited good stability under low voltage bias-stress for an extended period. Thus, our work demonstrates that the rare-earth oxides are the promising gate bilayer dielectric materials for OTFTs.

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