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Multiobjective Optimization of Design of 4H-SiC Power MOSFETs for Specific Applications

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The electrical characteristics of a 4H silicon carbide (4H-SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) have been investigated by using a multiobjective genetic algorithm (MOGA) to overcome the existing tradeoff between main device figures of merit such as the breakdown voltage, drain current, and ON-state resistance. The aim of this work is to achieve an optimized device for a specific application. In particular, without loss of generality, we refer to a dual-implanted MOSFET (DMOSFET) dimensioned for use as a low-power transistor in direct current (DC)–DC converters for solar power optimizers. Typical blocking voltages for these transistors are around 150 V. In this investigation, both analytical and numerical models are used as objective functions in MOGA to determine a set of optimized physical and geometrical device parameters that meet the application constraints while minimizing the ON-state resistance (R_{ON}). The optimized DMOSFET exhibits an R_{ON} value of a few hundred k$\Omega \times \mu m^2$ for different breakdown voltages in the range from 150 V to 800 V.

Key words: 4H-SiC MOSFET, power device, design optimization, ON-state resistance, blocking voltage

INTRODUCTION

During the last decade, use of 4H silicon carbide (4H-SiC)-based metal–oxide–semiconductor field-effect transistors (MOSFETs) for high-power, high-temperature, and switching applications has been widely proposed.[1–5] Thanks to its outstanding physical and electronic properties (i.e., mechanical strength, thermal conductivity, and critical electric field),[6,7] silicon carbide has been recognized worldwide as a promising material to improve device performance in terms of ON-state resistance, breakdown voltage, and switching capabilities. In particular, SiC MOSFETs are widely used as power devices in onboard DC–DC converters for use in specific modules; For example, in Ref. 8, a boost-based converter was proposed, describing the design of a zero-voltage zero-current switch (ZVZCS) suitable for high duty cycle and wide load currents; in Ref. 9, dual-SiC MOSFET modules were designed for use in the electric traction context; in Ref. 10, a dual active bridge (DAB) converter was implemented using 10-kV SiC MOSFETs; in Ref. 11 a high-frequency, 1-kW, 800 V output voltage boost DC–DC converter was developed.

To meet the specific constraints related to modern power electronics, the design of 4H-SiC MOSFETs requires deployment of intensive modeling effort based in turn on numerical, analytical, and empirical calculations, carefully taking into account the different geometrical and physical parameters that affect device performance.[12–15]

Although several studies have dealt with the tradeoff between the electrical characteristics of a MOSFET in 4H-SiC,[15–18] to the best of the authors' knowledge, no investigations on global performance

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optimization based on evolutionary algorithms have been carried out. Such tools are very useful for optimization problems where various objective functions must be treated simultaneously, offering low complexity and reasonable computational time.

To achieve this aim, in the work presented herein, we investigated optimized design of a 4H-SiC dual-implanted MOSFET (DMOSFET) well suited for a specific application by means of a multiobjective genetic algorithm (MOGA).[19] In more detail, starting from combined analytical and numerical analysis of the device current–voltage (I_D–V_{DS}) characteristic, both analytical and numerical models are used as objective functions in MOGA to determine fundamental design parameters that minimize the ON-state resistance of a device dimensioned for a blocking voltage (BV_{DS}) in the range from 150 V to 800 V. Although typical 4H-SiC MOSFETs are designed to support high breakdown voltages ranging from 600 V to 1700 V,[20–22] recent papers have also investigated low-power transistors (in the 100 V to 200 V class) to be used, for example, for photovoltaic module-level applications, enabling operation in harsh conditions with considerable lifetime.[23–28] In fact, smart maximum-power-point tracking converters for photovoltaics should be characterized by BV_{DS} values close to 150 V or less and R_{ON} in the limit of a few hundred kΩ × μm^2. In particular, in Ref. 23, the authors underlined the need to overcome the existing tradeoff between BV_{DS}, I_D, and R_{ON} to design low-voltage 4H-SiC MOSFETs with optimized performance. As mentioned above, without loss of generality, we adopt a genetic algorithm framework to search for the commonly called Pareto-optimal (i.e., nondominated) solution for several physical and geometrical device parameters. The results obtained in terms of R_{ON} are compared with those reported in Ref. 23.

DMOSFET STRUCTURE

A schematic cross-sectional view of the single-cell n-channel 4H-SiC DMOSFET considered herein is shown in Fig. 1, along with the notation adopted to describe the geometry of the different device regions. In particular, W_{cell} is the cell width, L_{ch} is the device channel length, X_{JFET} is the distance between the base regions, W_{drift} is the thickness of the n-drift region, and X_{JP} and X_{N+} are the p-base and n-source depths, respectively.

The source contact shorts the source and the base regions to prevent the switch-on of the parasitic substrate (n^+)–epilayer (n)-base (p)–source (n^+) bipolar junction transistor. Finally, a silicon oxide layer is used to insulate the actual MOS structure.

COMPUTATION METHODOLOGY

Detailed analytical and numerical models are first used to investigate the current–voltage behavior of the DMOSFET. These models are then assumed as objective functions in MOGA to determine the optimized physical and geometrical device parameters for a specific application. The fundamental simulation models are briefly recalled in the following subsections.

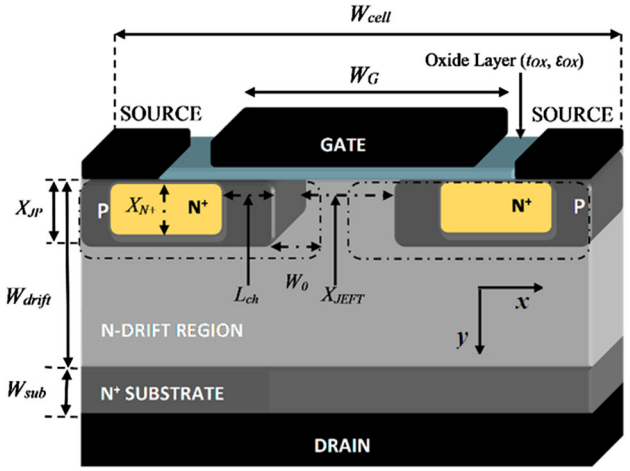

Fig. 1. Cross-sectional view of single-cell n-channel 4H-SiC DMOSFET (drawing not to scale).

Analytical Models

Breakdown Voltage

The breakdown or blocking voltage (BV_{DS}) characteristics of a DMOSFET can be calculated when the device is in a firm OFF-state, i.e., V_G = 0 V with grounded source. The BV_{DS} value is related to the onset of breakdown within the base–drain p-i-n structure as the bias voltage V_{DS} is increased. Assuming that the drift region is in a punchthrough condition, namely totally depleted before breakdown occurs, a first estimate of BV_{DS} is given by[7]

$$BV_{DS} = E_{pn}^{crit} W_{drift} - \frac{qN_{drift}W_{drift}^2}{2\varepsilon_{sc}}, \qquad (1)$$

where E_{pn}^{crit} is the critical electric field that appears somewhere along the border of the p-base/n-drift junction, ε_{sc} is the material permittivity, and N_{drift} is the doping concentration in the drift region. This expression is valid for $W_{drift} \le \varepsilon_{sc} E_{pn}^{crit} q^{-1} N_{drift}^{-1}$; For example, considering typical values for the permittivity of 4H-SiC and a critical electric field of 2 MV/cm, the width of the n-type drift region must be in the limit of 10 μm for $N_{drift} = 1 \times 10^{16}$ cm^{-3}.[7] This result was also calculated in Refs. 29,30 for similar p-i-n structures. The dependence of the electric field on N_{drift} is in the form[31]

$$E_{pn} = 2.49 \times 10^6 (5 - 0.25 \log N_{drift}). \qquad (2)$$

ON-State Resistance

The total ON-state resistance in the device current path is the sum of different terms as follows:

$$R_{ON} = R_{N+} + R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{sub}, \quad (3)$$

where R_{N+} is the source resistance, R_{ch} is the channel region resistance, R_{acc} is the accumulation region resistance relative to the distance X_{JFET} next to the channel (Fig. 1), R_{JFET} refers to the JFET channel portion, R_{drift} is the resistance of the drift region, and R_{sub} is the substrate contribution. In accordance with Fig. 1, appropriate expressions for these terms can be written as[7]

$$R_{ch} = \frac{L_{ch} W_{cell}}{2\mu_{ch} C_{OX}(V_{GS} - V_{TH})}, \quad (4)$$

$$R_{acc} = \frac{X_{JFET} W_{cell}}{4\mu_{acc} C_{OX}(V_{GS} - V_{TH})}, \quad (5)$$

$$R_{JFET} = \frac{\rho_{JFET} X_{JP} W_{cell}}{W_G - 2X_{JP} - 2W_0}, \quad (6)$$

$$R_{drift} = \frac{\rho_{drift} W_{drift} W_{cell}}{W_{cell} - W_G + 2X_{JP} + 2W_0} \ln\left(\frac{W_{cell}}{W_G - 2X_{JP} - 2W_0}\right). \quad (7)$$

Here, in particular, R_{acc} is the gate oxide capacitance, μ_{ch} and μ_{acc} are the doping-dependent carrier mobility in the inversion and accumulation layer, respectively, ρ_{JFET} is the resistivity of the JFET region, and W_0 is the zero-bias depletion width in the JFET region computed as

$$W_0 = \sqrt{\frac{2\varepsilon_{SC} N_A V_{bi}}{qN_{JFET}(N_A + N_{JFET})}}, \quad (8)$$

where N_A and N_{JFET} are the doping concentration in the p-base and JFET region, respectively, and V_{bi} is the built-in potential in the form

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_{JFET}}{n_i^2}\right). \quad (9)$$

Note that, for the sake of simplicity, the resistance contributions R_{N+} and R_{sub} are considered to be negligible in these calculations, because they are relative to heavily doped regions.

Threshold Voltage and Drain Current

The MOSFET threshold voltage (V_{TH}) is defined as the gate bias voltage that ensures the strong inversion regime in the channel region. Its value depends on the doping concentration in the p-base and increases linearly with the gate oxide thickness. A typical expression for V_{TH} is[7]

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_{SC} kTN_A \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right). \quad (10)$$

By neglecting the subthreshold current (i.e., $I_D = 0$ for $V_{GS} < V_{TH}$) and assuming a MOSFET operating point in the triode region (i.e., $V_{DS} \le V_{GS} - V_{TH}$), the drain current can be calculated as[10]

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{L_{ch}} \left[2(V_{GS} - V_{TH})(V_{DS} - I_D R_{ON}) - (V_{DS} - I_D R_{ON})^2\right], \quad (11)$$

where the term $V_{DS} - I_D R_{ON}$ is the drain internal voltage, differing from the terminal voltage by the ohmic contribution.

Finally, for $V_{DS} > V_{GS} - V_{TH}$, we use

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{2L_{ch}} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{DS} - I_D R_{ON})], \quad (12)$$

where λ is an appropriate channel modulation coefficient.

Numerical Framework

Numerical simulations of the DMOSFET were performed by using a commercial two-dimensional (2D) technology computer-aided design (TCAD) physical simulator that provides the solution of Poisson's equation and carrier continuity equations.[32] The physical models and reference parameters included at T = 300 K are summarized in Table I.

They include Shockley–Read–Hall recombination (R_{SRH}),[33] Auger recombination (R_{Auger}),[34] incomplete ionization of impurities ($N_{A,D}^{-,+}$),[35–37] apparent bandgap narrowing ($\Delta E_{gp,n}$),[38] doping-dependent carrier lifetime ($\tau_{n,p}$),[39,40] impact ionization rate ($\alpha_{n,p}$),[41] and low- and high-field carrier mobility ($\mu_{n,p}$).[42–44]

The simulation setup assumed in this work has been used in other recent works of ours,[45–48] where it is also supported by comparison with experimental results obtained on both p^+-i-n and Schottky structures over wide ranges of current and temperature.[49–52]

SIMULATION ANALYSIS

In this section, we develop the background for the MOGA optimization. In particular, the impact of the fundamental design parameters on the main figures of merit of the DMOSFET is investigated by using the reference values listed in Table II as initial entry data for modeling.

Blocking Voltage Characteristics

The device BV_{DS} value is strictly dependent on the n-drift thickness, which determines the distance between the base junction and substrate, namely the difference $W_{drift} - X_{JP}$ in Fig. 1.

In the numerical analysis, BV_{DS} is calculated by considering the device in the OFF-state and gradually raising V_{DS} until the electric field reaches the

Table I. Physical models and reference parameters

$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(-\frac{E_{trap}}{kT}\right)\right)}$	$n_i = 6.7 \times 10^{-11}$ cm^{-3}
$R_{Auger} = (C_{Ap}p + C_{An}n)(np - n_i^2)$	$C_{An} = 5 \times 10^{-31}$ cm^6/s $C_{Ap} = 2 \times 10^{-31}$ cm^6/s
$\tau_{n,p} = \frac{\tau_{0n,p}}{1 + \left(\frac{N}{N_{n,p}^{SRH}}\right)}$	$\tau_{0n} = 500$ ns $\tau_{0p} = 100$ ns $N_{n,p}^{SRH} = 1 \times 10^{30}$ cm^{-3}
	$N_V = 3.29 \times 10^{19}$ cm^{-3} $N_C = 1.66 \times 10^{19}$ cm^{-3}
$N_{A,D}^{-,+} = N_{A,D}\left(\frac{-1 + \sqrt{1 + 4g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}}{2g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}\right)$	$g_v = 4$, $g_c = 2$ $\Delta E_A = 190$ meV $\Delta E_D = 70$ meV
$\alpha_{n,p} = a_{0n,p}\exp\left(-\frac{b_{0n,p}}{E}\right)$	$a_{0n} = 2.5 \times 10^5$ cm^{-1} $a_{0p} = 3.25 \times 10^6$ cm^{-1} $b_{0n} = 1.84 \times 10^7$ V/cm $b_{0p} = 1.71 \times 10^7$ V/cm
$\Delta E_{gp,n} = A_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{2}} + B_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{3}} + C_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{4}}$	$A_p = 1.54 \times 10^{-3}$ $B_p = 1.3 \times 10^{-2}$ $C_p = 1.57 \times 10^{-2}$ $A_n = 1.17 \times 10^{-2}$ $B_n = 1.5 \times 10^{-2}$ $C_n = 1.9 \times 10^{-2}$
$\mu_{n,p} = \mu_{0n,p}^{min} + \frac{\mu_{0n,p}^{max} - \mu_{0n,p}^{min}}{1 + \left(\frac{N}{N_{n,p}^{crit}}\right)^{\delta_{n,p}}}$,	$\mu_{0n}^{min} = 40$ cm^2/V s $\mu_{0p}^{min} = 15.9$ cm^2/V s $\mu_{0n}^{max} = 950$ cm^2/V s $\mu_{0p}^{max} = 125$ cm^2/V s
$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1 + \left(E\frac{\mu_{n,p}}{v_{sat}}\right)^{\kappa_{n,p}}\right]^{\frac{1}{\kappa_{n,p}}}}$	$N_n^{crit} = 2 \times 10^{17}$ cm^{-3} $N_p^{crit} = 1.76 \times 10^{19}$ cm^{-3} $\delta_n = 0.76$, $\delta_p = 0.34$ $k_n = 2$, $k_p = 1$ $v_{sat} = 2 \times 10^7$ cm/s

Table II. DMOSFET reference parameters (Fig. 1)

Silicon oxide thickness, t_{ox} (μm)	0.08
Source thickness, X_{N+} (μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_{JP} (μm)	1.5
Base-to-base distance, X_{JFET} (μm)	7
Epilayer thickness, W_{drift} (μm)	10
Substrate thickness, W_{sub} (μm)	100
Gate width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
Device footprint area (μm^2)	15
n^+-Source doping, N_D (cm^{-3})	1×10^{18}
p-Base doping, N_A (cm^{-3})	1.5×10^{17}
n-Drift doping, N_{drift} (cm^{-3})	1×10^{16}
n^+-Substrate doping, N_{sub} (cm^{-3})	1×10^{19}

threshold of 1.9 MV/cm. The increase of V_{DS}, in fact, is responsible for the expansion of the depletion region to the low-doped side of the p-base/n-drift junction, and the more the depletion region expands, the greater the increase in the electric field. The drain leakage current density, J_D, was kept below 10 mA/cm^2.

Table III. DMOSFET breakdown voltage versus n-drift thickness assuming an electric field threshold of 1.9 MV/cm and $N_{drift} = 1 \times 10^{16}$ cm^{-3}

W_{drift} (μm)	BV_{DS} (V)
10	900
8	800
6	700
4	500
3	350
2	200
1.8	150

For the device described in Table II, we calculate a BV_{DS} of about 900 V. Then, W_{drift} is reduced to 1.8 μm to meet the constraint of a BV_{DS} close to 150 V. Different values of BV_{DS} as a function of W_{drift} are summarized in Table III.

The influence of the n-drift doping concentration on BV_{DS} is also evaluated. In particular, on decreasing the doping concentration N_{drift} from 1×10^{16} cm^{-3} to 1×10^{15} cm^{-3}, a decrease in the critical electric field with a maximum reduction of

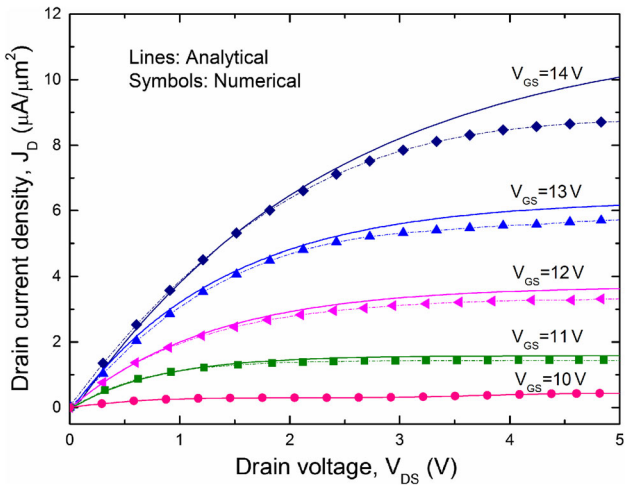

Fig. 2. DMOSFET forward J_D–V_{DS} characteristics at T = 300 K for W_{drift} = 1.8 μm and N_{drift} = 3 × 10^{15} cm^{-3} with other geometrical and electrical parameters as listed in Table II.

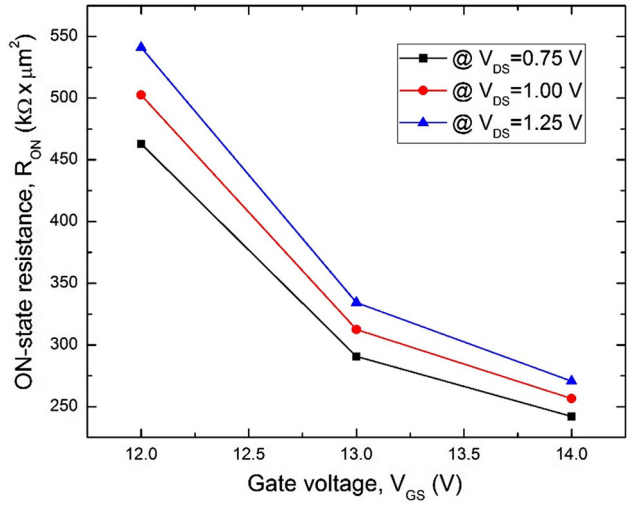

Fig. 3. R_{ON} as function of V_{GS} for different V_{DS} at T = 300 K.

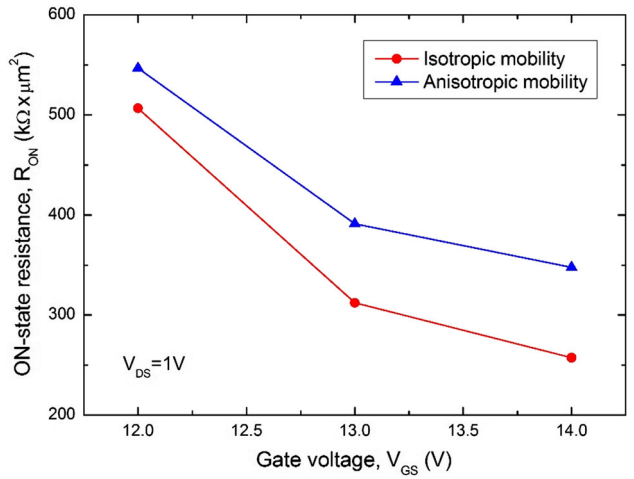

Fig. 4. R_{ON} as function of V_{GS} for different mobility behaviors at T = 300 K.

BV_{DS} on the order of 10% is calculated for the same drain leakage current level assumed previously; For example, for the device in Table II, the simulation gives BV_{DS} = 850 V for N_{drift} = 3 × 10^{15} cm^{-3}, as in Ref. 23. However, N_{drift} has only a limited effect on the device BV_{DS} characteristic considering the thinner W_{drift} (i.e., $W_{drift} \leq 3$ μm in Table III).[7]

ON-State Characteristics and Temperature Effect

The I_D–V_{DS} curves of a DMOSFET with W_{drift} = 1.8 μm and N_{drift} = 3 × 10^{15} cm^{-3} are shown in Fig. 2 for V_{GS} from 10 V to 14 V. These simulation results indicate that the device is truly in ON-state for $V_{GS} > 8$ V at room temperature.

The numerical simulations and analytical results are in good agreement, especially when assuming the device operates in the deep triode region ($V_{DS} \leq 2$ V). For V_{DS} = 1 V and V_{GS} = 14 V, the drain current is close to 3.9 $\mu A/\mu m^2$, corresponding to an ON-state resistance R_{ON} of about 255 kΩ × μm^2. From Fig. 2, the R_{ON} values calculated for different V_{DS} as a function of V_{GS} are plotted in Fig. 3.

It is worth noting that, although for comparison purposes with the results reported in Ref. 23 isotropic mobility behavior was assumed by default, during the simulations the impact of an anisotropic model in determining the device R_{ON} was also evaluated. In particular, the anisotropic mobility model was defined using different parameter values along the x- and y-direction in Fig. 1, which we can suppose applies to the <1100> and <0001> planes[32] within the 4H-SiC structure, respectively. In other words, the MOS channel lies in the high-mobility <1100> plane, whilst the perpendicular <0001> plane is characterized by a longer resistive path along which the drain current flows. Assuming the parameters in Table I for the Caughey–Thomas mobility model, with a perpendicular to parallel ratio of 0.83 as suggested in Ref. 53, the variation of R_{ON} for different mobility behaviors is shown in Fig. 4.

By accounting for the current degradation in the <0001> plane due to the thickness and doping concentration of the drift region, the anisotropic mobility gives higher values of R_{ON} while the isotropic model underestimates R_{ON} by the order of 25% on average in the considered voltage range.

The drift region thickness W_{drift} and doping concentration N_{drift}, as well as the channel length L_{ch}, are critical parameters affecting R_{ON}, as shown in Fig. 5 for V_{GS} = 14 V and V_{DS} = 1 V.

From Fig. 5a, b, the drain current increases with decreasing W_{drift} and increasing N_{drift} as a result of the decreasing R_{ON} due to a reduction of its R_{drift} component. On the other hand, from Fig. 5c, increasing the channel length tends to increase

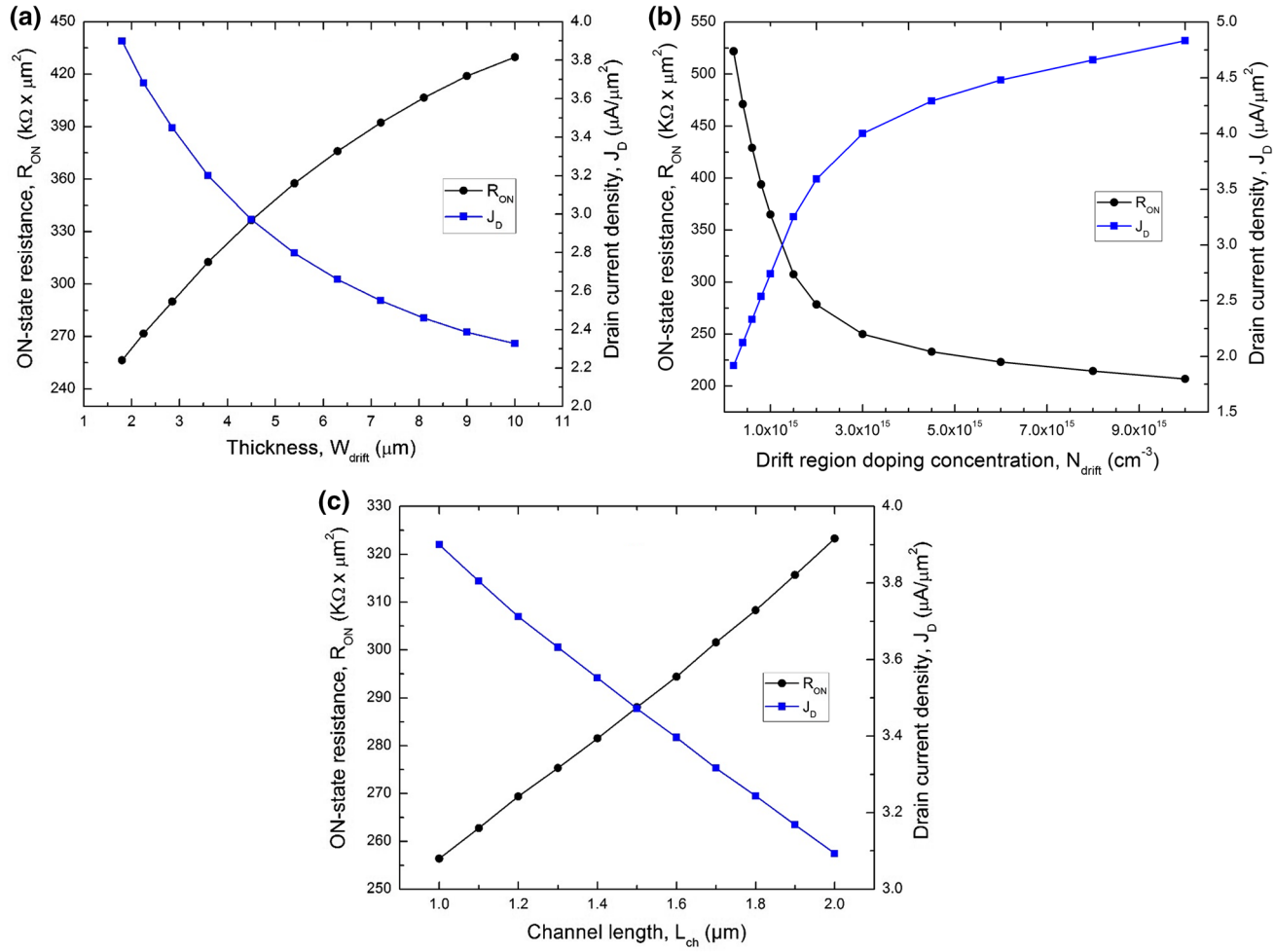

Fig. 5. R_{ON} and J_D behaviors as functions of (a) W_{drift}, (b) N_{drift}, and (c) L_{ch}, for V_{GS} = 14 V and V_{DS} = 1 V.

R_{ON} via the R_{ch} component in a rather linear manner.

The effect of temperature on the device current capabilities is shown in Fig. 6a, b.

As expected, J_D decreases with increasing temperature in Fig. 6a. This effect is due to the temperature dependence of the carrier mobility and the overall increase of R_{ON}, as shown in Fig. 7. In particular, the increased temperature limits the current components which originate in the inversion layer and drift region.[7] At the same time, linked to the increase of the intrinsic carrier concentration in 4H-SiC, Fig. 6b shows that the threshold voltage of the DMOSFET tends to decrease, leading to a zero temperature coefficient (ZTC) point close to V_{GS} = 11 V.

Finally, for fixed base depth and distance between the base regions, we simulate the R_{ON} behavior for different doping concentrations in the JFET region under the gate oxide (N_{JFET}). In the adopted N_{JFET} doping range (3×10^{15} cm^{-3} to 3×10^{16} cm^{-3}), the results show that this parameter has only limited impact on R_{ON} at different temperatures, making the device ON-state current capability only weakly dependent on the majority carrier concentration in the JFET region where the inversion layer is formed.

THEORETICAL BASIS FOR MOGA

In recent years, MOGA-based techniques have gained great popularity in the scientific community in many research areas, focused on the optimal solution of multidimensional and nonlinear problems.[54–57] Distinctive characteristics of the MOGA approach are its universality and simple implementation. It is well known that the majority of optimization procedures provide a single solution. In contrast, MOGA-based techniques permit the identification of a set of optimized solutions, commonly called a “Pareto front,” which allows the selection of an appropriate combination of results according to the application field.

The background in this scenario is to establish many proper arguments, namely a set of objective functions, different constraints, and design parameters. Then, the multiobjective optimization

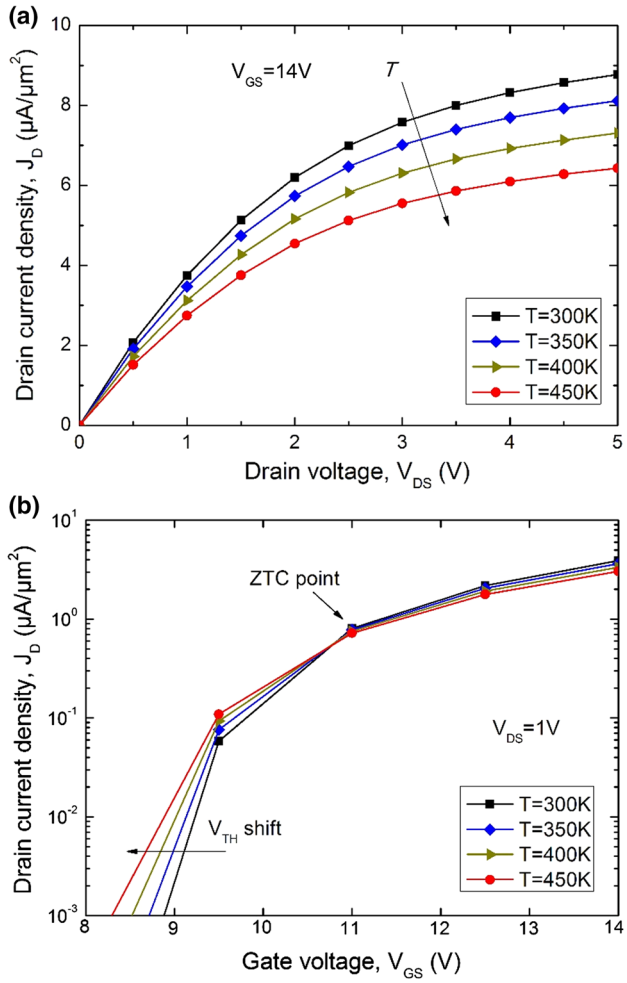

Fig. 6. (a) J_D–V_{DS} and (b) J_D–V_{GS} curves in the temperature range from 300 K to 450 K with W_{drift} = 1.8 μm and N_{drift} = 3 × 10^{15} cm^{-3}.

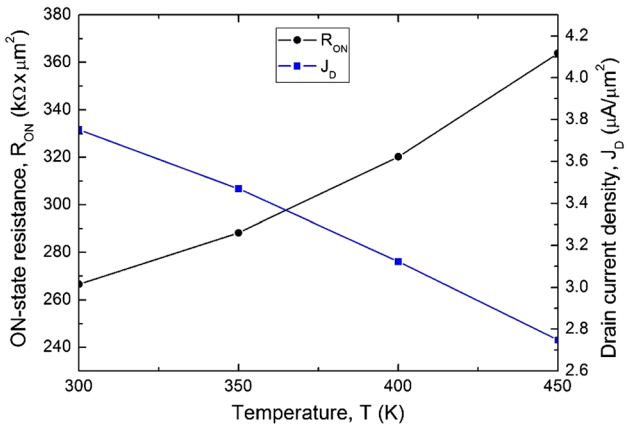

Fig. 7. R_{ON} and J_D behaviors as functions of temperature for V_{GS} = 14 V and V_{DS} = 1 V.

provides different solutions that achieve the best compromise between the considered functions. Moreover, the criteria can involve dilemma and/or complementary conditions.

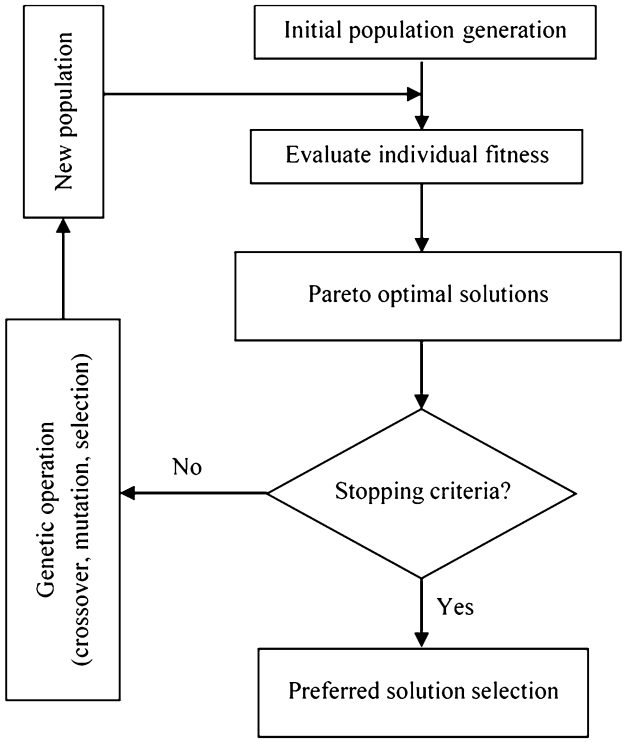

Fig. 8. Schematic flowchart for a multiobjective genetic algorithm.

A simplified schematic flowchart for a multiobjective genetic algorithm is shown in Fig. 8. As seen, it is based on the application of selection, crossover, and mutation operations on a certain generation. Starting from an initial population, these operations allow the algorithm to evolve through different generations until a required criterion is reached. Otherwise, the constraint on the maximum number of iterations determines its termination.

In MOGA terminology, a population is a set of chromosomes generated randomly, where each chromosome is made of numbered units called genes. The genes correspond to the design physical and geometrical fitting parameters (e.g., drift region thickness and doping, channel length, etc.). The initial population is made of two chromosomes (parents), and the crossover operation consists in combining them to obtain a new chromosome called offspring. This process is repeated for all the chromosomes to yield the best offspring. At the same time, mutation occurs at the genetic level to ensure the exploration of all the considered parameters. Finally, the selection operation permits the choice of the best offspring to create the next population.

Optimized 4H-SiC DMOSFET Design

In this section, the MOGA-based technique is used to support the numerical and analytical simulation results in order to design an optimized 4H-SiC DMOSFET in terms of breakdown voltage and ON-state resistance. In other words, we deal with

Table IV. Configuration parameters used for MOGA-based optimization

Number of variables	10
Population size	1000
Maximum number of generations	100
Selection	Tournament
Crossover	Scattered
Mutation	Adaptive feasible migration
Crossover fraction	0.8
Migration fraction	0.2
Pareto front population fraction	0.5

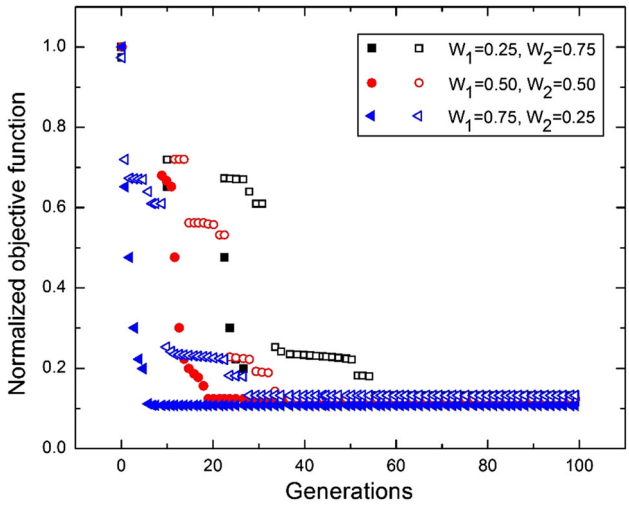

Fig. 9. $F(Y)$ behavior versus generations for different values of the weighting factors w_1 and w_2 when using both numerical (filled symbols) and analytical (empty symbols) models as fitness functions.

two objective functions, considered in the form$\mathrm{BV_{DS}}(Y)$ and $R_{\mathrm{ON}}(Y)$, where $Y = \{t_{\mathrm{ox}}, W_{\mathrm{G}}, L_{\mathrm{ch}}, W_{\mathrm{drift}}, X_{\mathrm{JP}}, X_{\mathrm{N+}}, X_{\mathrm{JFET}}, N_{\mathrm{A}}, N_{\mathrm{D}}, N_{\mathrm{drift}}\}$ is a vector of device parameters.

The design optimization is evaluated according to the following aim: minimize the ON-state resistance while maximizing the breakdown voltage for a fixed drain–source voltage range. Proper constraints on the physical and geometrical parameters in Y with respect to realistic values are defined during the computations. Also, tournament selection and scattered crossover techniques are employed to generate random vectors, and each combination of Y is binary-coded using biomimicry considerations.

A full set of configuration parameters assumed for the MOGA-based optimization is summarized in Table IV.[58,59]

It is noteworthy that a MOGA-based technique can use either analytical or numerical models indifferently as fitness functions. However, the complexity of the DMOSFET design, which

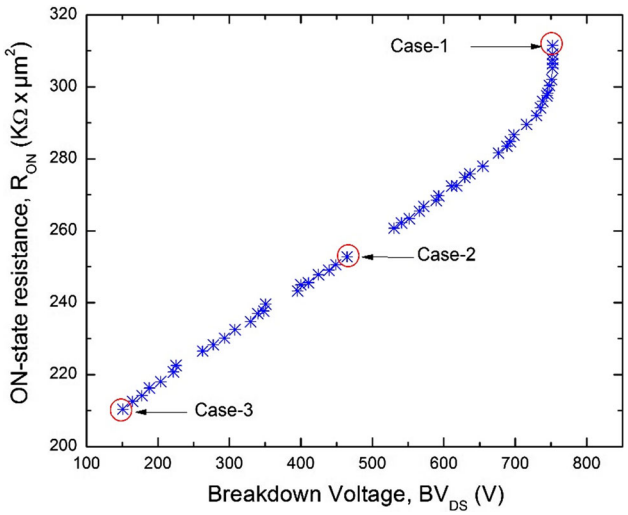

Fig. 10. Pareto-optimal solutions for the DMOSFET design.

involves different interrelated parameters, suggests that the computational time required by the algorithm should be compared when using numerical or analytical approaches. Moreover, as shown above, the output I_{D}–V_{DS} characteristics of both models are in good agreement within the device triode region.

To achieve such a comparison of computational time, the weighted sum approach is used to incorporate the two objective functions defined above into a single one, expressed as

$$F(Y) = w_1(1/\mathrm{BV_{DS}}) + w_2 R_{\mathrm{ON}}, \qquad (13)$$

where the optimal solution varies according to the values of the weighting factors w_1 and w_2. In particular, we consider three cases, namely (a) $w_1 = 0.25$, $w_2 = 0.75$; (b) $w_1 = w_2 = 0.5$; (c) $w_1 = 0.75$, $w_2 = 0.25$. The behavior of $F(Y)$ as a function of the evolving generations can be plotted to determine the convergence of the algorithm in each case (Fig. 9).

As shown by this figure, for a single-objective function $F(Y)$ based on a numerical fitness function, convergence occurs within 28 (a), 18 (b), and 5 (c) generations, respectively. In contrast, it occurs within 55 (a), 35 (b), and 28 (c) generations for the analytical function. In addition, the latter optimization procedures require much longer computational time (about twice), amounting to about 10 min to 15 min on a modern personal computer (PC). For the sake of brevity, in what follows only the numerical model is thus considered.

The Pareto front with the assumed objective functions $R_{\mathrm{ON}}(Y)$ and $\mathrm{BV_{DS}}(Y)$ is depicted in Fig. 10. Each pair of solutions (R_{ON}, $\mathrm{BV_{DS}}$) corresponds to a specific combination of the vector Y.

As shown in Fig. 10, we choose three pairs of solutions to assess the accuracy of the proposed optimization of the design of a device rated for $\mathrm{BV_{DS}}$

Table V. MOGA-based optimization of 4H-SiC DMOSFET design parameters

	Case 1	Case 2	Case 3	Ref. 23
Design Parameter				
Silicon oxide thickness, t_{ox} (μm)	0.085	0.085	0.085	0.08
Source thickness, X_{N+} (μm)	0.5	0.5	0.5	0.5
Channel length, L_{ch} (μm)	1.06	1.14	1.0	1.0
Base junction depth, X_{JP} (μm)	2.0	2.0	1.65	1.5
Base-to-base distance, X_{JFET} (μm)	6.13	6.72	7.6	7.0
Epilayer thickness, W_{drift} (μm)	10	3.75	1.8	1.8
Gate width, W_G (μm)	8.65	9.4	10	9.4
n^+-Source doping, N_D (cm^{-3})	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}
p-Base doping, N_A (cm^{-3})	1×10^{17}	1×10^{17}	1.25×10^{17}	1.5×10^{17}
n-Drift doping, N_{drift} (cm^{-3})	2.88×10^{15}	2.89×10^{15}	2.89×10^{15}	3×10^{15}
Objective functions				
ON-state resistance, R_{on} (k$\Omega \times \mu$m^2)	315	250	210	260
Breakdown voltage, BV_{DS} (V)	800	450	150	150

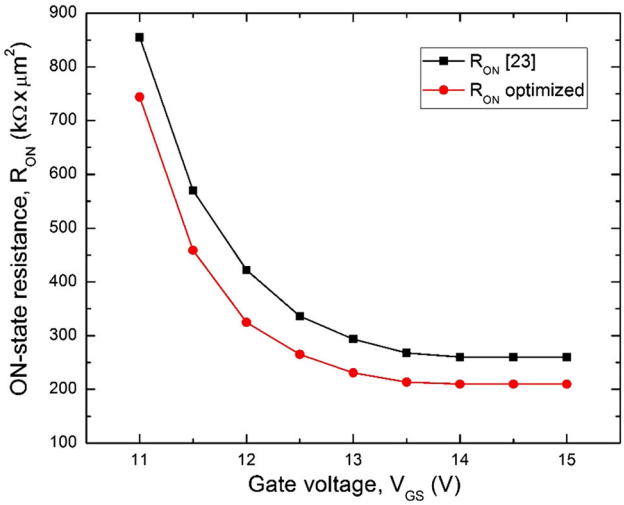

Fig. 11. R_{ON} comparison between MOGA-based results and those reported in Ref. 23.

of 150 V (case 1), 450 V (case 2), or 800 V (case 3), respectively. The relevant geometrical and physical parameters are summarized in Table V. Here, the fundamental device parameters reported in Ref. 23, which refer to a 4H-SiC DMOSFET with the same device footprint area (15 μm^2) and dimensioned for BV_{DS} = 150 V, are also listed for comparison. The R_{ON} values are calculated for V_{GS} = 14 V and V_{DS} = 1 V.

To highlight the efficiency of the proposed design strategy, a comparison with the R_{ON} results calculated in Ref. [23] for V_{GS} in the range from 11 V to 15 V and V_{DS} = 1 V is shown in Fig. 11.

It can be clearly seen that, for a device with the same BV_{DS} value, the MOGA-based optimization achieves lower R_{ON} over the whole explored V_{GS} range. In the full ON-state condition, R_{ON} is decreased by a factor of up to 20%.

CONCLUSIONS

An optimized design for a 4H-SiC DMOSFET for a specific application was obtained using a multiobjective genetic algorithm. The electrical characteristics of the device were investigated in terms of the ON-state resistance and breakdown voltage using both analytical and numerical models, revealing good agreement in the considered voltage range. To evaluate the effective device performance, the temperature effect and drain current degradation due to the anisotropic carrier mobility behavior were also introduced. The simulation models were then used as fitness functions for a MOGA-based design with the aim of determining optimal values of the geometrical and physical parameters to minimize the ON-state resistance value for devices with different breakdown voltages in the range from 150 V to 800 V. The analytical and numerical results were also used to evaluate the effectiveness of the MOGA analysis. With respect to a low-voltage DMOSFET dimensioned for BV_{DS} = 150 V, the optimized device achieved an R_{ON} value close to 210 k$\Omega \times \mu$m^2, decreased by a factor of 20% with respect to that reported in previous work.

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