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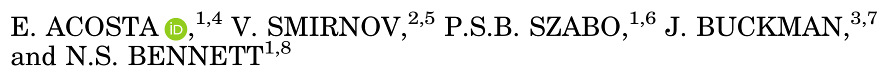
Optimizing Thermoelectric Power Factor in *p*-Type Hydrogenated Nano-crystalline Silicon Thin Films by Varying Carrier Concentration



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Most approaches to silicon-based thermoelectrics are focused on reducing the lattice thermal conductivity with minimal deterioration of the thermoelectric power factor. This study investigates the potential of *p*-type hydrogenated nano-crystalline silicon thin films (μc-Si:H), produced by plasma-enhanced chemical vapor deposition, for thermoelectric applications. We adopt this heterogeneous material structure, known to have a very low thermal conductivity ($\sim$ 1 W/m K), in order to obtain an optimized power factor through controlled variation of carrier concentration drawing on stepwise annealing. This approach achieves a best thermoelectric power factor of $\sim 3 \times 10^{-4}$ W/mK^2 at a carrier concentration of $\sim 4.5 \times 10^{19}$ cm^3 derived from a significant increase of electrical conductivity $\sim \times 8$, alongside a less pronounced reduction of the Seebeck coefficient, while retaining a low thermal conductivity. These thin films have a good thermal and mechanical stability up to 500°C with appropriate adhesion at the film/substrate interface.

Key words: Thermoelectric, nano-crystalline silicon, thin films, carrier concentration, annealing, power factor

INTRODUCTION

Thermoelectric technology constitutes an ongoing option to enhance energy efficiency by direct conversion of the energy harvested from, among other things, the enormous amount of waste heat released by large-scale power generators in the production of primary energy. However, the practical application of thermoelectric generators (TEGs) has not achieved prominent market penetration, due to low efficiency and the high cost of materials, and, for some of them, toxicity. Hence, the necessity persists for low-cost thermoelectric materials with higher thermoelectric figure-of-merit (ZT), suitable for large-scale manufacturing, in order to expand the scope of application into markets traditionally dominated by other technologies. The efficiency of a material to directly convert heat into electricity is governed by the ZT, defined as[1–3]

$$\mathrm{ZT} = \frac{S^2 \sigma T}{k} \quad (1)$$

where S represents the Seebeck coefficient, σ is the electrical conductivity, and k represents the total thermal conductivity defined as ($k = k_\mathrm{l} + k_\mathrm{e}$), where k_l and k_e are the lattice and electronic contributions, respectively, and T represents the absolute temperature. Thus, achieving a maximum possible value of thermoelectric power factor (PF) ($= S^2\sigma$) accompanied by the smallest total thermal conductivity are

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the basic approaches to optimize ZT. Nonetheless, the challenge of decoupling these interrelated parameters has impeded the attainment of values for ZT beyond unity for most commercially applicable materials, such as Bi_2Te_3, for near-room-temperature (RT) applications.

Silicon has become the prominent base material in the development of new technologies, such as microelectronics and photovoltaics, in the last decades[4,5] thanks to its enormous reserves and relative low cost, combined with the ability to very accurately control its electrical, electronic and optical properties, mainly by doping. However, thermoelectrics is a field that has remained an exception, due mainly to its intrinsic high thermal conductivity (149 W/m K at RT),[6] giving poor thermoelectric performance (ZT about 0.01 at RT). Most approaches to Si thermoelectrics have focused on reducing this parameter by decoupling the lattice contribution of thermal conductivity from the electronic transport properties. In this respect, significant achievements have been reported in silicon-based materials. Works on silicon nanowires with diameters ~ 50 nm have attained high success, achieving a reduction in thermal conductivity approaching the amorphous limit (0.76–1.5 W/m K) resulting in ZTs in the range 0.4–0.6 at RT.[7,8] Along the same lines, a considerable reduction of thermal conductivity (1.14–2.03 W/m K) attributed to a 'necking' effect for phonon scattering is produced when single crystalline membranes are decorated with nano-holes, resulting in a ZT around 0.4 at RT.[9] A lower level of improvement of k (4.4–6.3 W/m K) accompanied with a slight deterioration of electrical transport properties was reported in Refs. 10 and 11 but still giving ZTs larger than an order of magnitude higher, compared to single crystal silicon. Lately, a ZT of 0.2 at 360 K was reported in Ref. 12, attributed to a 20-fold reduction of k due to increased phonon scattering by large concentrations of lattice vacancies incorporated in Si nano-films, while leaving electronic transport properties unchanged.

On the other hand, approaches have also aimed at enhancing ZT by improving the PF. Previous works have reported an increase of the PF alongside a reduction of k in silicon-based structures. Early in the 1960s, the suitability of Ge-Si alloys for thermoelectric applications was demonstrated due to their high PF and low thermal conductivity values at high temperatures (900–1000°C).[13] In the late 1980s, Vining[14] demonstrated the increase of the PF due to an anomalous parallel increase of S and hole mobility as a function of carrier concentration in nano-crystalline silicon. Yu et al.[15] demonstrated the enhancement of electrical conductivity and reduction of k while S remained unaffected through modulation-doping in nano-composites giving a ZT 1.3 at 900°C. A similar behaviou was found in phosphorous-doped nanostructured bulk silicon, resulting in a moderate ZT (0.6 at 1050 K)[16] ascribed to significant phonon scattering of nano-precipitates with little influence on either S or Hall mobility, giving a PF ~ 4.4 mW/m K^2 at 800°C. Most recently, a simultaneous increase of S and electrical conductivity providing a high PF was experimentally demonstrated by Narducci et al.,[17] and later theoretically approached by Neophytou et al.[18] in highly boron-doped nano-crystalline silicon.

In the present study, we adopted the approach of taking a Si-based material that, in its as-deposited state, has an intrinsically low thermal conductivity. Hydrogenated nano/micro-crystalline silicon (μc-Si:H) is an inhomogeneous material whose microstructure consists of small crystallites clustered in a columnar structure (conglomerates of crystallites) extending perpendicularly from the substrate, surrounded by incoherent material or grain boundaries embedded in amorphous tissue. Characterization of k in this kind of material structure has demonstrated extremely low values, as low as < 0.1 W/m K,[19] which is consistent with the high phonon scattering induced within the microstructure. During deposition, hydrogen is contained in micro-voids present in the amorphous phase and grain boundaries, but also forms a large number of Si-H bonds whose vibrational modes absorb part of the heat, reducing thermal conductivity. Furthermore, phonon scattering is reinforced by the micro-spaces formed inbetween the conglomerates of the crystallites, typical in this material.[20] Similarly, a relatively low k (~ 7.8 W/m K) has been shown for intrinsic nano-crystalline silicon with grain size ~ 64 nm and porosity of 17% ascribed to phonon scattering at grain boundaries. Such a scattering mechanism is known to be present in our material, as the conglomerates are formed by smaller crystallites separated by a large density of twin boundaries and stacking faults.[20,21] In particular, characterization of k in these samples in as-grown state was reported in Ref. 22 showing similarly low values. Therefore, any enhancement in the PF with at least invariable k would provide an attractive ZT for μc-Si:H. Loureiro et al.[23,24] achieved a PF of 10^{-3} W/mK^2 in n-type hydrogenated nano-crystalline silicon, but a lower value of 4×10^{-4} W/mK^2 in p-type material, where the PF was maximized by post-annealing. In our previous work,[25] we have also shown the promise of phosphorus-doped n-type hydrogenated nano-crystalline silicon, and showed that changes in the PF from post-annealing are largely a result of changes in the free hole concentration—the property classically controlled in order to optimize PF.

In this paper, we report on attempts to enhance the PF in p-type μc-Si:H thin films produced by plasma-enhanced chemical vapor deposition (PECVD) by systematic variation of the free boron concentration through stepwise annealing. Improvement of the PF in line with n-type material, along with an established intrinsically low k, would

provide a promising scalable manufacturing alternative for thermoelectric applications. The deposition technique utilized guarantees the production of robust films with controllable doping, crystallinity and grain size at relatively low cost, suitable for industrial scale, as already proven in the photovoltaics.[26,27]

EXPERIMENTAL

Highly boron-doped μc-Si:H thin films of 1 μm thickness were deposited on glass substrates of 1 mm thickness utilizing the PECVD technique. Samples were fabricated using very high frequency (94.7 MHz), power of 10 W, substrate temperature of 185°C and total pressure of 0.04 kPa, using 2 sccm of trimethylborane (TMB) in helium (He), 1.5 sccm of silane (SiH_4) and 200 sccm of hydrogen (H_2).

A set of seven square samples (1 × 1 cm) were used in the experiment, as well as two further sets of repeats. One sample in each set was kept in the as-deposited state for subsequent comparison (control sample). Each of the other six samples was annealed at stepwise temperatures from 250°C to 550°C for 1 h. The treatment was carried out in air, utilizing a hot plate equipped with a programmable controller that allows for rapid temperature stabilization with annealing temperatures reached in a ramp time of 8 min and maintained for 1 h. Thereafter, samples were slowly cooled on the hot plate until reaching a temperature of 30°C in approximately 2 h. The accuracy of temperature was corroborated with an independent thermocouple measurement placed near the sample.

A number of techniques were employed to identify morphological changes as a result of post-annealing treatment. First, micro-Raman spectroscopy was used to determine crystallite size and the percentage of crystallinity in all seven samples. Measurements were performed using a Renishaw inVia Raman microscope equipped with a 514-nm laser with 1800 L/mm grating and a magnification of ×50. A low laser power sufficient to provide a good signal-to-noise ratio and to avoid any microstructural changes due to excessive local heating was selected. Second, scanning electron microscopy (SEM) micrographs from as-grown and selected annealed samples were obtained to study the microstructural changes using a Quanta FEG 650 SEM equipped with a concentric backscatter detector using backscatter imaging at low vacuum (~ 0.11 kPa) at 12 kV and a magnification of ×50,000.

In order to corroborate any variation in the thermal conductivity due to structural changes or/and variation of carrier concentration, the cross-plane thermal conductivity was measured by a commercial vendor using a 3ω methodology[28] in the as-grown and post-processed samples.

In-plane characterization at room temperature of electrical resistivity was performed on samples before and after annealing using a Bio Rad HL 5900, based on the Van der Pauw method to eliminate the effect of contact resistance on the conductance measurements. Likewise, the suitability of this same equipment to measure the Hall coefficient permitted the extraction of the carrier concentration and Hall mobility at room temperature.

Afterwards, the in-plane Seebeck coefficient was characterized in each sample in the range from room temperature up to 150°C using a home-built system. It consists of a LakeShore 325 temperature controller with heater and resistance temperature detector, a Linkam LTS 420 temperature-controlled stage, two thermocouples, a Keithley 2700 digital multimeter, and a Keithley 7700 switch card. A steady-state temperature method was utilized that stabilized the sample at a specific temperature difference before the measurement of the signals. The systems provided the Seebeck coefficient after correction for offset voltages from the wire contribution.

Finally, envisaging the fabrication of TEGs, the appropriateness of the deposition method in terms of film/substrate adhesion for the production of thin films was evaluated, drawing on a standard test method established by the American Society for Testing and Materials (ASTM D3359-9). It consisted of making a number of straight cuts equidistantly spaced, using a blade cutter. Then, "Elcometer 99" tape, known as ASTM D 3359 Adhesive Tape, which provides an average removal force of 6.42 Newtons per 10 mm width, was placed over the grid, ensuring good contact was achieved. Then, after waiting for 90 s ± 30 s, the tape was rapidly removed and the removal area of the film was inspected and rated according to a scale. Before the test, it was confirmed that the sample surface was clean and dry to avoid contamination or humidity affecting the tape adhesion, respectively. Under these conditions, for a sample having a thin film thickness of 1 μm, it was necessary to make 11 cuts spaced 1 mm apart with a length of about 20 mm.

RESULTS AND DISCUSSION

Morphological Study

The crystalline volume fraction (X_c) and crystallite size (L) were obtained based on the Raman technique. Crystallinity was determined using the relationship $X_c = (I_c + I_m)/(I_c + I_m + yI_a)$ drawing on data collected in the spectrum range from 400 cm^{-1} to 600 cm^{-1}, where the transverse optical mode is active for the crystalline and amorphous Si phases. The three integrated intensities of μc-Si:H were extracted by deconvolution of Raman spectra fitted with Gaussian components centered at: (1) ~ 480 cm^{-1}, corresponding to the amorphous phase (I_a); (2) a second band ocurring at ~ 518 cm^{-1} (I_c), ascribed to micro-crystallites embedded in an amorphous phase; and (3) an intermediate band peak at ~ 510 cm^{-1} (I_m), associated with Si-Si bonds at the grain boundaries.[20,29] The Raman emission cross-

sectional ratio (y), which is defined as ratio of the integrated Raman cross-section for crystalline silicon to amorphous silicon,[30] strongly relies exponentially on the crystallite size (L) by $y(L) = 0.1 + e^{\left(-\frac{L}{250}\right)}$ and the laser wavelength used for the measurements, and is still under debate;[31,32] thus, in the present study, we assume unity as a value for y in accordance with the expected range of crystallite size (5–30 nm).

Figure 1 shows the results of the crystalline volume fraction and crystallite size computed from Raman data. A high degree of crystallinity is observed in the as-grown sample ($\sim$ 62%) in agreement with pre-defined deposition conditions, i.e., the high hydrogen dilution ratio. After post-processing, the Raman crystalline ratio does not undergo significant changes, with values ranging from $\sim$ 63% to $\sim$ 67%, reflected in the small standard deviation of $\pm$ 1.7%. This scattering falls within the standard error induced in the methodology. In particular, for highly crystalline material, the error is as much as 5%.[33] Hence, we can conclude that, due to the apparent inaction of annealing on crystallinity, the material has reached its crystallization limit prior to post-annealing.

The estimation of the average crystallite size was carried out using the correlation length model[34–36] whose results proved to be valid for sizes no smaller than 5 nm under certain conditions. As the Raman band shape is strongly sensitive to temperature changes, a low laser power was used in order not to induce local heating and/or crystallization at the sample surface. Furthermore, the influence of film stress in the feature of Raman spectra could be considered negligible due to the fact that both the Corning glass substrate (0.355×10^{-5} K^{-1}) and silicon (0.3×10^{-5} K^{-1}) films have very similar coefficients of thermal expansion at the deposition temperature.[33] Thus, the Raman frequency downshift and broadening of line-shape are ascribed to the effect of small crystallite size. Figure 1 shows the average crystallite size obtained for as-grown and annealed samples based on the Raman downshift. Although the data show a low scattering with a standard deviation about $\pm$ 2 nm, the values range between 5 nm and 10 nm, which validates our previous assumption about crystallite size in order to choose y for Raman crystallinity estimation.

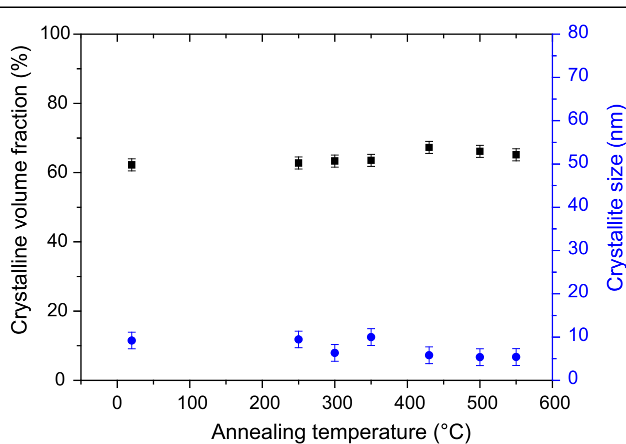

Fig. 1. Effect of post-processing on crystallinity and crystallite size of μc-Si:H films. Crystalline volume fraction (closed squares) does not show a significant variation after post-processing with an average of 62%, while crystallite size (closed circles) ranges from 5 nm to 10 nm with no clear growth trend following annealing. Data points at 20°C represents as-grown values.

Figure 2a–d shows the surface SEM micrographs of samples in (a) as-grown state and those showing significant changes of electronic properties after annealing at (b) 430°C, (c) 500°C and (d) 550°C. All the samples show similarities in microstructure, i.e., protrusions of elongated crystalline clusters (conglomerates of crystallites) of identical shape with different sizes emerging at the surface surrounded by a large fraction of disordered regions. An average length and width around 210 nm and 110 nm, respectively, has been determined for all samples, giving a ratio near 2. This rather homogeneous average dimension, alongside a visual inspection of micrographs, leads us to presume an insignificant growth of conglomerates as a result of annealing, at least in the lateral direction. Previous work has shown a strong correlation between grain size and carrier mobility establishing a linear increase with increasing crystallite size,[37] or sublinearly correlated[38] due to scattering of carriers at grain boundaries. As the film thickness increases, the size of the conglomerates of crystallites observed at the surface is expected to enlarge and reach saturation. An earlier saturation is likely to occur for randomly oriented crystallites, as in μc-Si:H with the corresponding saturation of the carrier mobility.[39] In an attempt to verify this effect in our samples, we carried out mobility measurements on thicker samples (3 μm) deposited under the same conditions. Twelve as-grown samples were characterized giving an average mobility of 2.8 cm^2/Vs, which does not show a large deviation from its counterpart (2.09 cm^2/Vs, 1 μm) considering the error induced during the measurements ($\sim$ 10%). Thus, this apparent saturation of mobility may corroborate the belief that the lateral size saturation of the conglomerates occurs in the as-grown state. Any variation of mobility, without evident increase of crystallinity and crystallite size after annealing, may have its foundations in defects localized in the grain boundaries. The apparent discrepancy in crystallite size obtained between Raman and SEM is because SEM observes the large conglomerates of crystallites, whilst Raman downshift is originated by the small crystallites clustered in these conglomerates.[20,21] In addition, it is observed that adjacent conglomerates of crystallites are separated by narrow boundaries of lower-density material where most defects, dangling bonds and micro-voids are thought to be located.[40] By means of image analysis, it was possible to estimate the surface crystalline fraction through the

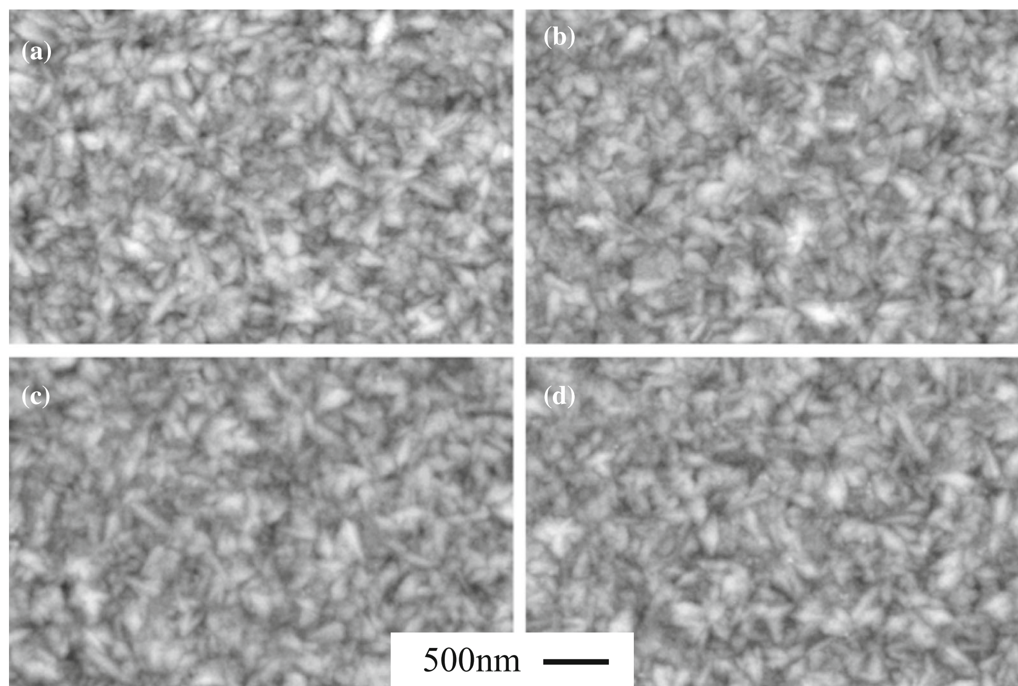

Fig. 2. SEM micrographs showing the microstructure of as-grown (a) and post-processes μc-Si:H films obtained with a magnification of $\times$50,000 at 12 kV: post-processed samples at (b) 430°C, (c) 500°C, and (d) 550°C that presented significant changes in electronic transport show no appreciable variation in lateral size of conglomerates of crystallites. Scale bar applies to all 4 parts.

comparison of bright regions (conglomerates of crystallites) and dark areas (amorphous phase), giving an average crystallinity ~ 64% with a standard deviation of ± 0.65% for all samples. This slight variability between as-grown and annealed samples corroborates the assumption that material has reached its saturation limit. Considering that the Raman technique employed in this study provides the crystalline volume fraction probed over a few hundred nano-meters due to the penetration depth of the laser of 514 nm,[41,42] the good agreement in percentage with the surface crystalline fraction from SEM indicates a similar crystallinity density in-plane and through-plane, which suggests that the length of the conglomerates extending perpendicularly from the substrate[43] covers the whole sample thickness.

Electrical Transport Properties

Despite little variation in sample morphology, significant changes are observed in electrical transport properties in highly boron-doped μc-Si:H as a function of carrier concentration, resulting from post-annealing. Figure 3 shows the variation with carrier concentration of (a) Hall mobility, (b) electrical conductivity, (c) Seebeck coefficient and (d) thermoelectric PF. All values represent room-temperature values after the samples were subjected to an annealing treatment to introduce the desired carrier concentration. Due to post-processing, the range of variation of carrier concentration is from 1.82×10^{19} cm^{-3} for the as-grown sample up to a maximum of 4.49×10^{19} cm^{-3} at 500°C. This value decayed slightly to 4.28×10^{19} cm^{-3} for post-processing at 550°C. In Fig. 3a, it is noticeable that the Hall mobility experiences a boost as carrier concentration rises. It starts at 2.09 cm^2/Vs for the as-grown sample and steadily increases to reach a peak of 6.65 cm^2/Vs at 4.21×10^{19} cm^{-3} (430°C). This observation is in contrast to the well-known trend in bulk Si, in which Hall mobility falls with increasing carrier concentration as a result of increased ionised impurity scattering. In nano-crystalline *p*-type silicon, however, an increase in mobility in the doping range 10^{19}–10^{20} cm^{-3} has been observed in numerous previous studies. A similar simultaneous increase of both parameters was found by Seto[44] and Cowher et al.[45] in boron-doped polycrystalline silicon films over a critical degree of carrier concentration, which coincides with the doping concentration in our samples. This concurrent effect was ascribed to the formation of potential energy barriers at the grain boundaries, which decrease over a certain carrier concentration due to carrier-filling of trapping states.

To understand the behavior of electrical transport properties, we need to discuss the probable effect of annealing in the microstructure. Hydrogen incorporation into the microstructure during deposition of μc-Si:H thin films has been documented.[46–48] During the transition from amorphous to micro-crystalline, the atomic hydrogen penetrates the subsurface passivating dangling bonds at the grain boundaries, also, reacting with clustered hydrogen to form molecular hydrogen, which is trapped within microvoids, and inserting into strain Si-Si bonds present in the amorphous phase to induce

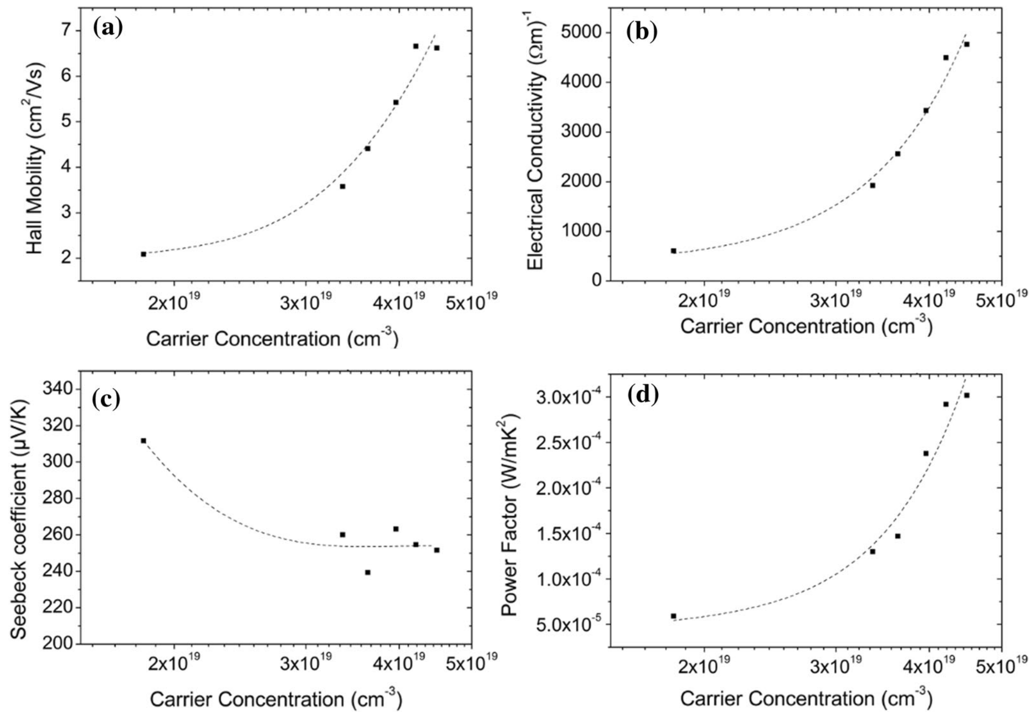

Fig. 3. Variation of thermoelectric properties with carrier concentration. (a) Evolution of Hall mobility with carrier concentration showing a rise of mobility from 2.09 65 cm^2/Vs in the as-grown state up to a maximum of 6.65 cm^2/Vs at 4.21 $\times$ 10^{19} cm^{-3} (430°C). (b) Evolution of electrical conductivity with carrier concentration maximizing to $\sim$ 4764 $(\Omega m)^{-1}$ at 4.49 $\times$ 10^{19} cm^{-3}. (c) Evolution of Seebeck coefficient with the gradual increase of carrier concentration reaching a value of $\sim$ 252 μV/K at peak. (d) Evolution of the power factor with carrier concentration reaching a maximum of 3 $\times$ 10^{-4} W/m K^2 at $\sim$ 4.5 $\times$ 10^{19} cm^3. Trend lines are provided as a guide to the eye.

crystallization after structural relaxation.[49] The largest portion of hydrogen has been identified at the grain boundaries by a number of studies[50,51] in the form of Si-H and Si-H_2 at the internal surfaces of micro-voids originated in the same grain boundaries. This feature is supported in our samples by the equally large volume fraction estimated from the Raman mode near 510 cm^{-1} ascribed to grain boundaries.[29] Following the same trend as the crystalline volume fraction, the counterpart for grain boundaries does not show a significant variation with annealing, giving an average percentage of $\sim$ 32% with a standard deviation of $\pm$ 3.6% for all samples.

It is known that out-diffusion of hydrogen in μc-Si:H occurs at a temperature higher than the deposition temperature depending on the exposure time.[52–54] Thus, with the annealing conditions of temperature and time applied, it is expected that hydrogen starts to effuse from the microstructure at temperatures over 185°C. This out-diffusion of hydrogen is partially contributed by the preferential removal of hydrogen after annealing from the large number of complexes (B-C-H_x, B-H-Si) present in the crystalline phase of μc-Si:H, as a result of the carbon contained in TMB.[55,56] This depassivation converts boron atoms which are initially electrically inactive into electrically active B-Si bonds, increasing the free hole concentration. The upper level of hole concentration achieved is limited by the solid solubility of boron in crystalline silicon, which is around 10^{20} cm^{-3} at 1000°C,[57] correspondingly, at the fabrication temperature of 185°C, the boron concentration in crystallites is well below this reference, and due to the possible segregation of boron atoms to grain boundaries and the amorphous phase. Another important contribution to effusion likely comes from the hydrogen contained in the grain boundaries, i.e., dangling bonds and micro-voids. The hydrogen released from the well-passivated grain boundaries leaves this disordered region in a less compact state, allowing the potential permeation of oxygen as a result of post-deposition oxidation. A number of studies have reporteds both an inverse correlation between hydrogen and oxygen content after being exposed to air, and a direct correlation between oxygen content and the density of defect states at the grain boundaries.[49,58–60] Hence, it is reasonable to presume that, once the carrier concentration has reached the saturation limit at the annealing temperature of 500°C, the excess of defects created in the next annealing stage at 550°C due to oxygen incursions traps more carriers, inducing a decay in concentration and mobility as evidenced in the experimental data.

Thus, considering the intrinsic microstructure of μc-Si:H, which is known to contain a large number of defects at the grain boundaries, we adopt this model to explain the relatively large increase of electrical conductivity.

Figure 3b shows that the mobility increase produces a rapid rise in electrical conductivity with carrier concentration, reaching its maximum of ~ 4764 $(\Omega m)^{-1}$ at 4.49×10^{19} cm^{-3} (500°C). As a result of the concurrent increase of Hall mobility with carrier concentration in the specified range, the electrical conductivity is boosted by nearly eight-fold at its optimized value, compared to the as-grown samples.

Thermoelectric Transport

Seebeck Coefficient

Figure 3c shows the evolution of the Seebeck coefficient measured at room temperature as a function of carrier concentration. All the measurements show positive values which confirms that holes are the dominant carrier type. The Seebeck coefficient in these samples showed a linear increasing trend with temperature (not shown), indicating a pronounced metallic behavior, in agreement with the high doping level. Initially, a relatively high absolute Seebeck coefficient for the as-deposited sample around 312 μV/K is observed. Similar studies on this material structure show values in the order of 220 and 512 μV/K, although electrical conductivity is considerably lower, at 720 and ~ 1370 Ω^{-1}/m, respectively, as compared to this work.[23,61] It has been demonstrated that, apart from the doping level, the magnitude of the Seebeck coefficient strongly depends on the degree of crystallinity in μc-Si:H.[62] As already reported, crystallinity remains roughly unchanged ($\sim$ 62%) after post-annealing. Accordingly, we ascribe the variation of the Seebeck coefficient to change in carrier concentration and density of defect states created due to oxygen at the grain boundaries. Overall, the Seebeck coefficient evolves in a decreasing trend with carrier concentration, as would be classically expected. In the first increasing step of carrier concentration, S experiments the largest fall, down to ~ 260 μV/K, which is in agreement with the largest increase of carrier concentration, up to 3.36×10^{19} cm^{-3}. In subsequent carrier concentration increment steps, variation of S occurs in shorter intervals consistent with the smaller change of carrier concentration, reaching a minimum of ~ 252 μV/K, which corresponds to the maximum carrier concentration (4.49×10^{19} cm^{-3}) in the post-processing.

Power Factor

Figure 3d depicts the resulting thermoelectric PF from the enhancement of electrical conductivity and the reduction of the Seebeck coefficient with carrier concentration, computed at room temperature. It can be seen that, due to the trade-off between electrical conductivity and S, the as-grown values do not provide an optimized PF, but the lowest ($= 6 \times 10^{-5}$ W/mK^2), in spite of the relative high S. Controlled increase of carrier concentration results in a PF improvement nearly 5-fold with respect to the as-grown value. It can be observed thatthe PF steadily increases with the rise of carrier concentration to reach a peak of $> 3 \times 10^{-4}$ W/mK^2 at the maximum carrier concentration ($\sim 4.5 \times 10^{19}$ cm^3). It should be noted that the substantial increase of the PF takes place in the range from $\sim 3.4 \times 10^{19}$ cm^3 to 4.2×10^{19} cm^3, and then marginally increases to reach a plateau at the peak.

The reported PF value is very similar to that of a recent publication for a similar material structure,[24] whose optimization was achieved with post-annealing at 250°C, to a value of 4×10^{-4} W/mK^2. In the present approach, the optimized PF is attained at a higher temperature (500°C). This difference likely has its foundations in the dissimilarity in film thickness, initial crystallinity and transport properties, which are driven by the deposition parameters adopted in each approach. The fact that the films can be reliably and repeatedly electrically measured at relatively high annealing temperatures reflects the good mechanical and thermal stability of the films, i.e., the absence of cracks after annealing, and provides the possibility that these films could be produced and operated in a broad window, i.e., 200–500°C, to expand the application of silicon thin films at higher temperatures with good mechanical and thermal stability. Both electrical conductivity and Seebeck coefficient measurements become unreliable following processing at 550°C. Therefore, higher processing temperatures will not lead to a higher PF. Annealing for longer times at temperatures in the range 250–500°C was attempted as a means to increase the doping concentration; however, a limit appeared to be reached. Indeed, in Ref. 24, the PF appears to saturate, also presumably as a result of a maximized free hole concentration being reached. Although the PF does appear to have reached a plateau, it would be interesting to attempt to push the doping concentration higher still, in an attempt to maximize the PF still further by other means, i.e., by altering deposition parameters and/or post-annealing under an inert atmosphere to avoid the creation of additional carrier traps due to oxygen. Consequently, post-processing demonstrates that it is possible to produce adequately boron-doped thin films with controlled carrier concentrations in the right order for thermoelectric applications.

Table I. Thermal conductivity of μc-Si:H thin films in as-grown and annealed states measured through 3ω method

Sample type	X_c (%)	Condition	k (W/m K)
p-type μc-Si:H	63	As-grown	3.2 ± 0.3
p-type μc-Si:H	66	Annealed at 500°C	1.5 ± 0.3

Thermal Conductivity

In order to evaluate the effectiveness of preserving the low thermal conductivity in μc-Si:H thin films, this property was characterized in the as-grown and post-annealed states, using a commercial vendor, and the results of the characterization are shown in Table I. Characterization of *p*-type samples of 1 μm thickness via the 3ω method shows a reduction of thermal conductivity for the post-annealed sample at 500°C. As an apparent unchanged crystalline volume fraction was demonstrated in the morphological study, the crystalline-dependent thermal conductivity correlation in μc-Si:H may not explain this reduction.[63] Thus, it is likely that the reduction of total thermal conductivity comes from the reinforcement of a scattering mechanism.

Phonon–phonon and phonon-boundary scattering are known to be the prevailing phonon scattering mechanisms. However, when carrier concentration is over 10^{18} cm^3, the electron–phonon scattering gains importance in reducing the lattice component of total thermal conductivity in bulk silicon.[64] A number of studies have shown the effect of this scattering mechanism in the reduction of lattice thermal conductivity in silicon.[65,66] Since the morphological study shows no evidence of significant changes in the material structure after annealing, yet the electrical measurements show that carrier concentration in our films more than doubles, it is possible that electron–phonon scattering leads to the additional decrease in thermal transport in the post-processed films.

It was demonstrated that, due to the similarity between the surface crystallinity determined via SEM and the volume crystallinity obtained via Raman, the conglomerates of crystallites in μc-Si:H are likely extending along the sample thickness. Thus, the deviation between in-plane and through-plane thermal conductivity due to microstructure should be minimal. Hence, a net increase of thermoelectric PF is verified, derived from a significant rise of electrical conductivity accompanied by a less pronounced reduction of the Seebeck coefficient, in accordance twith the increment of carrier concentration, which, in turn, may magnify the electron–phonon scattering mechanism that induces a reduction of the lattice thermal conductivity. This favorable relationship makes μc-Si:H a promising material for thermoelectric applications at higher temperatures.

Adhesion Assessment

The fabrication of TEGs, apart from good thermoelectric properties, requires robust films with adequate adhesion in the film/substrate interface. We draw on a standardized procedure to assess the adhesion level of *p*-type μc-Si:H thin films deposited on a glass substrate annealed at 500°C. The adhesion test was repeated for three different annealed samples, named A, B and C, and in different locations, to verify the homogeneity of the adhesion force. In Fig. 4, the cross-cut lattice pattern realized in one of the samples can be seen, consisting of 11 cuts in each direction separated by 1 mm each for a sample before (a) and after (b) the application of the adhesion tape test. A visual comparison between the two images suggests that the largest portion of the surface remains intact after the adhesion test, with a few tiny flakes appearing. The images were processed to quantify the area removed giving for (a) 0.64%, (b) 0%, and (c) 0.45%. The small flake surrounded by a red circle in Fig. 4b illustrates the small removed area.

According to the classification scale provided in ASTM D 3359-09, this very small removed area rates these samples in the upper part of the adhesion test ranking (5B-4B), which establishes

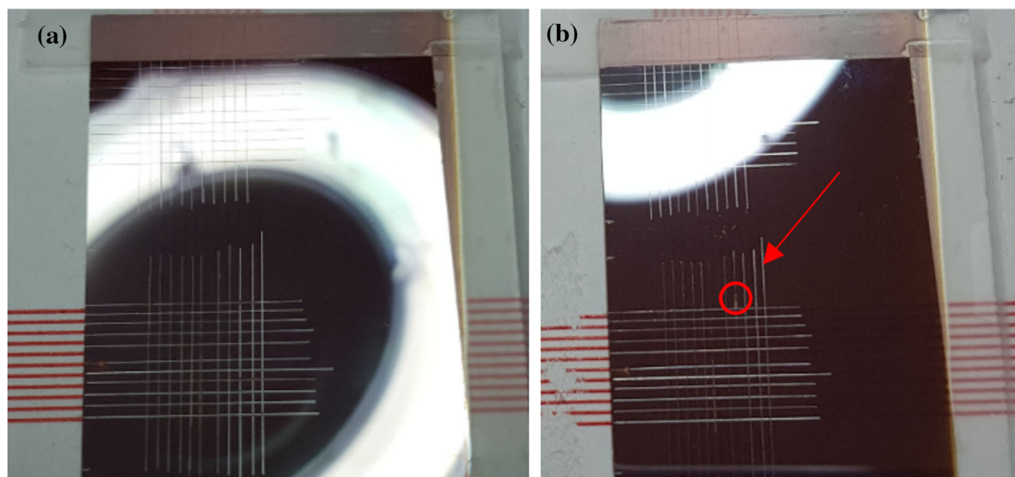

Fig. 4. State of *p*-type μc-Si:H thin film deposited on a glass substrate before (a) and after (b) the adhesion tape test fulfilling ASTM D 3359-09 criteria. A very small area ($\sim$ 0.45%), indicated by the red circle, is removed from the intersections of the cuts (Color figure online).

removed areas of 0% and < 5%, respectively. These results show that the adhesion force between the thin film and the glass substrate is at a generally adequate level. The low standard deviation (SD $\sim$ 0.27%) between the percentages of removed area in all repetitions proves that the adhesion is rather uniform over a large surface. Thus, this experimental test corroborates the suitability of PECVD for the production of thin films with appropriate adhesion to the substrate for the fabrication of TEGs.

CONCLUSION

This investigation explored the thermoelectric potential of boron-doped μc-Si:H thin films produced by the PECVD technique. An enhanced PF in line with the best previous demonstrations for similar material structures was achieved through a controlled variation of carrier concentration. The increase is attributed to a significant rise of electrical conductivity alongside a less pronounced fall of the Seebeck coefficient with carrier concentration. Post-processing of thin films with distinct deposition parameters, as evidenced in similar works, to obtain similar PFs demonstrates that an optimized thermoelectric PF has likely been reached, al though routes to increase the hole concentration in this material could be worth further exploration. Optimization of the PF at higher annealing temperatures (500°C), preserving a very low thermal conductivity, and fulfilment of adhesion test criteria, demonstrate that it is possible to fabricate robust films with good mechanical and thermal stability, which makes μc-Si:H a promising thermoelectric material for scalable production.

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