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Comparative Analysis of Mixed CNTs and MWCNTs as VLSI Interconnects for Deep Sub-micron Technology Nodes

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This research paper presents a performance analysis of the mixed carbon nanotube (CNT) as an interconnect for very large-scale integration (VLSI) circuits at deep sub-micron (DSM) technology nodes. The mixed CNT interconnect is a combination of multiwall CNTs (MWCNTs) and single-walled CNTs (SWCNTs). Using hierarchical modeling, a multiconductor circuit model is proposed for the mixed CNT bundle at global-level interconnect lengths. Due to the insertion of SWCNTs in a MWCNT interconnect, the overall density of the conducting tubes in the proposed mixed CNT interconnect structure increases, thereby decreasing the overall resistance and inductance of the mixed CNTs. The performance of the proposed mixed CNT interconnect is estimated in terms of delay and power delay product (PDP) for different technology nodes (32 nm, 22 nm, and 16 nm) at different interconnect lengths. For comparative analysis, a similar analysis is performed using MWCNT bundle interconnects. The comparative results show that there is reduction in the overall propagation delay and PDP for the proposed mixed CNTs compared to MWCNTs as the interconnect material for DSM technology nodes at global-level interconnect lengths.

Key words: Mixed CNT, multiconductor circuit, equivalent single-conductor circuit, propagation delay, power delay product

INTRODUCTION

In the semiconductor industry, device sizes and interconnect dimensions are decreasing, whereas the number of components in on-chip integrated circuits (ICs) is increasing. The bottleneck often encountered in the very large-scale integration (VLSI) IC design for deep sub-micron (DSM) technology nodes is the interconnect latency and power delay product (PDP). The problems of grain boundary scattering, surface scattering, and electro-migration are noticed in DSM technology nodes manufactured using copper as the VLSI interconnect material. Therefore, there is a definite requirement for alternative materials that can replace copper for better interconnect performance. In recent years, carbon nanotubes (CNTs) have been projected as an alternative to replace copper as VLSI interconnect material because of their large thermal conductivity and current-carrying capability. A graphene sheet is rolled to form cylindrical CNTs with different diameters, of the order of a few nanometers to hundreds of nanometers.[1,2] On the basis of their structure, CNTs can be classified as: single-walled CNTs (SWCNTs) and multiwalled CNTs (MWCNTs) as shown in Fig. 1.

Figure 1a shows the structure of an SWCNT that contains a single cylindrical layer of graphene sheet. Figure 1b shows an MWCNT that contains multiple cylinders of graphene sheets of different diameters concentrically inserted. MWCNTs are always metallic in nature; SWCNTs may be metallic or semiconducting subject to their chirality.[3,4]

In the recent past, researchers have been captivated by MWCNTs as an interconnect material because of their exclusive conductive and thermal

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properties as compared to those of SWCNTs.[5–7] MWCNTs have large diameters and mean free paths (MFPs) as compared to SWCNTs. MWCNTs also have a large number of conducting channels, even at DSM technology nodes. Moreover, the current-carrying capability of MWCNTs is comparable to SWCNTs, and the former can be fabricated more easily than the latter, owing to more efficient control of the growth process.[3,4,8]

It is concluded in the literature that the fabrication of closely packed MWCNT bundles containing large numbers of shells within an interconnect structure is a problematic process.[7,9,10] During the fabrication of conventional MWCNTs, a portion of free space is left owing to large outermost shell diameters, thus inadequately utilizing the space. In the current scenario, researchers have started analyzing models and structures for bundling with a combination of SWCNTs and MWCNTs called mixed CNT interconnects.[11,12] The schematic structure of a mixed CNT bundle, and a combination of SWCNTs and MWCNTs, is shown in Fig. 2.

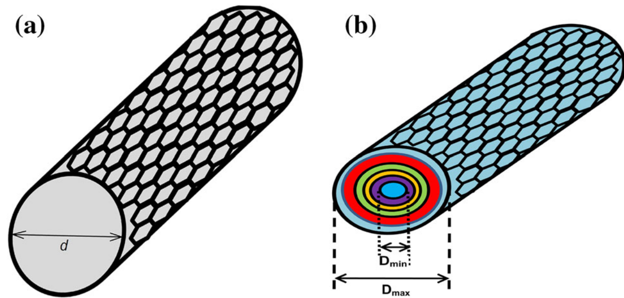


Fig. 1. Structures of an (a) SWCNT and (b) MWCNT.

This paper presents the structure of the proposed mixed CNT interconnect and its equivalent single-conductor (ESC) model, which is used to evaluate its parasitics. Using the proposed ESC model, a comparative analysis of propagation delay and PDP is also presented for variable interconnect length at 32-nm, 22-nm, and 16-nm technology nodes.

The paper is arranged in five sections: the "Physical Structure of the Proposed Mixed CNT Interconnect" section explains the structure of the proposed mixed CNT interconnects. The proposed multiconductor circuit (MCC) model and ESC model for mixed CNT interconnects is explained in the "Modeling of the Proposed Mixed CNT Interconnect Structure" section. In the "Results and Discussions" section, the results for various performance parameters are discussed for MWCNTs and the proposed mixed CNT interconnect. A comparative analysis of propagation delay and PDP of MWCNTs and the proposed mixed CNT interconnect is also presented. Finally, the "Conclusion" section summarizes the outcomes of our research.

PHYSICAL STRUCTURE OF THE PROPOSED MIXED CNT INTERCONNECT

The cross-sectional view of a conventional rectangular MWCNT structure as an interconnect is shown in Fig. 3. The interconnect cross section of width W and height H is placed above ground at a distance y and separated from adjacent interconnects by distance S. The interconnect structure consists of three spherically shaped MWCNT

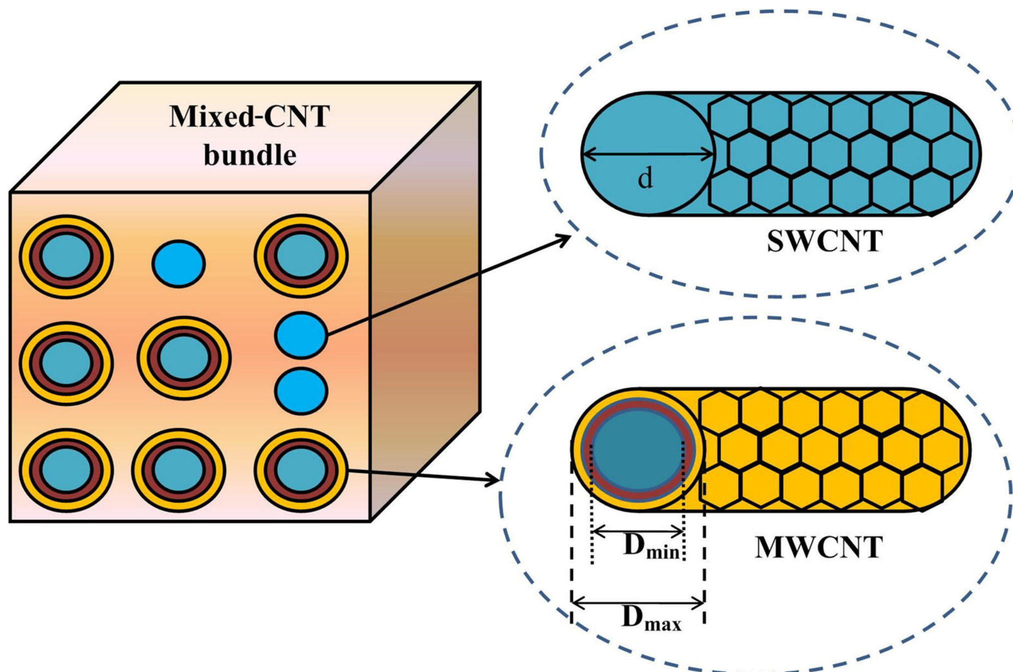


Fig. 2. Mixed CNT interconnect consisting of MWCNTs and SWCNTs.

bundles that are connected vertically parallel to each other. The aspect ratio is considered to be 3 for global-level interconnect lengths as shown in Table I.[13] The actual structure of the interconnect inside an IC is rectangular and that of an MWCNT bundle is spherical. Therefore, the corners and sidewalls of rectangular interconnects are not fully covered and a lot of free space is left, as shown in Fig. 3.

Therefore, a mixed CNT interconnect structure is proposed in such a way that the unfilled area of the MWCNT bundle is covered with a number of small SWCNTs to increase the density, which increases the overall conductivity of the proposed structure. In the proposed mixed CNT interconnect, SWCNTs of 1-nm diameter are inserted at the corners and sidewalls of the conventional MWCNT bundle to fill the gaps of the rectangular interconnect. The physical structure of the proposed mixed CNT interconnect is shown in Fig. 4.

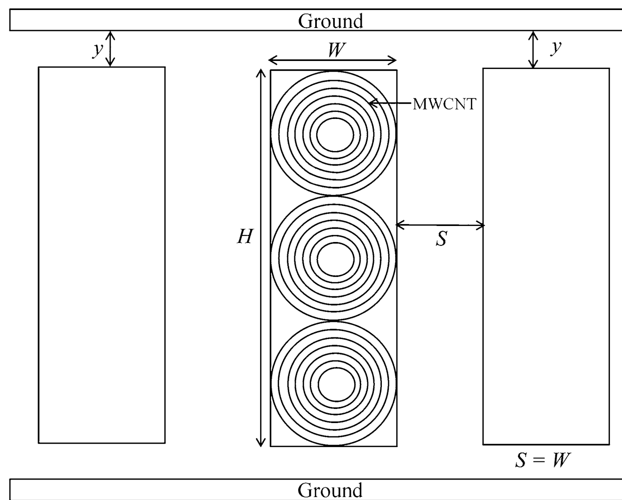
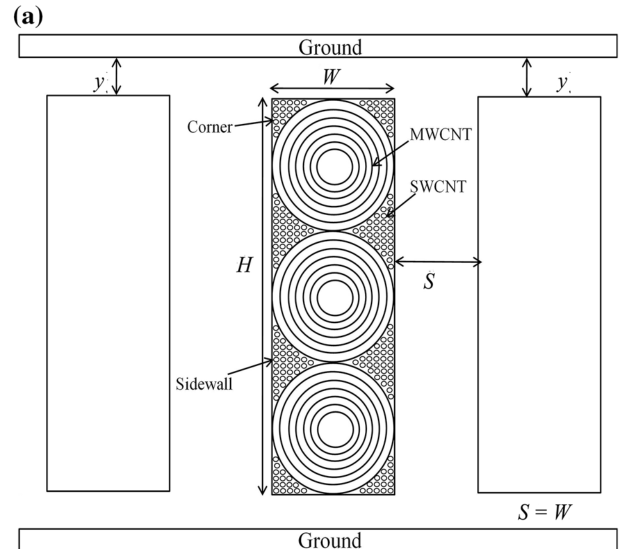
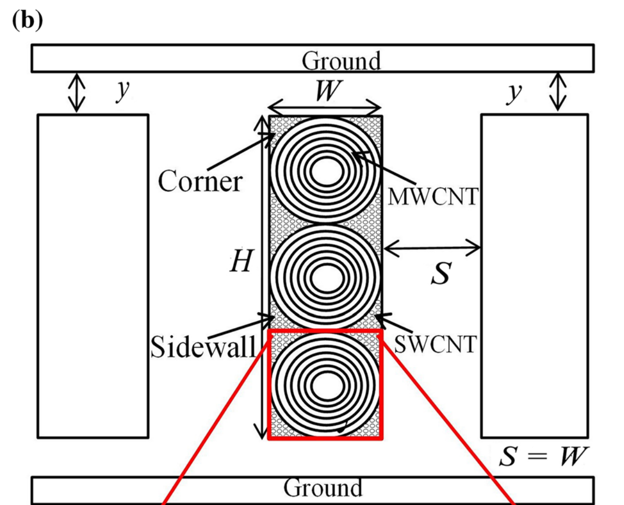


Fig. 3. Structure of a conventional MWCNT interconnect. Reprinted with permission of Ref. 14.

Table I. The interconnect parameters predicted in ITRS 2013 edition[13]

Parameters	Technology node 32 nm	22 nm	16 nm
Width (nm)	40	28	18
Thickness (nm)	120	84	54
Aspect ratio (AR)	3	3	3
Oxide thickness y (nm)	93.6	65.5	40
V_{dd} (V)	0.9	0.8	0.7
Dielectric constant (ε_r)	2.77	2.59	2.31
$D_{ratio}(D_{min}/D_{max})$	0.5	0.5	0.5
ρ_{Copper} ($\mu\Omega$ cm)	3.66	4.2	5.69





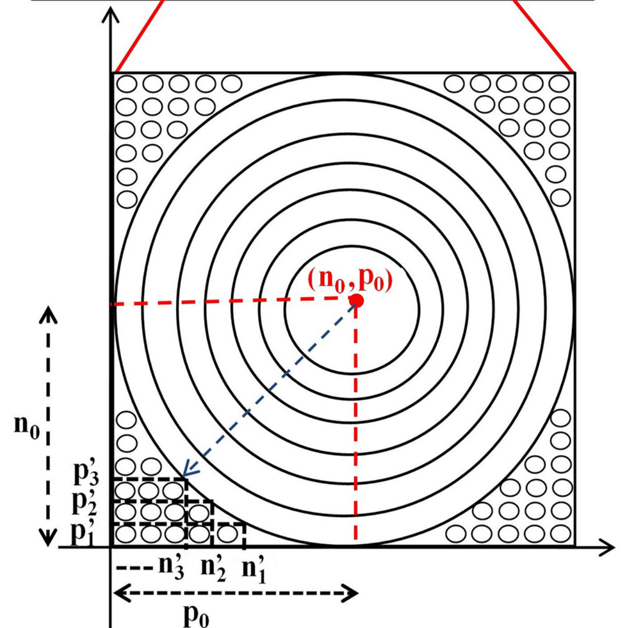


Fig. 4. (a) Structure of the proposed mixed CNT as an interconnect and (b) magnified structure showing the number of SWCNTs inserted at the corners and sidewalls of the MWCNT bundle.

The structure of the proposed mixed CNT as an interconnect, shown in Fig. 4a, contains both types of CNTs, i.e., SWCNTs and MWCNTs. The diameters of SWCNTs and MWCNTs inside the bundle follow the normal distributions depending upon the process control and conditions during CNT synthesis.[2] In the proposed mixed CNT structure, three MWCNTs are connected vertically parallel to each other, and SWCNTs are inserted in the unfilled area surrounding the conventional MWCNT interconnects, i.e., in the sidewalls and corners of the MWCNTs. Due to this insertion of SWCNTs, the overall conductivity of the proposed mixed CNT interconnect increases as the parallel combinations of the newly inserted SWCNTs are also contributing towards the conductivity, which decreases the overall resistance of the interconnect.

The performance of the proposed mixed CNT interconnect structure is analyzed for different interconnect lengths at the 32-nm, 22-nm, and 16-nm technology nodes. As the diameter of the MWCNT is technology dependent, the number of SWCNTs inserted around the MWCNT bundle is also different and technology-dependent. The magnified structure of the mixed CNT interconnect consisting of SWCNTs at the corners and sidewalls of the MWCNT bundle is shown in Fig. 4b. Therefore, the number of SWCNTs to be inserted can be calculated as

$$(n' - n_0)^2 + (p' - p_0)^2 = r^2 \tag{1}$$

where n_0 and p_0 are the center coordinates of the MWCNT and r is the radius of the outermost shell of the MWCNT. The value of n' is calculated for all the values of p', where p' = 1 nm, 2 nm, …, $p_0 - 1$ nm.

The vacant space surrounding the sidewalls and corners of the interconnect is known as a segment. These segments have been filled with SWCNTs. The total number of segments in a structure depends on the aspect ratio (AR) of the interconnect. The total number of segments in the proposed structure will be 4 × AR as shown in Fig. 4b.

The number of SWCNTs in one segment of the proposed structure can be calculated as

$$n_{\mathrm{SWCNT,seg}} = \sum_{p'=1}^{p'=p_0-1} n'_{p'} \tag{2}$$

Therefore, the total number of SWCNTs in the proposed structure is given as

$$n_{\mathrm{SWCNT,total}} = \text{Total number of segments} \times n_{\mathrm{SWCNT,seg}}$$
$$n_{\mathrm{SWCNT,total}} = [4 \times AR] \times n_{\mathrm{SWCNT,seg}} \tag{3}$$

MODELING OF THE PROPOSED MIXED CNT INTERCONNECT STRUCTURE

As discussed in the preceding sections, a mixed CNT is a combination of SWCNTs and MWCNTs. Therefore, to understand the performance of the mixed CNT, there is a need to understand the equivalent impedance model of the MWCNT bundle and SWCNT bundle. The mixed CNT interconnect consists of SWCNTs having similar diameter d and MWCNTs having two or more CNTs with different diameters varying from D_{min} to D_{max} concentrically inserted into each other.

Number of Channels and Shells of an MWCNT Interconnect

Every individual shell of an MWCNT has diameter-dependent conducting channels that allow the movement of electrons within the channel. The formula for calculating the conducting channels in every shell (N_{shell}) can be calculated as:

$$N_{\mathrm{shell}}(D_{\mathrm{i}}) \approx aD_{\mathrm{i}} + b \quad D_{\mathrm{i}} > 3\ \mathrm{nm} \tag{4}$$

where D_{i} represents the diameter of any individual shell of the MWCNT, a = 0.0612 nm^{-1}, and b = 0.425. The ratio of $D_{\mathrm{min}}/D_{\mathrm{max}}$ can be considered from 0.3 to 0.8 and here it is assumed to be 0.5.[15] The number of shells in each MWCNT bundle can be obtained by:

$$u = 1 + \mathrm{Inter}\left[\frac{(D_{\mathrm{max}} - D_{\mathrm{max}}/2)}{2d_s}\right] \tag{5}$$

where 'Inter[.]' considers the integer part only and d_{s} is the spacing between the two adjacent shells (d_{s}= 0.34 nm). The number of shells is to be calculated from the outermost to innermost shell as 1, 2, 3,…, i,…, u (innermost shell). The diameter of any individual shell can be calculated as

$$D_{\mathrm{i}} = D_{\mathrm{max}} - 2\,d_{\mathrm{s}}(i-1) \quad 1 \le i \le u \tag{6}$$

The size of the outermost shell is dependent on the technology node.[3,16,17]

Impedance Parameters for a Mixed CNT Interconnect

On the basis of the impedance parameters of SWCNTs and MWCNTs, an MCC model of a mixed CNT is to be developed.

Resistance

The fundamental resistance of the SWCNT (R_{Fs}) and the MWCNT (R_{Fm}) is the combination of two resistances, i.e., the quantum resistance R_{Q} and scattering resistance R_{S}. For MFP λ more than the interconnect length l, only contact quantum resistance comes into effect. However, the scattering resistance comes into effect when MFP is less than the length of the interconnect.[18] Therefore, the fundamental resistance of the SWCNT is given as[9,19]

$$R_{\mathrm{Fs}} = \frac{h}{4e^2}; \quad l \le \lambda\ (\mathrm{k}\Omega) \tag{7}$$

$$R_{\mathrm{Fs}} = \frac{h}{4e^2}\frac{l}{\lambda}; \quad l > \lambda \ (\mathrm{k\Omega}) \tag{8}$$

Similarly, the fundamental resistance of the MWCNT[15] is given as

$$R_{\mathrm{Fm}} = R_{\mathrm{Q}} + R_{\mathrm{S}} \cdot l = \frac{h}{2e^2N} + \frac{h}{2e^2N}\frac{l}{\lambda}; \ (\mathrm{k\Omega}) \tag{9}$$

where $h/2e^2 = 12.9\ \mathrm{k\Omega}$ and N, l, and λ are conducting channels in a shell, interconnect length, and MFP, respectively. The contact resistance (R_{mc}) arises because of the imperfect metal-CNT contacts and depends upon the growing process; R_{mc} is considered as 2 kΩ.

Inductance

CNTs consist of two types of inductances: magnetic inductance (L_{Ms} for an SWCNT and L_{Mm} for an MWCNT) and kinetic inductance (L_{Ks} for an SWCNT and L_{Km} for an MWCNT). The magnetic and kinetic inductances of a SWCNT are given as[15]:

$$L_{\mathrm{Ms}} = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \ (\mathrm{pH/\mu m}) \tag{10}$$

$$L_{\mathrm{Ks}} = \frac{h}{2e^2 v_{\mathrm{F}}} \ (\mathrm{nH/\mu m}) \tag{11}$$

The magnetic and kinetic inductances of an MWCNT are calculated as:

$$L_{\mathrm{Mm}} = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2y}{D_{\mathrm{i}}}\right) \ (\mathrm{pH/\mu m}) \tag{12}$$

In the MWCNT bundle, each individual shell consists of N_{shell} conducting channels and the shells are connected in parallel to each other. Therefore, the actual kinetic inductance ($L_{\mathrm{K/shell}}$) for each shell of an MWCNT is given as:

$$L_{\mathrm{K}}/\mathrm{channel} = \frac{h}{2e^2 v_{\mathrm{F}}} \cdot \frac{1}{2} \ (\mathrm{nH/\mu m}) \tag{13}$$

$$L_{\mathrm{K}}/\mathrm{shell} = \frac{L_{\mathrm{K}}/\mathrm{channel}}{N_{\mathrm{shell}}} \tag{14}$$

It can be seen from Eqs. 10–14 that the value of magnetic inductance is very large as compared to its kinetic inductance. Therefore, the influence of kinetic inductance on the performance of an MWCNT is insignificantly small.

Capacitance

The capacitances of the mixed CNT interconnects are the combined capacitive effect of the SWCNT and MWCNT capacitances. The capacitances of an SWCNT are of two types: electrostatic capacitance (C_{Es}) and quantum capacitance (C_{Qs}). The MWCNT capacitances are divided into three types: quantum capacitance (C_{Qm}), coupling capacitance (C_{sm}), and electrostatic capacitance (C_{Em}). The capacitances of an SWCNT can be calculated as[15]:

$$C_{\mathrm{Es}} \approx \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2y}{d}\right)}; \quad \text{for } y > 2\mathrm{d} \ (\mathrm{aF/\mu m}) \tag{15}$$

$$C_{\mathrm{Qs}} = \frac{2\mathrm{e}^2}{h v_{\mathrm{F}}} \ (\mathrm{aF/\mu m}) \tag{16}$$

The capacitances of MWCNT are calculated using the following equations[15]:

$$C_{\mathrm{Em}} = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2y}{D_{\max}}\right)}; \quad \text{for } y > 2D_{\max} \ (\mathrm{aF/\mu m}) \tag{17}$$

$$C_{\mathrm{Qm}}/\mathrm{channels} = 2 \times \frac{2\mathrm{e}^2}{h v_{\mathrm{F}}} \ (\mathrm{aF/\mu m}) \tag{18}$$

$$C_{\mathrm{Qm}}/\mathrm{shell} = C_{\mathrm{Qm}}/\mathrm{channels} \times N \tag{19}$$

To find the coupling capacitance between two adjacent shells, the coaxial capacitance formula to be used is shown below:

$$C_{\mathrm{sm}} = \frac{2\pi\varepsilon}{\ln(D_{\mathrm{out}}/D_{\mathrm{in}})} \ (\mathrm{aF/\mu m}) \tag{20}$$

where D_{in} and D_{out} are the diameters of the innermost and outermost shells, respectively, of two neighboring shells of the MWCNT bundle.

MCC Model of the Proposed Mixed CNT Interconnect

An MCC model is a parallel combination of the impedance parameters of all the individual shells of an SWCNT and MWCNT used to form a mixed CNT interconnect. Therefore, the MCC model of the mixed CNT interconnect is a combination of the MCC models of the MWCNT bundle and the SWCNTs. Therefore, using hierarchical modeling, the MCC model of the mixed CNT interconnect is developed as shown in Fig. 5.

In the MCC model of the mixed CNT interconnect shown in Fig. 5, all the impedance parameters of the different shells of the MWCNT bundle interconnects (upper part of Fig. 5) and SWCNTs (lower part of Fig. 5) are represented up to '*u*' and '*v*' shells, respectively. This model is used to compare the performance of the proposed mixed CNT interconnect with that of the MWCNT bundle at a global-level interconnect. In the MCC model of the mixed CNT interconnect, it is shown that the resistances of all shells of the SWCNTs and MWCNT bundle are connected in parallel with each other. This increases the overall conductivity of the interconnect and, hence, reduces the propagation delay and PDP of the mixed CNT interconnect.

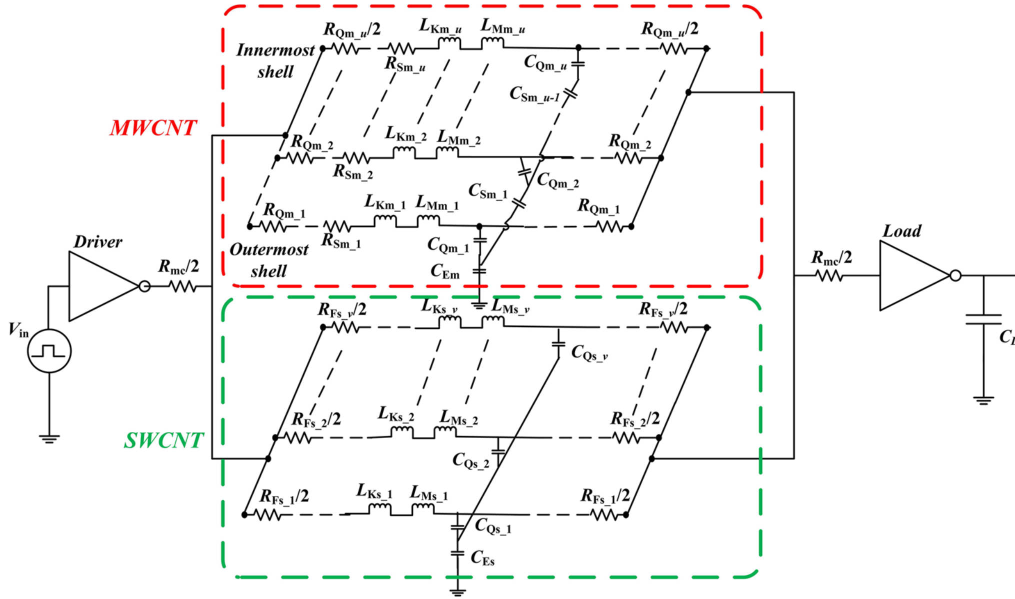


Fig. 5. MCC model of the proposed mixed CNT interconnect.

Realization of the ESC Model from the MCC Model of the Proposed Mixed CNT Interconnect

The MCC model is used to represent the parasitics of all the shells of the SWCNTs and MWCNTs in parallel combination, which becomes a complicated electrical circuit model. The ESC model is used to replace the complicated MCC model of the mixed CNT interconnect to ease the calculations of the impedance parameters. The equivalent impedance parameters of the ESC model are used to evaluate and analyze the performance of the mixed CNT interconnect in terms of propagation delay and PDP.

In the upper part of Fig. 5, all the impedance parameters of the different shells of the MWCNT bundle for the mixed CNT interconnect are represented from 1 to u. It is shown in Fig. 5 that all the shells of the MWCNT bundle are considered parallel to each other. Therefore, the realization of the ESC model for the MWCNT bundle is based on the assumption that all the shells are parallel and separated by a fixed distance, i.e., the Van der Waals distance of 0.34 nm.[20,21] The resultant of the ESC scattering resistance R_{Sm} and quantum resistance R_{Qm} can be calculated by considering the parallel combination of these resistances and is given by:[15]

$$R_{\mathrm{m}}^{-1} = \sum_{i=1}^{u} \left(R_{\mathrm{Qm}_i} + R_{\mathrm{Sm}_i}\right)^{-1} \quad (\text{for } i = 1, 2, \ldots u) \tag{21}$$

Similarly, the magnetic inductance L_{Mm} and kinetic inductance L_{Km} of the ESC can be calculated as:[15]

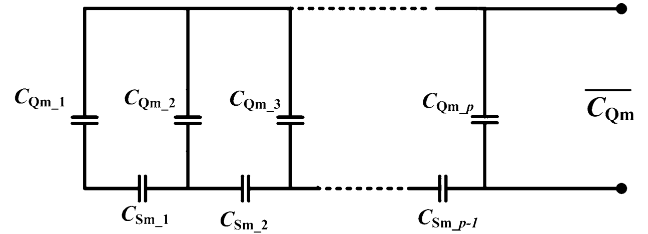


Fig. 6. Simplified circuit for ESC capacitance. Reprinted with permission of Ref. 8.

$$L_{\mathrm{m}}^{-1} = \sum_{i=1}^{u} \left(L_{\mathrm{Km}_i} + L_{\mathrm{Mm}_i}\right)^{-1} \quad (\text{for } i = 1, 2, \ldots u) \tag{22}$$

The calculation of the ESC capacitance is slightly different than that of the resistance and inductance, and a simplified circuit for the calculation of the ESC capacitance is shown in Fig. 6. Let $\overline{C_{\mathrm{Qm}}}$ be the equivalent capacitance, C_{Qm} be the quantum capacitance, and C_{Sm} be the scattering capacitance.

$$\overline{C_{\mathrm{Qm}}} = C_{\mathrm{i}} \tag{23}$$

where C_i is calculated in a recursive way:

$$C_{\mathrm{u}} = C_{\mathrm{Qm_u}} \tag{24}$$

$$C_{\mathrm{i-1}} = \left(C_{\mathrm{i}}^{-1} + C_{\mathrm{Sm_(i-1)}}^{-1}\right)^{-1} + C_{\mathrm{Qm_(i-1)}} \quad (\text{for } i = u \ldots 3, 2) \tag{25}$$

The ESC capacitance is given as:

$$C_{\mathrm{ESC,m}} = \left(C_{1}^{-1} + C_{\mathrm{Em}}^{-1}\right)^{-1} \tag{26}$$

The obtained equivalent values of resistance, inductance, and capacitance (RLC) of the MWCNT are used to develop the ESC model of the proposed mixed CNT interconnect shown in Fig. 7. As shown in the lower part of Fig. 5, all the impedance parameters of the different SWCNTs are represented from 1 to v and connected in parallel to each other in the proposed mixed CNT interconnect. Therefore, the realization of ESC for SWCNTs is based on the assumption that all the SWCNTs are of a similar diameter of 1 nm and connected in parallel to each other. To evaluate the ESC model, expressions for the equivalent impedance parameters of the SWCNTs are derived and are given as:

$$R_{\mathrm{S}} = \frac{R_{\mathrm{F}}}{n_{\mathrm{SWCNT,total}}} \quad (27)$$

Similarly, the equivalent of magnetic inductance (L_{Ms}) and kinetic inductance (L_{Ks}) are given as:

$$L_{\mathrm{S}} = \frac{\mathrm{L}_{\mathrm{Ms}} + L_{\mathrm{Ks}}}{n_{\mathrm{SWCNT,total}}} \quad (28)$$

Similarly, the overall capacitance is given as:

$$\overline{C}_{\mathrm{Qs}} = n_{\mathrm{SWCNT,total}} C_{\mathrm{Qs}} \quad (29)$$

$$C_{\mathrm{ESC,s}} = \left(\overline{C}_{\mathrm{Qs}}^{-1} + C_{\mathrm{Es}}^{-1}\right)^{-1} \quad (30)$$

The obtained ESC impedance parameters (resistance, inductance, and capacitance) of the MWCNT bundle and SWCNTs derived in this section are used to develop the ESC model of the proposed mixed CNT interconnect. The ESC model of the proposed mixed CNT is obtained by combining the ESC model of the SWCNTs and MWCNT bundle as shown in Fig. 7.

In the proposed ESC model, the capacitance known as coupling capacitance $C_{\mathrm{CM\text{-}ESC}}$ experienced between the SWCNT and MWCNT interconnects is:

$$C_{\mathrm{CM-ESC}} = \frac{\pi \varepsilon l}{\cosh^{-1}(s_{\mathrm{p}}/D_{\mathrm{a}})} \quad (31)$$

where S_{p} and D_{a} are the spacing between the two bundled structures and the average diameter of the SWCNT and MWCNT bundle, respectively.

RESULTS AND DISCUSSIONS

This section discusses the performance of the proposed mixed CNT interconnect in terms of propagation delay and PDP at 32-nm, 22-nm, and 16-nm technology nodes for variable interconnect lengths (100 μm to 2500 μm). For comparison, a similar analysis is performed for the MWCNT interconnect. On the basis of this comparison, the best structure suited for future interconnects with optimum propagation delay and PDP is discovered. The propagation delay and PDP are primarily dependent on the parasitics of the MWCNT bundle and mixed CNT interconnects. All the parasitics for different structures at different technology nodes are calculated by using the parameters predicted by the 2013 International Technology Roadmap for Semiconductors (ITRS 2013)[13] as shown in Table I. All parasitics for different technology nodes are obtained by writing the code in MATLAB.

Analyzing an MWCNT as an Interconnect

In this section, the impact of variation of the impedance parameters (resistance, inductance, and capacitance) on delay and PDP is analyzed for the better understanding of the MWCNT. The number of conducting channels in a shell and number of shells in an MWCNT are obtained by using Eqs. 4, 5, and 6. Based on the ESC model of an MWCNT, the different parasitics are calculated for 32-nm, 22-nm, and 16-nm technology nodes. Depending on these calculated parasitics of the MWCNT bundle, the propagation delay and PDP are simulated through the driver interconnect load (DIL) model

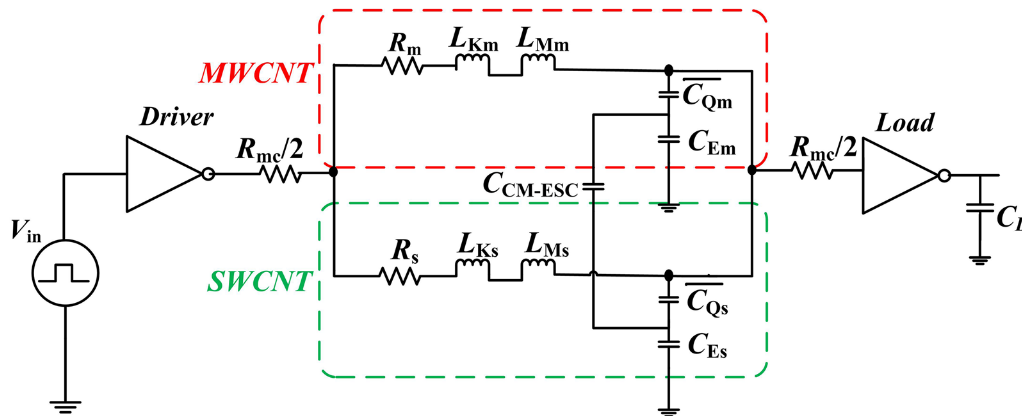


Fig. 7. ESC circuit model for the proposed mixed CNT interconnect.

at DSM technology nodes.[22] All the simulations are performed using the SPICE simulation tool. The model file level 54 obtained from the predictive technology model (PTM) is used for the simulations.[23]

The impact of length and technology scaling on the propagation delay and PDP of an MWCNT is shown in Figs. 8 and 9, respectively. The impedance parameters of an MWCNT increase with increase in interconnect length, which shows a considerable impact on propagation delay and PDP, as shown in Figs. 8 and 9. It is observed from the figures that the propagation delay and PDP are increasing exponentially while the interconnect length is increasing linearly. This is because the rate of increase in the impedance parameters product with respect to length is also exponential, which results in an exponential increase in delay.

However, the effect of scaled down technology nodes on the propagation delay is somewhat different. The results reveal that with scaled down technology nodes, the propagation delay increases as shown in Fig. 8. It is observed that the rate of increase in propagation delay is high for the 16-nm technology node as compared to the 32-nm technology node as shown in Fig. 8.

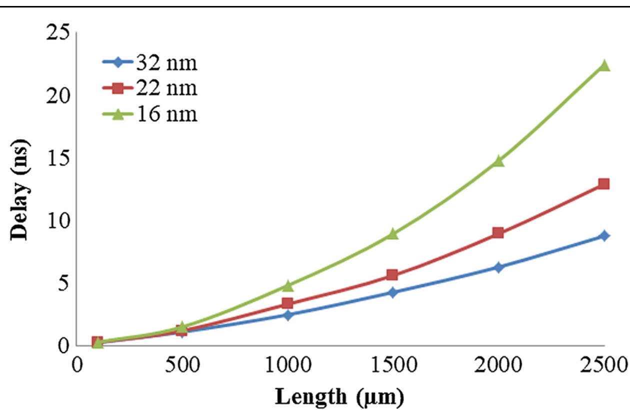


Fig. 8. Propagation delay of an MWCNT for variable interconnect length at different technology nodes.

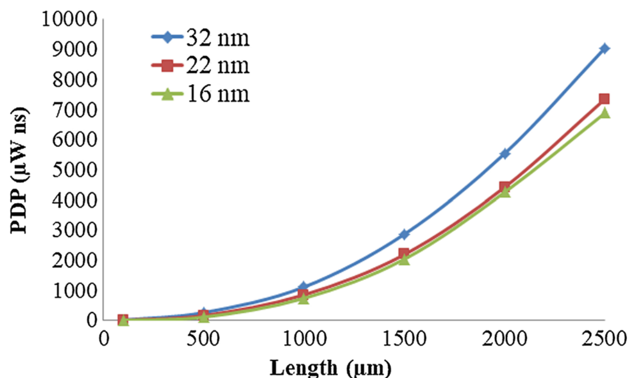


Fig. 9. PDP of an MWCNT for different interconnect lengths at different technology nodes.

Analyzing the Proposed Mixed CNT Interconnect as an Interconnect

The impedance parameters for the proposed mixed CNT interconnect are obtained as per the need of the required structure shown in Fig. 4. The structure is a combination of an SWCNT and MWCNT and its parameters are obtained by using Eqs. 4–20, and an MCC model is realized as shown in Fig. 5. Based on the MCC model, an ESC model is derived by using Eqs. 21–29 and 31 as shown in Fig. 7.

By considering the predefined ITRS parameters (as shown in Table I) for a mixed CNT, the impact of insertion of SWCNTs around the MWCNTs on the impedance parameters, propagation delay, and PDP is presented in this section. On the basis of the calculated parasitic, the performance in terms of delay and PDP for the mixed CNT is simulated by using a setup similar to that used to simulate the MWCNT bundle, as described in "Analyzing an MWCNT as an Interconnect" section. The estimated performance of delay and PDP of the mixed CNT interconnect for variable interconnect lengths (100–2500 μm) at 32-nm, 22-nm, and 16-nm technology nodes is summarized in Table II.

The performance of the mixed CNT interconnect in terms of delay and PDP for different interconnect lengths (from 100 μm to 2500 μm) at different technology nodes is shown in Figs. 10 and 11, respectively.

Figures 10 and 11 reveal that the rates of variation in propagation delay and PDP are exponential when the length increases linearly. The result also reveals that the rate of change of propagation delay is high for scaled-down technology nodes, i.e., smaller technology nodes have a sharper rise in delay.

Comparative Analysis of an MWCNT and the Proposed Mixed CNT Interconnect

A comparative analysis in terms of propagation delay and PDP of the MWCNT and proposed mixed CNT interconnects using the equivalent RLC parameters of both interconnects at different DSM technology nodes is presented in this section. The comparison of propagation delay at 32-nm, 22-nm, and 16-nm technology nodes between the MWCNT and proposed mixed CNT interconnects is summarized in Table III and shown in Fig. 12.

From Table III and Fig. 12a, b, c, it is observed that the proposed mixed CNT interconnect offers lesser propagation delay as compared to the MWCNT interconnect for all the technology nodes. It is revealed that the gap between the propagation delay of the MWCNT and the proposed mixed CNT interconnects increases as the interconnect length increases from 100 μm to 2500 μm.

Further, it is also predicted from Fig. 12d that there is a considerable difference of propagation delay at the 16-nm technology node as compared to

Table II. Delay and PDP for mixed CNT for different interconnect lengths (100–2500 μm) at different technology nodes

	Delay of mixed CNT interconnect (ns)			PDP of mixed CNT interconnect (μW ns)		
Length (μm)	32 nm	22 nm	16 nm	32 nm	22 nm	16 nm
100	0.2228	0.2074	0.2421	13.6802	7.2486	6.0765
500	1.0735	1.1495	1.4051	246.499	152.326	109.357
1000	2.2103	2.9826	4.0773	985.3044	783.535	634.305
1500	4.0699	5.1561	7.9434	2719.77	2087.72	1845.77
2000	5.9853	8.3436	13.1263	5253.862	4180.41	3880.42
2500	8.2443	11.9932	19.1412	8484.646	6967.27	6223.9

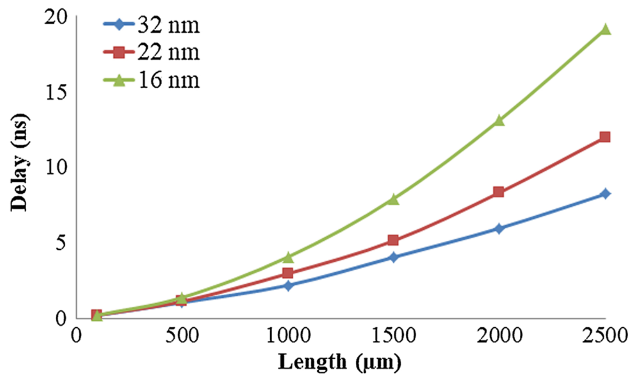


Fig. 10. Variation of delay in a mixed CNT interconnect at different lengths for different technology nodes.

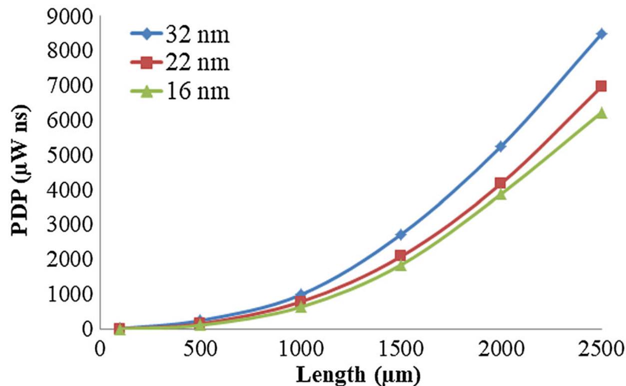


Fig. 11. Variation of PDP in a mixed CNT interconnect at different lengths for different technology nodes.

the 32-nm technology node for interconnect lengths larger than 1500 μm. Therefore, it is projected that the mixed CNT interconnect offers better performance in terms of delay, particularly for DSM technology nodes for global-level interconnect lengths.

The comparison of PDP between the MWCNT and mixed CNT interconnects at the 32-nm, 22-nm, and 16-nm technology nodes is provided in Table IV and shown in Fig. 13a, b, c, and d.

Table IV shows that the optimum values for the PDP are obtained for the mixed CNT interconnect at the 16-nm technology node for all the interconnect lengths as compared to the other two technology nodes under consideration, as shown in Fig. 13a, b, c. Further, from Fig. 13d, it is observed that the difference between the PDP of the MWCNT and the proposed mixed CNT interconnects increases with the increase in interconnect length at the 32-nm, 22-nm, and 16-nm technology nodes. Similarly, the PDP of the proposed mixed CNT interconnect is less than that of the MWCNT interconnect for all the technology nodes. Therefore, from the comparative analysis, it is observed that the proposed mixed CNT interconnect performs better than the MWCNT bundle.

This can be inferred from the fact that for a given cross-sectional dimension of the conventional MWCNT bundle at any technology node, a portion of free space is left owing to large outermost shell diameters, thus inadequately utilizing the space, because of which the number of overall conducting channels is less. This free space has been utilized by inserting SWCNTs in the proposed model of a mixed CNT interconnect, which increases the number of overall conducting channels. Therefore, the overall conductivity of the proposed mixed CNT interconnect has been increased, which reduced the propagation delay, power dissipation, and PDP for the mixed CNT interconnect as compared to the MWCNT interconnect.

CONCLUSION

This paper presents an analysis of the performance of the mixed CNT interconnect for DSM technology nodes. It is observed that the overall conductivity of the MWCNT bundle as an

Table III. Combined comparative analysis of delay for an MWCNT and mixed CNT interconnect for different technology nodes

	32 nm		22 nm		16 nm	
Length (μm)	MWCNT delay	Mixed CNT delay	MWCNT delay	Mixed CNT delay	MWCNT delay	Mixed CNT delay
100	0.2337	0.2228	0.2294	0.2074	0.2801	0.2421
500	1.0949	1.0735	1.1847	1.1495	1.4914	1.4051
1000	2.4647	2.2103	3.3144	2.9826	4.7991	4.0773
1500	4.2628	4.0699	5.5971	5.1561	8.9295	7.9434
2000	6.2741	5.9853	8.9331	8.3436	14.761	13.1263
2500	8.7507	8.2443	12.8722	11.9932	22.4175	19.1412

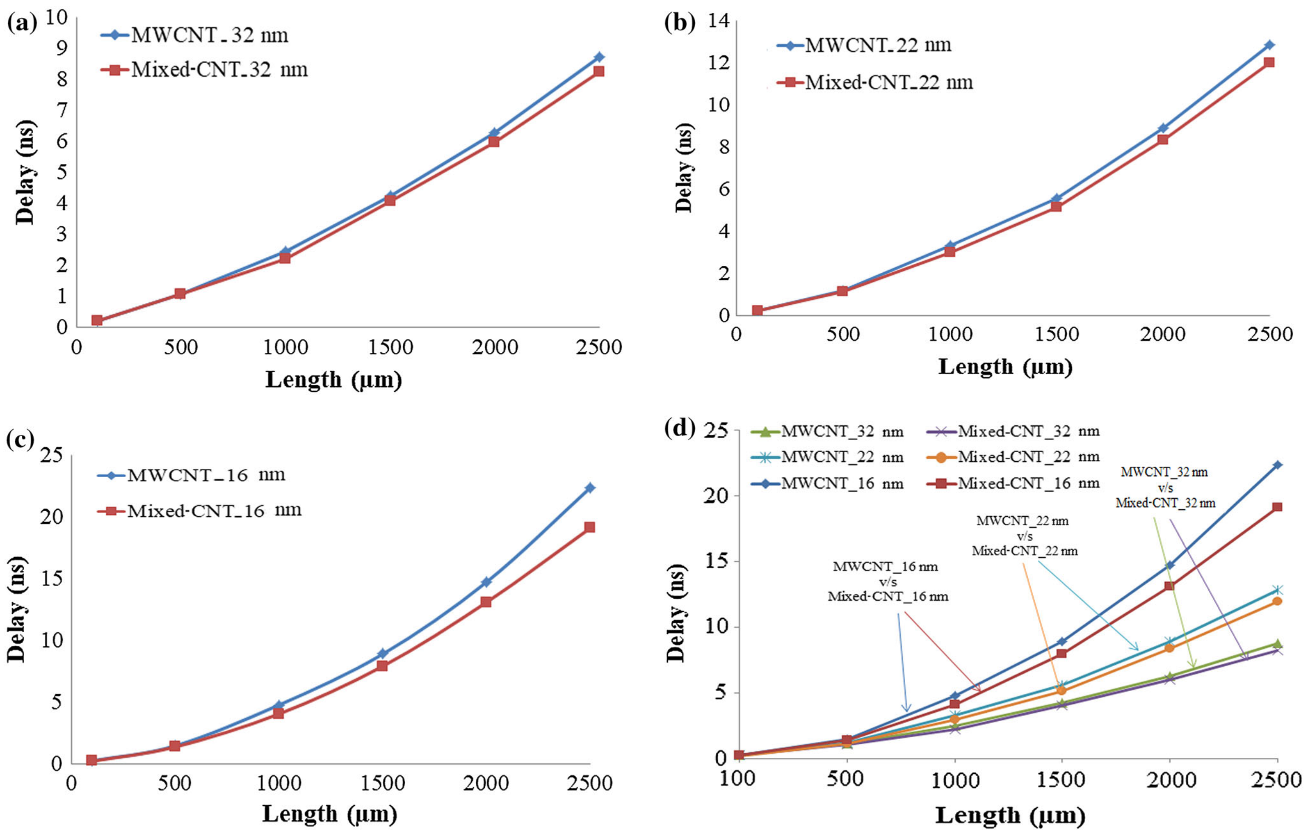


Fig. 12. Comparison of propagation delay of an MWCNT and mixed CNT interconnects for (a) 32-nm, (b) 22-nm, and (c) 16-nm technology nodes and (d) combined comparative analysis of an MWCNT and mixed CNT interconnects for different technology nodes.

interconnect can be increased by inserting SWCNTs at the sidewalls and corners of the MWCNT. The performance of the mixed CNT in terms of propagation delay and PDP is evaluated for different interconnect lengths (from 100 μm to 2500 μm) using the impedance parameters of the proposed ESC model. The results reveal that with increase in the interconnect length, the propagation delay and PDP also increase. To compare the obtained results, a similar analysis is performed for the MWCNT as interconnects. The comparative analysis indicates that the propagation delay and PDP is better for the proposed mixed CNT as compared to the MWCNT interconnects for all the technology nodes under consideration. The gap between the proposed mixed CNT and MWCNT interconnects increases for

Table IV. Comparative analysis of PDP for MWCNT and mixed CNT at different technology nodes

	PDP (μW ns)					
	32 nm		22 nm		16 nm	
Length (μm)	MWCNT	Mixed CNT	MWCNT	Mixed CNT	MWCNT	Mixed CNT
100	14.825	13.6802	8.4019	7.2486	6.7991	6.0765
500	260.48	246.499	163.18	152.326	112.080	109.357
1000	1112.235	985.3044	849.62	783.535	736.222	634.305
1500	2869.12	2719.77	2192.30	2087.72	2039.05	1845.77
2000	5539.89	5253.862	4420.97	4180.41	4254.94	3880.42
2500	9051.93	8484.646	7355.21	6967.27	6887.41	6223.90

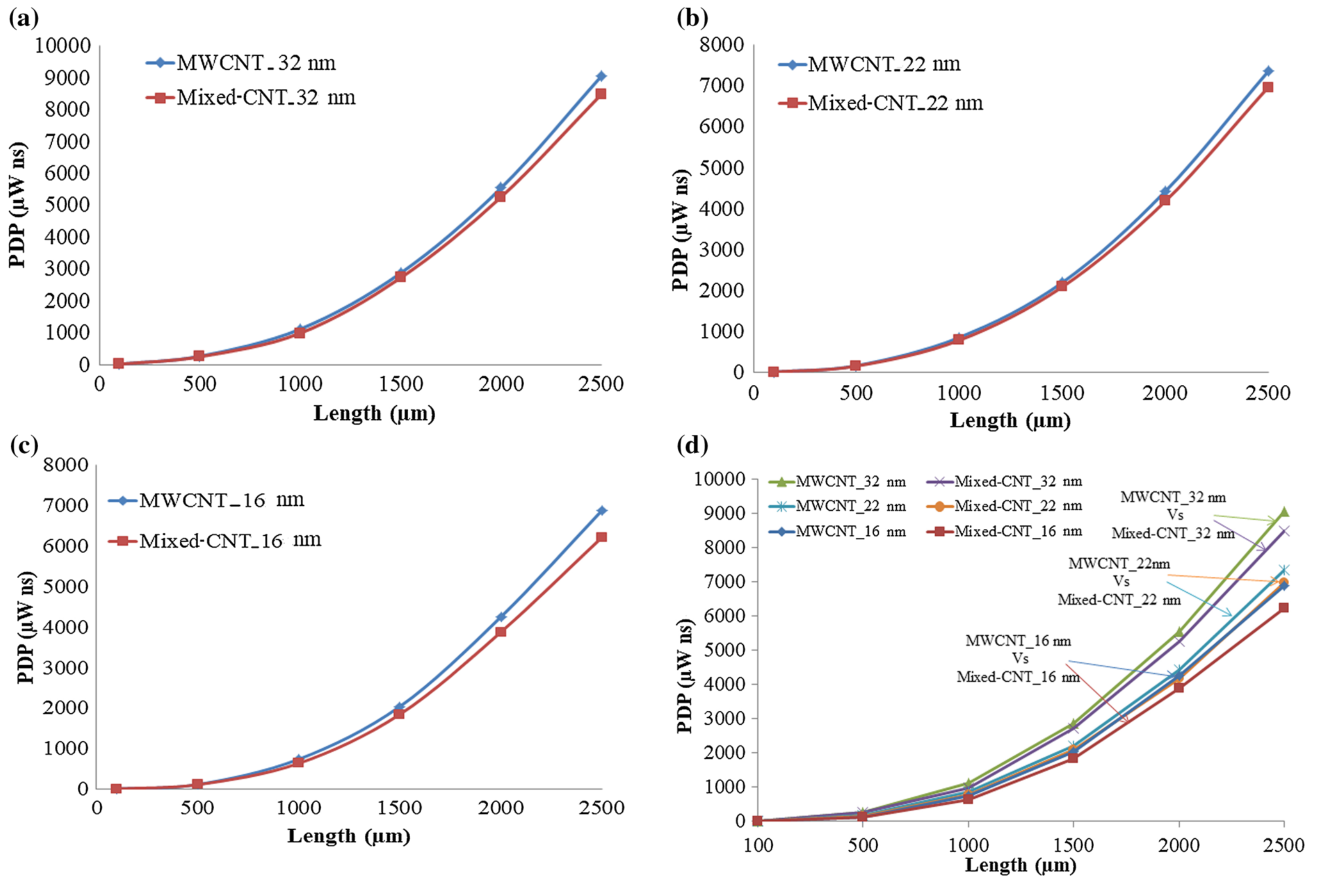


Fig. 13. Comparison of PDP of the MWCNT and proposed mixed CNT for (a) 32-nm, (b) 22-nm, and (c) 16-nm technology nodes. (d) Combined comparative analysis of an MWCNT and proposed mixed CNT interconnects for different technology nodes.

scaled-down technology nodes at larger interconnect lengths. Therefore, the proposed mixed CNT interconnect can be considered as the most suitable interconnect material at global-level interconnect lengths for next-generation VLSI-IC design fabrications.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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