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Impact of *In Situ* Annealing Time on CdTe Polycrystalline Film and Device Performance

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We studied the impact of *in situ* post-growth annealing process on cadmium telluride (CdTe) polycrystalline thin film in this work. Samples of different annealing times have been characterized by x-ray diffraction (XRD) and a scanning electron microscope (SEM). The optoelectronic properties of CdTe film were deeply studied with light I–V testing, external quantum efficiency (EQE) and photoluminescence (PL)/time-resolved photoluminescence (TRPL) measurements. It is found that the *in situ* post-growth annealing treatment has a great effect on cadmium sulfide (CdS)/CdTe intermixing as well as interface pinholes. Elementary correlations between annealing time, film and junction morphology, carrier lifetime and device performance were investigated, and the annealing time turns out to be crucial to CdTe device performance. Solar cells with CdTe polycrystalline thin film annealed *in situ* at 550°C/550°C for 10 min show the best performance. With the help of precisely controlled annealing time, better CdTe film microstructure and morphology can be realized after *in situ* post-growth annealing.

Key words: CdTe solar cell, *in situ* annealing, TRPL

INTRODUCTION

CdTe has long been recognized to be one of the most promising photovoltaic materials. The highest reported and certified efficiency for solar cells with CdTe absorber layers is 21.5%.[1] Various methods have been developed to deposit CdTe thin film, like vapor transport deposition (VTD), close-spaced sublimation (CSS), electro deposition (ED), physical vapor deposition (PVD), sputtering, etc.[2–4] Among these methods, CSS is one of the simplest ways to deposit CdTe thin film and many different groups have already achieved high efficiency by this method.[5–8] Controlling both high-quality CdTe polycrystalline thin film and *p–n* heterojunction interfaces with less pinholes is the key to realizing high performance CdTe-based solar cells based on CdS/CdTe structure.[9] Huge efforts have been made by scientists on optimizing the growth processes to get a better device performance. A great deal of attention has been paid on the source/substrate temperatures, oxygen partial pressure and so forth in CdTe deposition, and each of these parameters has great impact.[10] Besides the above well-known parameters, our previous results show that the heating and cooling processes before and after CdTe deposition have some non-negligible influences on film property and device performance. The interdiffusion between CdS and CdTe plays a significant role in formation of a good junction. But the intermixing is usually not enough due to the fast deposition of CdTe films. *In situ* annealing is thus used to promote the intermixing of CdS/CdTe, which reduces the lattice mismatch and the mismatch induced stress. Inappropriate thermal processes lead to excessive intermixing of CdS/CdTe and the

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advent of pinholes, which are detrimental to device performance. It is important to figure out whether *in situ* annealing treatment has a direct influence on interface pinholes or not. However, the research in this respect has rarely been reported. In this paper, the impact of *in situ* annealing time on structural and optoelectronic properties of CdTe film has been investigated. It is interesting to find that *in situ* annealing time really has an obvious effect on CdTe minority carrier lifetime and the cross-sectional morphology of CdS/CdTe interfaces, which was demonstrated to influence CdTe performance.

EXPERIMENT

CdTe Growth and Post-growth Processing

The device structure of the cells in this study is shown in Fig. 1. Fluorine doped tin oxide (FTO) film was deposited on 3.2 mm soda lime glass by metalorganic chemical vapor deposition (MOCVD). Chemical bath deposition (CBD) technique is used for the deposition of the CdS film and the thickness is about 80 nm. The CdTe polycrystalline thin film was then grown on CdS to a thickness of 2–3 μm by CSS, in which process the source/substrate temperature is 620°C and 550°C. The CSS system pressure in the deposition process is fixed at 2.13 kPa in an oxygen and helium atmosphere. The samples were divided into four groups to study the effect of different annealing times of *in situ* post growth annealing. Right after the CdTe deposition, we maintained both the source/substrate temperature at 550°C and annealed the samples at four levels: 0 (as-deposited), 10 min, 20 min and 40 min. All the samples were subjected to the same $CdCl_2$ treatment and turned into solar cells by depositing onto a layer of Au (100 nm) by the method of vacuum evaporation. ZnTe: Cu back contact was not performed in order to build an almost same baseline for all samples.

Characterization Methods

Film micro-structure and CdS/CdTe junction properties were studied using XRD, SEM and PL/TRPL. Low temperature PL emission measurements were carried out with a FLS-980 fluorescence spectrometer (Edinburgh Instruments) equipped with a 450 W Xeon light source and double excitation monochromators. The TRPL decay curves were obtained by time correlated single photon counting (TCSPC) methodology,[11] which utilized excitation with 98 ps pulses at 633 nm, 3 mW on average power and 4 MHz laser repetition rate. The laser source comes from a Nd: YAG laser modulated by the Acousto-Optical Tunable Filter (AOTF) system. The absorption depth is approximately 200 nm,[10] thus PL and TRPL measurements from the glass side could be applied to characterize the CdS/CdTe region.

Light I–V testing under 100 mW/cm^2 AM1.5 illumination condition and EQE measurements were operating at 25°C to determine solar cell photoelectric properties. Solar cell data were collected and used to establish a correlation between annealing condition and device performance.

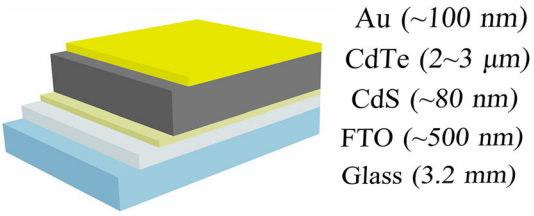

Fig. 1. Device structure of CdTe solar cells.

RESULTS AND DISCUSSION

Structure Properties of CdTe Films

In this part, the effect of *in situ* post-growth annealing time on structure properties of CdTe films was investigated. Annealing time is an important parameter among the post-treatment parameters on CdTe thin film. After the deposition of CdTe polycrystalline thin film by CSS technique, we kept the substrate/source temperature both at 550°C and annealed the samples for four different time durations: 0 (as-deposited), 10 min, 20 min and 40 min. XRD patterns and SEM micrographs of the sample surfaces are shown in Figs. 2 and 3. The texture coefficient (TC) of each (hkl) plane is calculated according to the following formula[12]

$$\mathrm{TC}_{(h_ik_il_i)} = \frac{I_{(h_ik_il_i)}}{Io_{(h_ik_il_i)}} \left\{ \frac{1}{N} \sum_{i=1}^{N} \frac{I_{(h_ik_il_i)}}{Io_{(h_ik_il_i)}} \right\}^{-1}, \qquad (1)$$

where $I_{(h_ik_il_i)}$ is the intensity of $h_ik_il_i$ diffraction peak on the sample; $Io_{(h_ik_il_i)}$ is the intensity of $h_ik_il_i$ plane

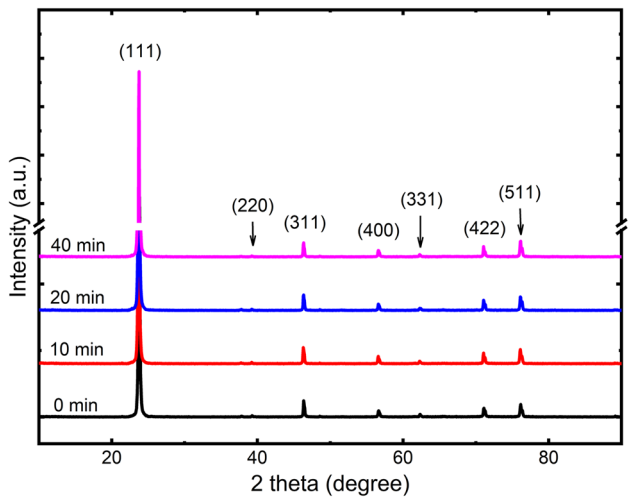

Fig. 2. XRD patterns of CdTe polycrystalline thin films annealed at 550°C for four durations.

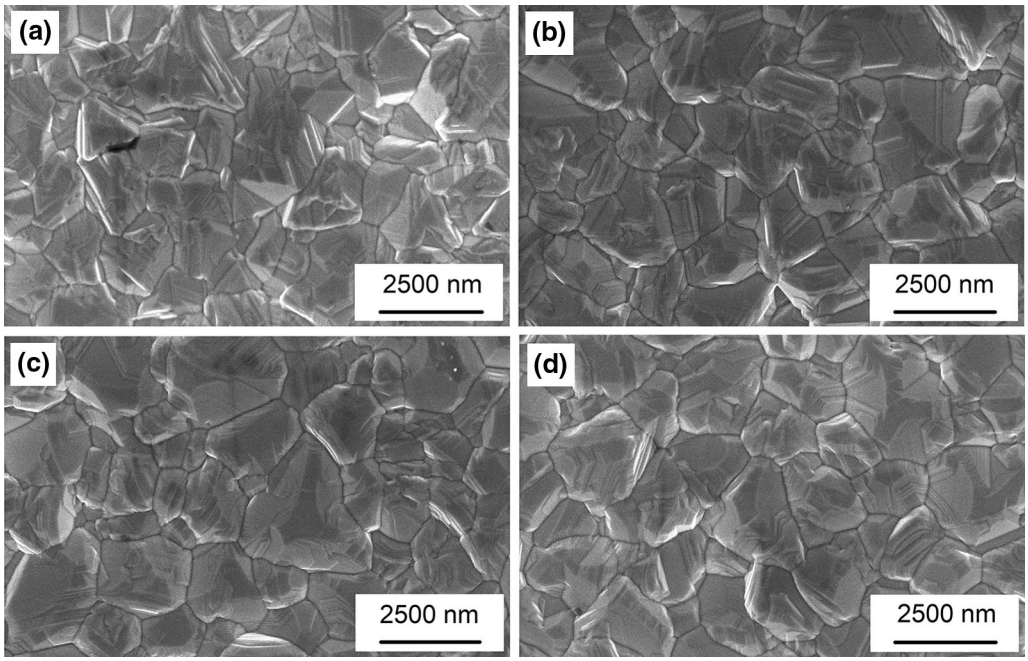

Fig. 3. SEM micrographs of CdTe polycrystalline thin films annealed at 550°C for four durations: (a) 0 min, (b) 10 min, (c) 20 min, (d) 40 min.

Table I. TCs of CdTe polycrystalline thin films annealed *in situ* for four durations

	TCs						
Annealing time (min)	**(111)**	**(220)**	**(311)**	**(400)**	**(331)**	**(422)**	**(511)**
0	5.53	0.02	0.40	0.70	0.15	0.58	1.61
10	5.51	0.02	0.37	0.76	0.16	0.60	1.59
20	5.52	0.02	0.36	0.70	0.18	0.62	1.61
40	5.72	0.01	0.29	0.65	0.14	0.47	1.71

on a completely random sample taken from a powder diffraction file card; N is the number of diffractions considered in the analysis. The determined TCs are given in Table I.

It is clear to see from Fig. 2 and Table I that when the annealing temperatures are the same (550°C), there is virtually no crystallinity discrepancy in all the four cases and basically all films prefer orientation along (111). When the annealing time is less than 40 min, the TC of samples along (111) is around 5.5 and increases to 5.7 for the 40 min case. It is considered that CdTe polycrystalline thin films show almost the same degree of preferred orientation after annealing for different time durations. We analyzed the SEM micrographs of thin film surfaces in Fig. 3 by ImageJ.[13] The average grain sizes for samples annealed for 0 min (as-deposited), 10 min, 20 min, 40 min are 1.64 μm, 1.88 μm, 1.92 μm, 2.33 μm, respectively. From the above results, we know that the *in situ* annealing treatment promotes the grain growth to some extent, which is predictable since the annealing time is short and the temperature is not very high. It has been widely reported that the CdTe grain size plays a crucial role in improving the device performance.[14–17] And an *ex situ* annealing process called $CdCl_2$ treatment has been proved to be one of the most effective ways to promote CdTe recrystallization and increase the grain size.[14] But the device performance in this study should not be simply improved by larger grains because the grain sizes of CdTe films in four annealing cases are very close. As the intermixing of CdS/CdTe is a nonnegligible issue which affects the device performance, it is meaningful to further investigate the influence of *in situ* annealing on the interface properties. Therefore, we turned to cross-sectional SEM and characterized the CdS/CdTe interface microstructure.

Cross-sectional SEM images of a FTO/CdS/CdTe junction annealed for different durations are shown in Fig. 4. The length of interface studied in each image is 3 μm and the thickness of interface area is 200 nm. Pinholes were circled on four interfaces (red dotted circles) and their numbers on the 3 μm × 200 nm interface area are 6 (+ 2), 2 (+ 1), 13 (+ 3) and 18 (+ 3), respectively. For the as-

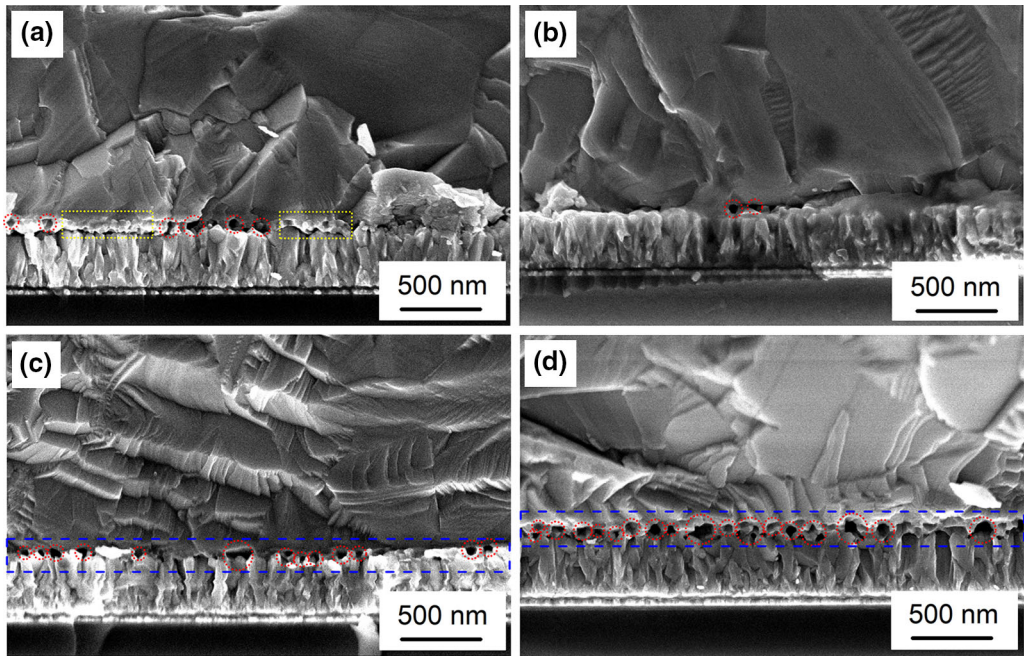

Fig. 4. Cross-sectional SEM micrographs of FTO/CdS/CdTe, with CdTe polycrystalline thin films annealed at 550°C for four durations: (a) 0 min, (b) 10 min, (c) 20 min, (d) 40 min. Pinholes are labelled by red dotted circles, CdS layers are labelled by yellow dotted squares. Chemical intermixing regions are labelled by blue dotted squares (Color figure online).

deposited group, some parts of the CdS layer can still be clearly spotted by yellow dotted squares in Fig. 4a. It appears obvious that the CdS layer has already began diffusing into CdTe during the CdTe deposition. The advent of six pinholes is considered to be the result of nonuniformity of the very thin CdS layer (80 nm). When annealed for 10 min, CdS/CdTe intermixing is more sufficient and the interface becomes coherent with only two pinholes, and we think that a good CdS_xTe_{1-x} thin film is formed. With an annealing time of 20 min and 40 min, too much intermixing happens and leads to 13 and 18 pinholes respectively, which have been reported to cause the deterioration in cell performance.[18] Pinholes are sure to be harmful, and it is believed that devices made from 10 min annealed thin films will have higher cell performance because of the better interface morphology brought by suitable CdS/CdTe intermixing.

Optoelectronic Properties of CdTe Solar Cells

In this part, we tried to establish a correlation between annealing time and properties of thin films and device performance by SEM, EQE and PL/TRPL measurements. All the samples were naturally cooled (18°C/min) and subjected to the same $CdCl_2$ treatment. The processed samples were made into devices by depositing an Au layer as real conductor. Photovoltaic properties of the devices were measured and shown in Fig. 5.

Compared to the as-deposited samples, the solar efficiency (η) increases for all cells treated with *in situ* post-growth annealing. It is because that the *in situ* annealing treatment causes strain relaxation and promotes CdS/CdTe intermixing, which is beneficial to the forming of a better junction.[18] But the efficiency against annealing time is not monotonically increasing. Devices from thin films annealed for 10 min show the best average efficiency as they are supposed to. For the devices which received *in situ* annealing treatment, their performance parameters known as open circuit voltage (V_{OC}), fill factor (FF), and short current density (J_{SC}), are all improved to different extents. As the CdTe crystallinity does not seem to vary a lot for the four groups and the grain size difference is also small, the device performance is thought to be more dependent on the interface morphology. Combining the cross-sectional SEM images with the photovoltaic parameters, we notice that *in situ* annealing treatment is essential to improve the device performance mainly by promoting the intermixing of CdS/CdTe and releasing the mismatch-induced stress there. With the annealing time increasing, the CdS layer gradually diffuses into CdTe and forms an activated junction. However, too long annealing is not advisable. From Fig. 4d we can see that excessive *in situ* annealing treatment (40 min) causes plenty of clearly visible pinholes, which lead to a high density of weak diodes and poor device performance. Higher J_{SC} was measured from all *in situ* post-growth annealing processed solar cells as compared to the as-deposited one. EQE measurements are made to figure out the difference between as-deposited and *in situ* annealed cells on quantum efficiency (QE).

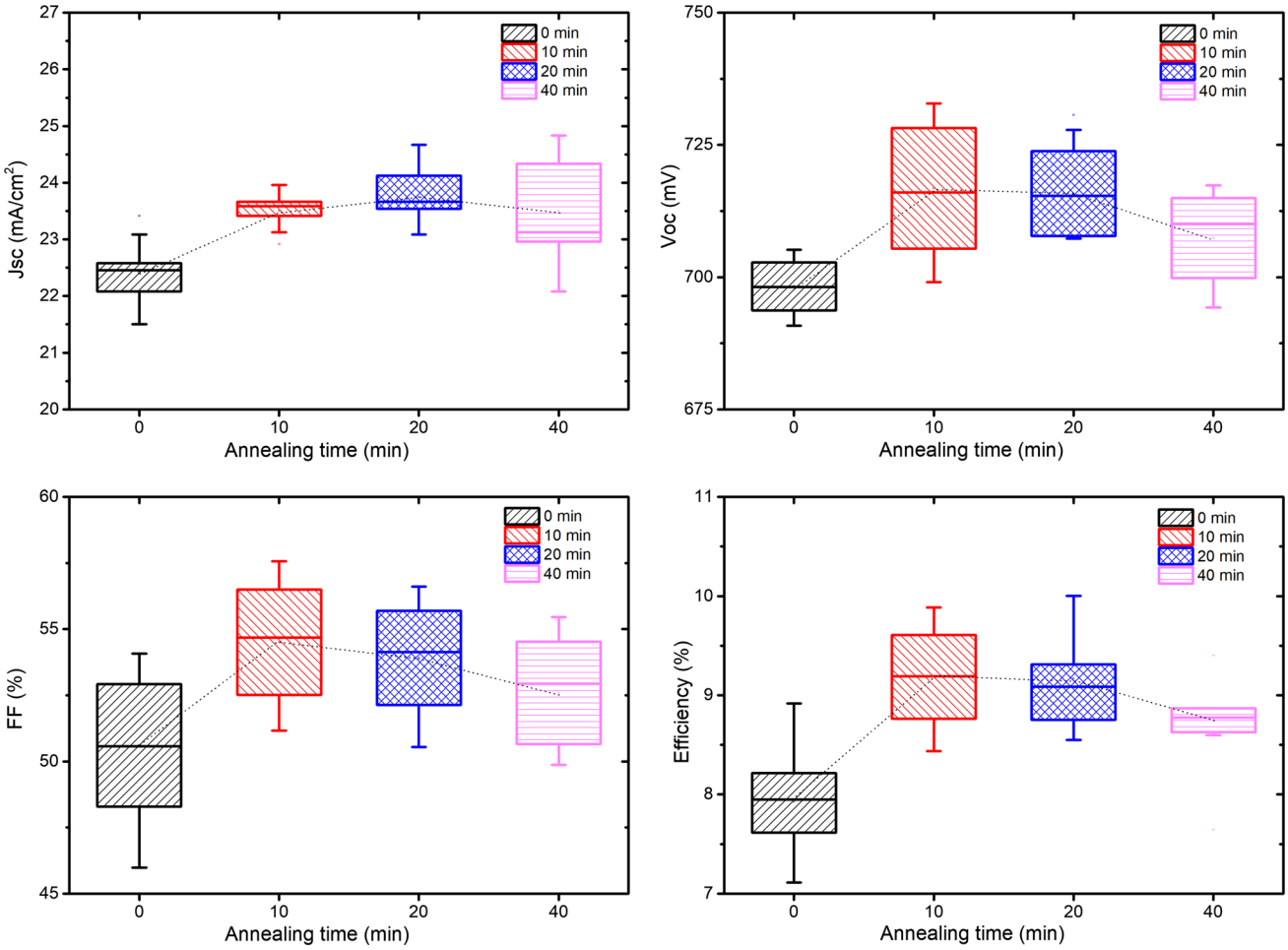

Fig. 5. Photovoltaic properties of the cells, with CdTe polycrystalline thin films annealed at 550°C for four durations: (a) 0 min, (b) 10 min, (c) 20 min, (d) 40 min.

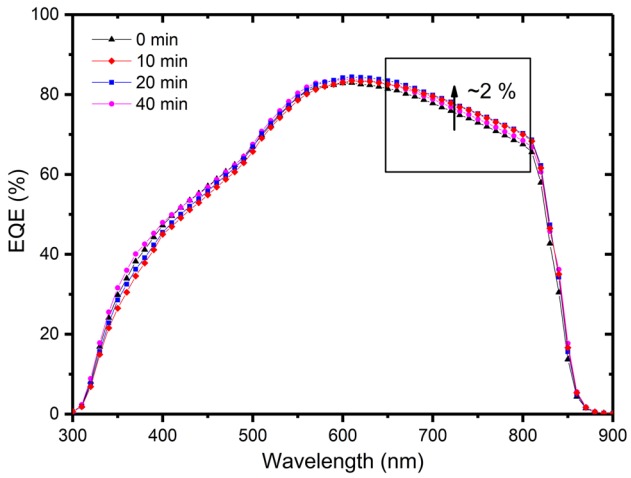

Fig. 6. EQE of the cells, with CdTe polycrystalline thin films annealed at 550°C for four durations.

The EQE for the four groups of cells is depicted as a function of wavelength in Fig. 6. At wavelengths of 650–800 nm, the spectral responses for devices annealed for 10 min, 20 min and 40 min are better than the as-deposited case. As we have already analyzed from Fig. 3, longer *in situ* annealing treatment brings larger grain and decreases the photo-generated carrier recombination as reduced grain boundaries. That is one of the reasons for the increase of QE. Meanwhile, more intermixing of CdS/CdTe and the formation of $CdS_{1-x}Te_x$ thin film with moderate annealing treatment would also promote the QE.[19] The lower QE for the 40 min annealing case may due to the poor interface with more pinholes that lead to a loss in carrier transportation and collection. The EQE improvement of about 2% brought by *in situ* post-growth annealing could be crucial to high efficiency CdTe solar cells.

It has been reported that inter-diffusion at the CdS/CdTe surface leads to the reduction of the lattice mismatch and increases the width of the depletion region.[4,20] To develop a deep understanding of what happened at the CdS/CdTe interface after *in situ* annealing treatment, PL spectra from the glass side were measured and shown in Fig. 7, which can provide us some information of the interface area. According to Ref. 21, the 1.35–1.50 eV band in the spectrum can be ascribed to a

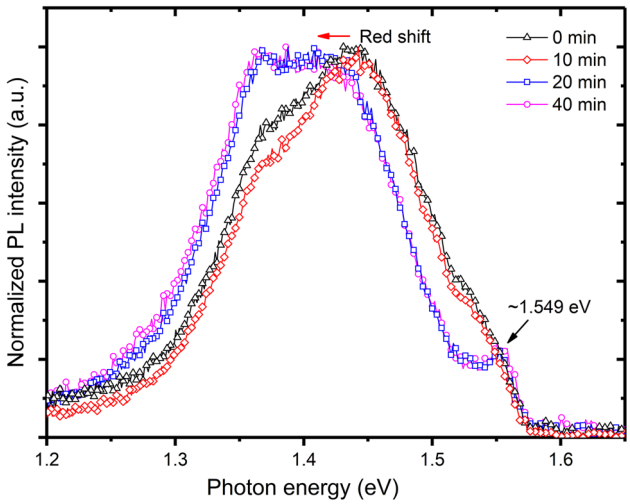

Fig. 7. Normalized PL intensity of CdS/CdTe junction at low temperature, with CdTe polycrystalline thin films annealed at 550°C for four durations.

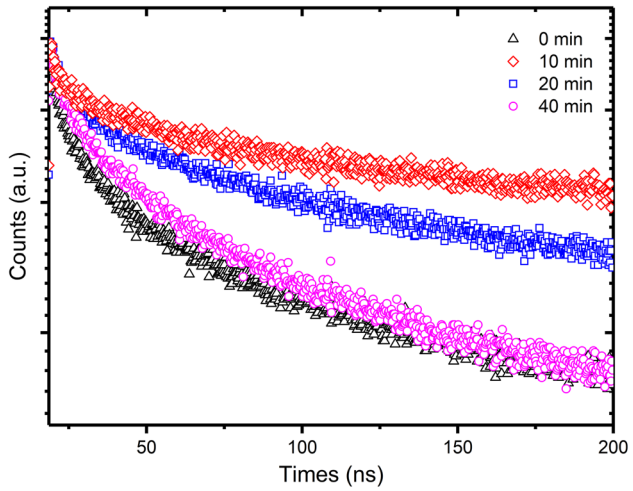

Fig. 8. Photoluminescence decay curves of CdS/CdTe annealed at 550°C for four durations.

superposition of two PL lines: The Y-line and the A-center DAP (donor–acceptor pair) recombination. For the junction with 20 min and 40 min *in situ* annealed CdTe, the stronger PL intensity than the as-deposited and 10 min annealed films at the defect band indicates that more shallow defects form at the interface with longer annealing time. The slightly red shift of the 20 min and 40 min line suggests a decrease in the band gap, which means more S has diffused into the CdTe.[22,23] The peak at 1.549 eV for 20 min and 40 min annealed samples has been assigned to longitudinal phonon replicas for exciton peaks.[21] The appearance of this peak means that longer *in situ* annealing time leads to higher CdTe crystal quality, which coordinates well with the observed larger average grain size from SEM images. The 40 min line shows almost the same shift as the 20 min line, which manifests that they have the same extent of S diffusion. This result supports the blue dotted square signed area in Fig. 4 that nearly all CdS is consumed in the 20 min and 40 min annealed samples and more pinholes emerge. In this way, PL measurement is supposed to be a good method to ascertain the extent of CdS/CdTe inter-diffusion.

For further study the photoelectronic properties of CdS/CdTe cells, we used TRPL to analyze charge carrier transportation and recombination from the FTO/CdS/CdTe side. The 633 nm illumination was adopted, the analysis depth is about 200 nm and the decay curves are more affected by the CdS/CdTe interface properties.[10,24] Figure 8 shows the PL decay curves obtained from the CdS/CdTe interface of cells with thin films annealed at 550°C for different annealing times.

TRPL signal is determined by multiple factors including bulk carrier lifetime, interface recombination velocity, doping density, electric field, photo-generated carrier density and carrier mobility.[25]

The minority carrier lifetime can be extracted from the experimental data by the following formula

$$\frac{1}{\tau_{\mathrm{TRPL}}} = \frac{1}{\tau_B} + \frac{1}{\tau_{\mathrm{INTERFACE}}}, \qquad (2)$$

where τ_{TRPL} is the experimentally measured lifetime, τ_B is the minority carrier lifetime inside the CdTe film, and $\tau_{\mathrm{INTERFACE}}$ is the interface recombination lifetime. The τ_{TRPL} can be considered equal to $\tau_{\mathrm{INTERFACE}}$ in this work because we chose the specific wavelength to measure the interface area. The actual decay curve is often fitted with a bi-exponential model with lifetime τ_1 and τ_2

$$I_{\mathrm{PL}(t)} = A + B_1 \exp\left(-\frac{t}{\tau_1}\right) + B_2 \exp\left(-\frac{t}{\tau_2}\right), \qquad (3)$$

where t is the time, $I_{\mathrm{PL}(t)}$ is the time-correlated TRPL intensity, A is a constant number, and B_1/B_2 are amplitudes of decay components τ_1/τ_2.

The numerical simulations by Kanevce et al.[25] provide insight for interpreting TRPL measurements on CdTe devices. The faster initial part of the decay is dominated by charge separation effects, which determines the value of τ_1. They have also calculated the $n \times p$ product at different moments during the decay to show that the interface recombination affects the second, slower part of the decay. Based on their results, we use τ_2 to characterize the CdS/CdTe interface property. Measured and fitted τ_2 of CdS/CdTe interfaces annealed for four durations are shown in Table II. From Figs. 5 and 9, we can see that the trend of τ_2 changing against annealing time is like that of V_{OC} against annealing time. The similar correlations of higher V_{OC} that bring higher lifetime have been figured out by other groups.[10,23,26] As the slower part of TRPL decay τ_2 is reported to be dominated by interface recombination,[25] the samples annealed *in situ* for 10 min are thought to have the least defect density and the best interface material quality among the four groups. This result is

Table II. Measured τ_2 of CdS/CdTe interfaces annealed *in situ* for four durations

Annealing time (min)	Lifetime τ_2 (ns)	Chi square criterion χ^2
0	76.73	1.123
10	84.19	1.106
20	83.56	1.121
40	82.25	1.091

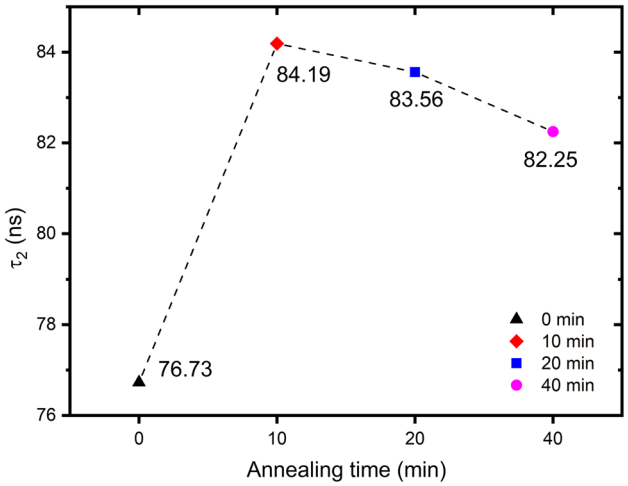

Fig. 9. Measured τ_2 against annealing time curve.

corresponding to the cross-sectional SEM images shown in Fig. 5. It suggests that TRPL measurements can be used for CdS/CdTe interface characterization and help us ascertain favorable interface.

CONCLUSION

In summary, we studied the structural, optical and electrical properties of CdTe solar cells with a structure of FTO/CdS (80 nm)/CdTe (3 μm)/Au to understand the growth mechanism during *in situ* post-growth annealing. Cells with CdTe polycrystalline thin film annealed *in situ* at 550°C/550°C for 10 min show the best performance. Moderate *in situ* annealing treatment increases the grain size and helps the diffusion of S, which account for the improved EQE in 650–800 nm. However, excessive annealing also causes deterioration. Proper *in situ* post-growth annealing (550°C, 10 min) brings better crystallinity of the CdTe thin film and favored CdS/CdTe interface structure and morphology, which help to improve carrier collection and transportation. The PL results also indicate that an appropriate post-growth thermal process is expected to control the elements diffusion. And the most accepted relationship of higher V_{OC} with longer carrier lifetime in CdTe is confirmed here by TRPL, which is helpful to determine interface optoelectronic properties. These results are important towards understanding the impact of *in situ* post-growth annealing and remind us that the thermal process after CdTe deposition should be seriously treated.

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REFERENCES

1. M.A. Green, Y. Hishikawa, W. Warta, E.D. Dunlop, D.H. Levi, J. Hohl-Ebinger, and A.W. Ho-Baillie, *Prog. Photovolt. Res. Appl.* 25, 668 (2017).
2. V.P. Singh, H. Brafman, J. Makwana, and J.C. Mcclure, *Solar Cells* 31, 23 (1991).
3. S.A. Ringel, A.W. Smith, M.H. Macdougal, and A. Rohatgi, *J. Appl. Phys.* 70, 881 (1991).
4. B.E. McCandless, L.V. Moulton, and R.W. Birkmire, *Prog. Photovolt.* 5, 249 (1997).
5. C. Ferekides, J. Britt, Y. Ma, and L. Killian, in *Presented at the Conference Record of the Twenty Third IEEE Photovoltaic Specialists Conference* (1993) **(unpublished)**.
6. C.S. Ferekides, D. Marinskiy, V. Viswanathan, B. Tetali, V. Palekis, P. Selvaraj, and D.L. Morel, *Thin Solid Films* 361, 520 (2000).
7. B. Li, L. Feng, J. Zheng, W. Cai, Y. Cai, J. Zhang, W. Li, L. Wu, and Z. Lei, in *Presented at the 2006 IEEE 4th World Conference on Photovoltaic Energy Conference* (2006) **(unpublished)**.
8. A. Romeo, G. Khrypunov, S. Galassini, H. Zogg, A. Tiwari, N. Romeo, A. Bosio, and S. Mazzamuto, in *Presented at the 22nd European Photovoltaics Solar Energy Conference* (2007) **(unpublished)**.
9. A.A. Al-mebir, P. Harrison, A. Kadhim, G. Zeng, and J. Wu, *Adv. Condens. Matter. Phys.* 2016, 1 (2016).
10. W.K. Metzger, D. Albin, D. Levi, P. Sheldon, X. Li, B.M. Keyes, and R.K. Ahrenkiel, *J. Appl. Phys.* 94, 3549 (2003).
11. V. Buschmann, H. Hempel, A. Knigge, C. Kraft, M. Roczen, M. Weyers, T. Siebert, and F. Koberling, *J. Appl. Spectrosc.* 80, 449 (2013).
12. J. Gao, W. Jie, Y. Yuan, T. Wang, G. Zha, and J. Tong, *J. Vac. Sci. Technol. A* 29, 051507 (2011).
13. C.A. Schneider, W.S. Rasband, and K.W. Eliceiri, *Nat. Methods* 9, 671 (2012).
14. G.C. MLAMorris and S.K. Das, in *Photovoltaic Specialists Conference, Conference Record of the Twenty Third IEEE.* IEEE (2002).
15. A. Morales-Acevedo, *Sol. Energy Mater. Sol. Cells* 90, 678 (2006).
16. J.R. Sites, J.E. Granata, and J.F. Hiltner, *Sol. Energy Mater. Sol. Cells* 55, 43 (1998).
17. N. Romeo, A. Bosio, R. Tedeschi, A. Romeo, and V. Canevari, *Sol. Energy Mater. Sol. Cells* 58, 209 (1999).
18. A. Romeo, D.L. Bätzner, H. Zogg, C. Vignali, and A.N. Tiwari, *Sol. Energy Mater. Sol. Cells* 67, 311 (2001).
19. A. Gupta, V. Parikh, and A.D. Compaan, *Sol. Energy Mater. Sol. Cells* 90, 2263 (2006).
20. T.H. Myers, J.F. Schetzina, S.T. Edwards, and A.F. Schreiner, *J. Appl. Phys.* 54, 4232 (1983).
21. D.P. Halliday, M.D.G. Potter, J.T. Mullins, and A.W. Brinkman, *J. Cryst. Growth* 220, 30 (2000).
22. S.-H. Wei, S.B. Zhang, and A. Zunger, *J. Appl. Phys.* 87, 1304 (2000).

23. D. Kuciauskas, P. Dippo, Z. Zhao, L. Cheng, A. Kanevce, W.K. Metzger, and M. Gloeckler, *IEEE J. Photovolt.* 6, 313 (2016).
24. A. Kanevce, D. Kuciauskas, T.A. Gessert, D.H. Levi, D.S. Albin, and IEEE, in *2012 38th IEEE Photovoltaic Specialists Conference (Pvsc)*, pp. 848–853 (2012).
25. A. Kanevce, D.H. Levi, and D. Kuciauskas, *Prog. Photovolt. Res. Appl.* 22, 1138 (2014).
26. I.L. Repins, B. Egaas, L.M. Mansfield, M.A. Contreras, C.P. Muzzillo, C. Beall, S. Glynn, J. Carapella, and D. Kuciauskas, *Rev. Sci. Instrum.* 86, 013907 (2015).