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# Void Formation and Intermetallic Growth in Pulse Electrodeposited Cu-Sn Layers for MEMS Packaging

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Electrodeposited copper (Cu)-tin (Sn) based solid–liquid interdiffusion (SLID) bonding is becoming popular in wafer-scale packaging of inertial Micro-Electro-Mechanical-Systems (MEMS) sensors due to its inherent advantages of lower cost, low processing temperatures and less stringent surface uniformity requirements. However, eliminating micron-size voids within intermetallic compounds (IMCs) and bond interfaces has remained a challenging task. The present study focuses upon IMC growth and void formation at varying temperatures and times. Stacks of varying thickness of Cu and Sn were fabricated by electrodeposition, and the samples were annealed at temperature ranging up to 300°C. Scalloped shaped $Cu_6Sn_5$ ($\eta$-phase) and comparatively uniform $Cu_3Sn$ ($\varepsilon$-phase) intermetallics were observed. Experimental results show that the growth of metastable $Cu_6Sn_5$ dominates IMC formation at lower temperatures but as temperature increases, $Cu_3Sn$ dominates over the $Cu_6Sn_5$ growth. This IMC growth transition from $Cu_6Sn_5$ dominant growth to $Cu_3Sn$ dominant growth depends on the annealing temperature and has a critical time duration. The IMC thicknesses are compared with those obtained by numerical simulation models. For given annealing temperatures, intermittent voids formed in the IMC layers show increasing size and decreasing void fraction trends with increasing annealing times. The results suggest that Cu-Sn SLID bonding performed at 275°C yields reliable bonding since the void growth is minimal. Based on these results, a test vehicle containing a kelvin structure and daisy chains (having large number of Cu-Sn bonded structure), was fabricated, resulting in electrical resistances lower than 30 m-ohms and 6 ohms, respectively.

**Key words:** Solid–liquid interdiffusion, bonding, voids growth, micro-electro-mechanical-systems, 3-D packaging

## INTRODUCTION

Micro-Electro-Mechanical-Systems (MEMS) devices often consist of moving structural elements which require a controlled environment in their vicinity to inhibit damping effects and increase a product's reliability. This can be achieved by hermetic (airtight) encapsulation of MEMS devices in order to achieve better performance and long-term reliability. As per MEMS sensor's literature, the packaging constitutes a major part of total device cost.[1]

Different techniques have been used in hermetic packaging of MEMS structures like anodic bonding, fusion bonding, eutectic bonding, thermo-compression bonding, etc. Direct metal-to-metal bonding (i.e., Au-Au or Cu-Cu) is the most desirable bonding technique for MEMS packaging applications since they provide rigid mechanical support, highly conductive interconnections and efficient heat dissipation, all in a single fabrication step. Achieving

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process-compatibility and reliable bonds in direct metal-to-metal bonding of MEMS and cap wafers has consistently remained a challenge due to native oxide formation (in Cu), high cost (of Au), high processing temperatures, high bonding pressure and surface uniformity requirements.[2] MEMS devices require packaging at low processing temperatures due to the presence of low melting point metals (e.g., Al) and requires some room for surface non-uniformity too, which are always ascertained due to the deposition process employed in MEMS fabrication processes (e.g., electrodeposition). Thus, there has been continuous requirement for such a process, which can circumvent these stringent requirements and provide cheaper, reliable and hermetic packaging solutions to MEMS devices.

Solid–liquid Interdiffusion (SLID) bonding technique has been investigated to address the above-mentioned requirements. SLID bonding has low processing temperatures since the bonding mechanism involves intermetallic compounds (IMCs) formation of a lower melting point metal (typically Sn). Additionally, the surface uniformity requirements are not so rigid as compared to the thermo-compression bonding, as the lower melting point metal is in liquid phase during the bonding process.[3,4] SLID bonding can also be used to form interconnects, simultaneously while hermetic packaging of MEMS devices, since the IMCs formed are electrically conductive.[5] Moreover, the IMC formed in the bonding process signifies a very strong mechanical and metallurgical bonding. These resultant IMCs have higher melting temperatures ($T_{m,IMC}$) than the processing temperature, which aids multi-levels processing on the same wafer without affecting the previously bonded structures, being an added advantage in three-dimensional (3-D) integration in addition to low processing temperatures. SLID bonding has been shown to offer highly reliable, hermetic and mechanically strong bonds even after several reliability tests.[6–8] Xu et al. have shown Cu-Sn bonds to be better than Au-Sn bonds in terms of strength and reliability.[8]

In Cu-Sn interdiffusion system (Fig. 1), initially, Cu diffuses into Sn to form a Sn rich $Cu_6Sn_5$ ($\eta$-phase) at Cu-Sn interface (Fig. 1a), followed by further Cu diffusion into the $\eta$-phase to finally form more stable and preferred Cu rich $Cu_3Sn$ ($\varepsilon$-phase) at the Cu-$Cu_6Sn_5$ interface (Fig. 1b) since $Cu_3Sn$ has superior properties over $Cu_6Sn_5$ for electronics packaging applications.[9] Now there is a growth competition at $Cu_3Sn$-$Cu_6Sn_5$ interface between $Cu_3Sn$ or $Cu_6Sn_5$ growth depending upon interdiffusion coefficients of Cu and Sn in $Cu_3Sn$ and $Cu_6Sn_5$ phases, respectively. Diffusion of Cu in $Cu_3Sn$ is reported to be three times higher than that of Sn in $Cu_6Sn_5$,[10] resulting in increased growth of stable $Cu_3Sn$ (Fig. 1c) and finally consuming the metastable $Cu_6Sn_5$ completely (Fig. 1d). IMC growth in SLID bonding depends upon metal thicknesses, grain size of electrodeposited metals and the temperature profile applied while bonding. Electrodeposited metals having fine grains microstructures result in rapid growth of IMCs due to the increased grain boundaries regions, because it provides more nucleation sites and increased grain boundary diffusion.[11] In Cu-Sn SLID bonding, IMCs are formed through an interdiffusion process

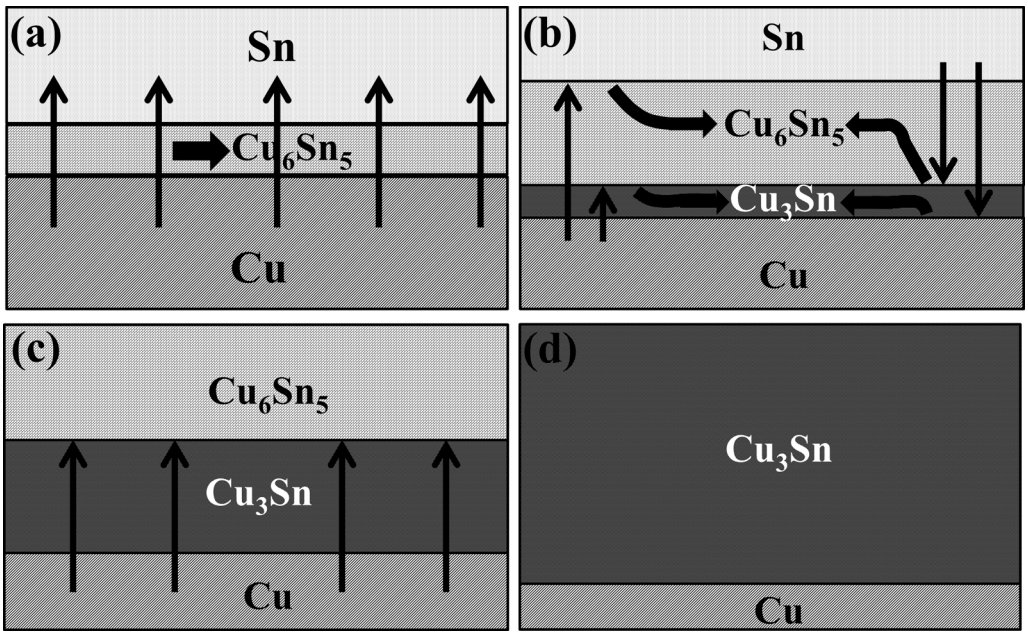



Fig. 1. Schematic of diffusion reactions in Cu-Sn intermetallic growth in discrete steps. (a) Cu diffuses in Sn to form $Cu_6Sn_5$, (b) $Cu_6Sn_5$ further grows and simultaneously Cu diffuses in $Cu_6Sn_5$ to form stable $Cu_3Sn$, (c) Sn gets consumed to $Cu_6Sn_5$ and $Cu_3Sn$, and (d) Cu diffuses in metastable $Cu_6Sn_5$ to form single stable $Cu_3Sn$ over Cu.

involving both solid–solid diffusion and solid–liquid diffusion. These diffusion reactions depend upon rate of diffusing metal through different underlying phases and are represented by interdiffusion coefficients.

Due to easier availability and lower cost, Cu-Sn SLID bonding has attracted a lot of interest. Literature has shown very high potentials for Cu-Sn based SLID bonding.[5,12,13] Wide range of mechanical strengths has been reported for Cu-Sn bonds (i.e., from 10 MPa to 60 MPa[6,7,11,14]) which warrants further research to attain a better understanding of the process. Nevertheless, a major concern is that IMC growth and void formation studies in literature show high deviations, and still lack common agreement. Thus, low cost SLID bonding process involving electrodeposited Cu and Sn is investigated for hermetic packaging of MEMS devices. In this study, IMC growth and void formation in Cu-Sn metal stacks annealed at different temperatures and times durations are presented in terms of IMC thickness, void sizes and void fractions. IMC thicknesses were predicted using a MATLAB numerical simulation model for respective annealing temperature and time durations, using the diffusion parameters from the literature.[13] The experimentally observed IMC thicknesses were compared with the thicknesses predicted by numerical simulation. The deviations in experimental and predicted IMC thicknesses were analyzed and possible reasons for the same are discussed in detail. Test vehicles containing several daisy chain structures were fabricated using SLID bonding and their electrical characterization were carried out.

## NUMERICAL SIMULATION OF IMC FORMATION

Initially, IMC thicknesses were predicted by a MATLAB numerical simulation model using interdiffusion empirical relations. A simulation model is used to predict pure Sn layer thickness available at the melting temperature and time required to attain final bond by complete conversion of both Sn and metastable $Cu_6Sn_5$ to stable $Cu_3Sn$ IMC. Metal diffusion rates and reaction kinetics decide IMC growth in any metal system. Since, the movement of metal atoms in SLID bonding is only in the direction perpendicular to the electrodeposited metal plane, it can be fairly assumed as a one-dimensional (1-D) diffusion process. As per the reaction kinetics model for 1-D diffusion, IMC thickness or consumed Sn thickness for given temperature and time is given by[13]:

$$y_t^2 - y_o^2 = k_o \exp\left(-\frac{E_a}{RT}\right) t^{2n}, \tag{1}$$

where, $y_t$ represents IMC thickness or Sn thickness consumed to form IMCs at time $t$, $y_o$ is initial IMC thickness, i.e., zero, $k_o$ is the diffusion coefficient, $E_a$ is the activation energy, $R$ is a gas constant, $T$ is absolute temperature, $t$ is annealing time and $n$ is an empirical time constant. If $n = 0.5$, then Eq. 1 corresponds to an analytical solution of conventional 1-D diffusion problem. Nevertheless, if the empirical time constant ($n$) deviates from 0.5, it implies that apart from diffusion, other phenomena such as void formation and reaction kinetics at IMC interfaces also influence the IMC growth.

Initial Sn thickness is very critical in Cu-Sn SLID bonding,[15] since higher Sn thickness results in Sn flow out while annealing which causes short circuiting of the electrical device encapsulated within the package and low Sn thickness results in void formation at the bonding interface. Consequently, an optimum thickness of Sn is required for successful performance of Cu-Sn SLID bonding. Sn is converted to $Cu_6Sn_5$ and $Cu_3Sn$ IMCs by gradual interdiffusion and reaction of Cu and Sn among themselves. Therefore, at any point of time, the amount of Sn consumed will always be equal to the amount of Sn present in total IMCs formed. Thus, by comparing the volume of Sn that has reacted or consumed to form IMC, and the amount of Sn present in $Cu_6Sn_5$ and $Cu_3Sn$ IMCs, a relationship among the thickness of $Cu_6Sn_5$, $Cu_3Sn$ and consumed Sn can be obtained, as cross-sectional area remains the same before and after the annealing. Thus, consumed Sn thickness can be correlated to IMC thicknesses by mass conservation as[13]:

$$Y_{Sn,con} = \frac{m_{Sn,Cu_3Sn}}{\left[\rho_{Sn}/\rho_{Cu_3Sn}\right]} Y_{Cu_3Sn} + \frac{m_{Sn,Cu_6Sn_5}}{\left[\rho_{Sn}/\rho_{Cu_6Sn_5}\right]} Y_{Cu_6Sn_5}, \tag{2}$$

where $Y_{Sn,con}$ is consumed Sn thickness, $m_{Sn}$ is the mass of Sn in respective IMCs, $Y$ is the thickness of respective IMCs and $\rho_{Sn}$ is the density of Sn. Thus if the thickness of IMCs are known, required Sn thickness can be calculated or if the consumed Sn thickness and $Cu_3Sn$ thickness is known (i.e., from Eq. 1), then the thickness of $Cu_6Sn_5$ can be estimated. With these relationships, a MATLAB simulation model was used to predict the IMC thicknesses using the diffusion coefficient and activation energy values from the literature.[13] As an illustration, the output of the simulation model with the given input temperature profile and 1.5 $\mu$m initial Sn thickness is shown in Fig. 2. Since the activation energy for $Cu_6Sn_5$ is lower than that of $Cu_3Sn$, $Cu_6Sn_5$ grows rapidly and $Cu_3Sn$ growth is marginal[3,16] at lower temperatures. Total annealing time depends on initial pure Sn thickness[8] and annealing temperature. Higher initial Sn thickness and low annealing temperature require longer processing time for the complete conversion of Sn into stable $Cu_3Sn$, since diffusion is a temperature dependent phenomenon. Additionally, the IMC layers formed between Cu-Sn layers act as diffusion

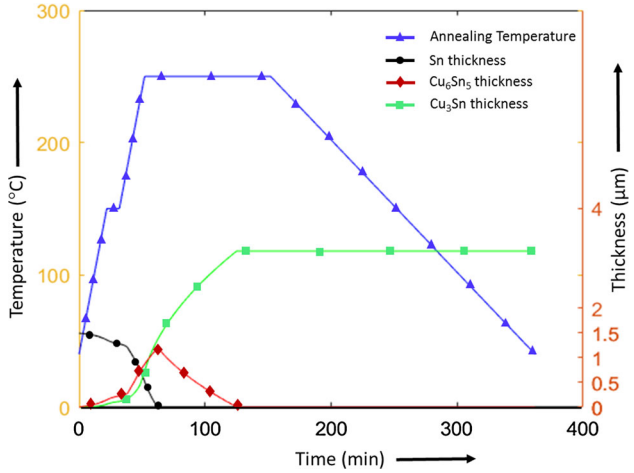



Fig. 2. Illustrative simulation output showing input temperature and variation of pure Sn, $Cu_6Sn_5$ and $Cu_3Sn$ IMC thicknesses with respect to time.

barrier layers for further diffusing Cu and Sn atoms.

## EXPERIMENTAL PROCEDURE

### Sample Preparation

At first, 2″ *p-type* (100) Si wafers were cleaned using standard cleaning (SC), which was developed at Radio Corporation of America (RCA), thus it is commonly referred as RCA cleaning. This cleaning process involves three sequential steps: SC-1, HF dip and SC-2. In SC-1 process, standard Si wafer is dipped in SC-1 solution (i.e., $NH_4OH$:$H_2O_2$:DI water in 1:1:5 proportion) at 80°C for 10 min to remove any organic contaminations. Native oxide is then removed by dipping the wafer in 2% hydrogen fluoride (HF) for 30 s. The wafer is then dipped in SC-2 solution (i.e., HCl:$H_2O_2$:DI water in 1:1:6 proportion) at 80°C for 10 min to remove any metallic contamination. After the RCA cleaning, wafer is rinsed in DI water followed by spin drying.[17] Then 200 nm thick silicon oxide ($SiO_2$) was grown to electrically isolate the substrate. Then, chromium (10 nm) and gold (100 nm) were sputter deposited for an adhesion/diffusion barrier layer and a seed layer, respectively. Circular and square shaped bond pads were patterned using AZ4620 photoresist in MJB4 mask aligner. The in-plane dimensions of the bond pads were 100 $\mu$m. Since, the formation of stable $Cu_3Sn$ IMC is the final goal of the bonding, thickness of Cu should always be greater than that required by the given initial Sn thickness to form $Cu_3Sn$ IMC as the only IMC between Cu layers. This minimum threshold Cu thickness, corresponding to given initial Sn thickness for complete conversion of Sn into $Cu_3Sn$, can be estimated by volume of Cu and Sn present in $Cu_3Sn$[15]:

$$\frac{y_{Cu}}{y_{Sn}} = \frac{m_{Cu,Cu_3Sn}}{m_{Sn,Cu_3Sn}} \times \frac{\rho_{Sn}}{\rho_{Cu}} = 1.31, \quad (3)$$

where, $m$ is the mass and $\rho$ is the density of respective metals and IMCs. Thus, Cu thickness should be at least 1.3 times the Sn thickness in order to achieve single stable $Cu_3Sn$ IMC layer. Therefore, 6 $\mu$m thick Cu and 3 $\mu$m thick Sn were sequentially electrodeposited by pulse electrodeposition to ensure smooth fine-grains of electrodeposited Cu and Sn. The average current density applied in Cu and Sn electroplating was 5 mA/cm$^2$. Electroplating was performed using a commercial electrolyte (supplied by Atotech, Germany), with continuous filtration and agitation of electrolyte to achieve uniform and good quality electrodeposits ($R_a \sim 90$ nm).

After electrodeposition, Si wafers were diced into individual dies for annealing. These samples were annealed at 250°C, 275°C and 300°C for 10 min, 60 min and 150 min into a vacuum furnace to avoid oxidation of Cu at elevated temperatures. Samples were not annealed at 300°C for 150 min, since pure Sn was expected (from numerical simulations) to completely transform into $Cu_3Sn$ at 60 min of annealing. Annealing temperature was attained in two steps, i.e., firstly the samples were ramped to intermediate temperature ($T_{int}$ = 150°C) with a ramping rate of 5°C/min and was held there for 10 min. Then, the temperature was ramped to various predetermined annealing temperaturse with the same ramp rate and was held there for different time durations (Fig. 2).

Dies were then molded into epoxy mold and polished using standard metallographic methods to observe cross-sectional microstructures under a scanning electron microscope (SEM) (FEI Quanta 200) and study IMCs and void growth. All micrographs were taken at the same magnification, i.e., 10,000× for easy comparison, which has a resolution of 0.013 $\mu$m pixel$^{-1}$. Electron dispersive spectroscopy (EDS) was performed to identify the IMC's composition. The SEM micrographs were analysed in image processing software "ImageJ" to determine the thicknesses of different IMCs and void areas at different locations. For each sample, IMC thicknesses were measured at ten different locations of arbitrary bond pads in order to take averaged data. For void growth study, averaged void size and void fraction, i.e., number of voids per unit length of SEM micrograph, were measured from arbitrary bond pads of each sample. Void growth is completely arbitrary in nature, thus, it is fairly assumed that averaged data represents the entire bond pad's behavior.

### Design and Fabrication of Test Vehicle

Test vehicle having individual kelvin and daisy chain structures were designed to characterize the

electrical performance of the Cu-Sn SLID bonding assisted interconnects. Kelvin structures were used to estimate the electrical resistances of single interconnect and daisy chain with increasing number of interconnects that were designed to estimate the electrical resistance of daisy chain structures having different numbers of interconnects.

Test vehicle consisted of two separate dies (Fig. 3), i.e., substrate die having Cu redistribution lines (RDL) and top die having the conjugate RDL with Cu-Sn pillars over them, so that when substrate and top dies were bonded continuous electrical connections were obtained (Fig. 3f). The fabrication steps for test vehicles were the same as those discussed for Cu-Sn bond pad structures in a previous section. Substrate dies had a single layer of 5 $\mu$m thick Cu RDLs fabricated by a single lithography step using substrate mask (#1) having contact pads for electrical characterization too (Fig. 3a and d). In top dies, two levels of lithography were performed; first to electrodeposit a 4 $\mu$m thick Cu for conjugate RDL and second to electrodeposit Cu (6 $\mu$m) and Sn (3 $\mu$m) pillars on previously deposited 4 $\mu$m thick Cu RDL (Fig. 3b and e). Top conjugate RDL mask (#2) and pillar mask (#3) were provided with wafer level alignment marks, since pillar mask (#3) had to undergo lithography above the layer patterned by a top conjugate RDL mask (#2) on the same Si wafer. Die level alignment marks were designed to align top and substrate dies while bonding in a flip chip bonder (Fig. 3c). Test vehicles were designed having two different diameters of Cu interconnect pillars, i.e., 100 $\mu$m and 80 $\mu$m. The minimum number of interconnects in test vehicles having 100 $\mu$m and 80 $\mu$m diameters, were 2 and maximums were 138 and 240, respectively.

## RESULTS

### Numerical Simulation Results

A numerical simulation model was used to analyze the effect of various input process parameters, such as initial Sn thickness, ramping rate, annealing temperature and duration on the SLID bonding characteristics. From the simulation model, pure Sn availability at its melting temperature (232°C), IMC thicknesses, time required for complete conversion of Sn into IMCs, i.e., $Cu_6Sn_5$ and $Cu_3Sn$ and total processing time required to completely form a single stable $Cu_3Sn$ IMC were predicted. General trends of IMC thicknesses and processing time corresponding to varying input parameters and reported diffusion parameters were obtained from a numerical simulations model (Fig. 4). The IMC thicknesses predicted by the numerical simulation model and its comparison with experimentally measured thicknesses are presented in the next section. It was expected that samples annealed at 250°C for 10 min will have pure Sn at their top surface since the annealing time wouldn't be sufficient to completely transform Sn into $Cu_6Sn_5$ and $Cu_3Sn$ IMCs. For samples annealed at 300°C for 60 min, numerical simulation predicted to have stable $Cu_3Sn$ at its top surface. Samples annealed at remaining combinations of temperatures and time durations were expected to have $Cu_6Sn_5$ on their top surfaces.

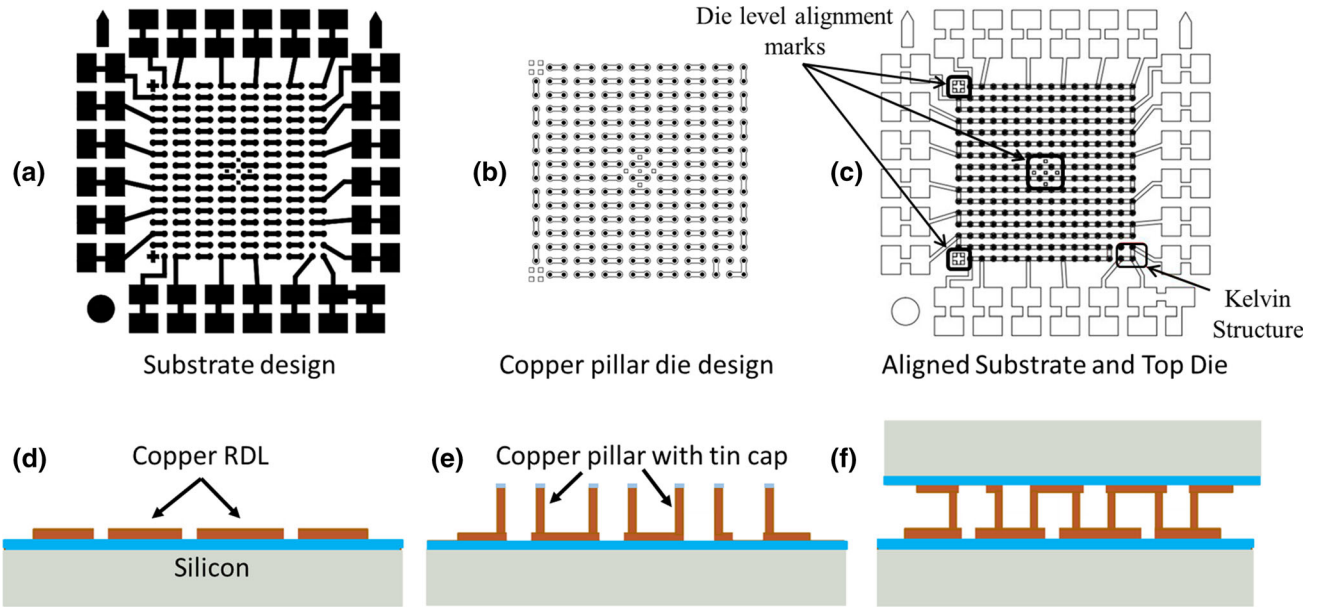



Fig. 3. Test vehicle design and fabrication schematic. (a) Substrate die having Cu RDL, (b) die mask layout having bottom RDL and Cu pillar with Sn cap, (c) layout of bonded dies (d) schematic of bottom substrate die (e) schematic showing 4 $\mu$m thick bottom Cu RDL and Cu (6 $\mu$m)/Sn (3 $\mu$m) pillars (f) bonded die schematic.

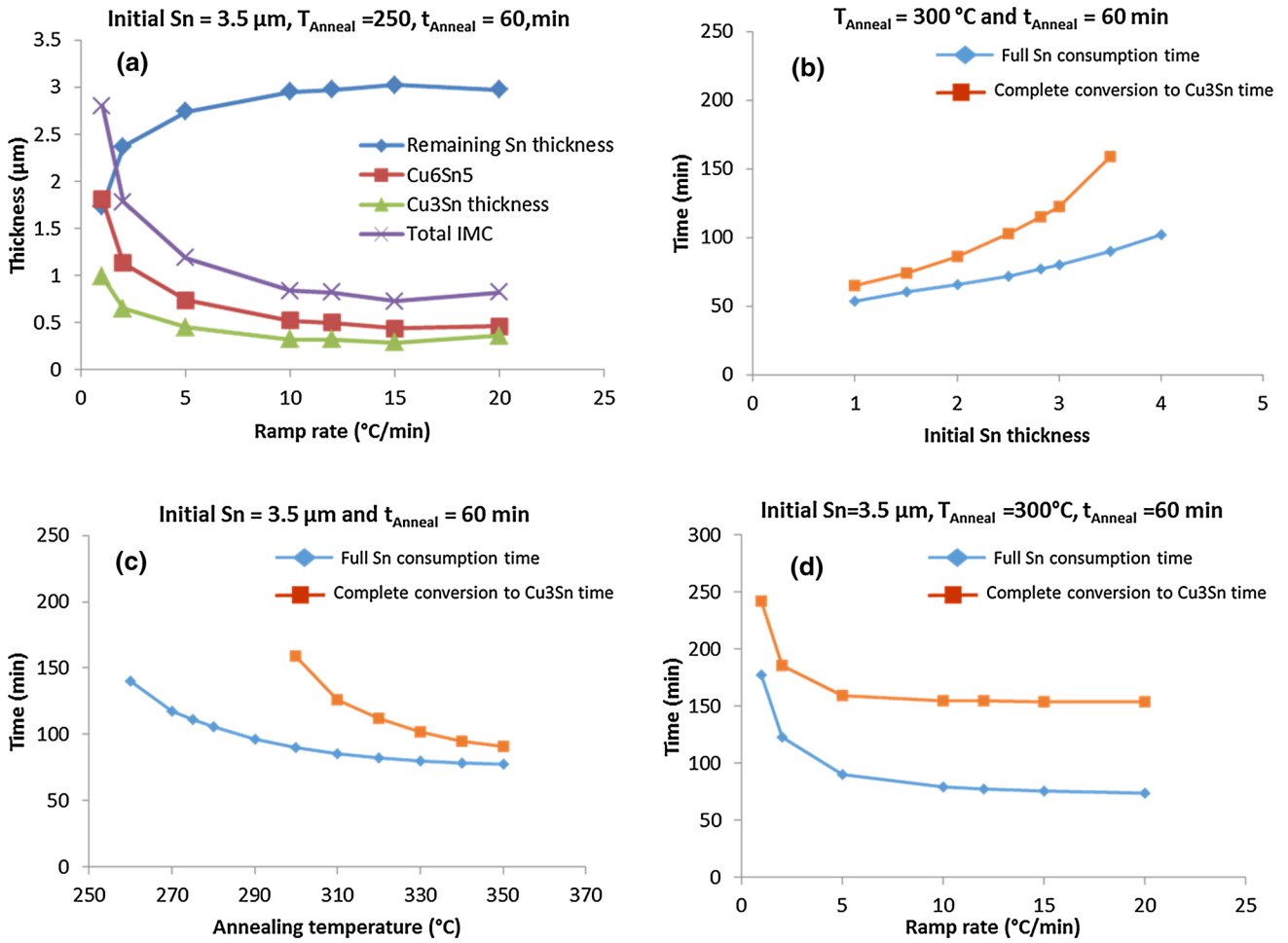



Fig. 4. Parametric effect on SLID bonding characteristics. (a) Effect of ramp rate on IMC and Sn thickness availability at $T_m$ = 232°C, (b) effect of initial Sn thickness, (c) effect of annealing temperature, and (d) effect of ramp rate on processing time.

## Experimental Results: IMC Growth and Void Formation

### *Intermetallic Growth*

Top surfaces of the annealed samples were observed in SEM and EDS was performed to evaluate the top surface's composition, i.e., if it has pure Sn, $Cu_6Sn_5$ or $Cu_3Sn$ in accordance with the numerical simulation results. It was observed that all the samples annealed at 250°C had pure Sn and those annealed at 275°C and 300°C had $Cu_6Sn_5$ on their top surfaces. Numerical simulation expectations were verified experimentally except few exceptions. The experimentally observed top surface compositions for 250°C for 60 min and 150 min were not same as that predicted by the simulations; rather these samples had pure Sn at their top surfaces instead of expected $Cu_6Sn_5$ IMC. The samples annealed at 300°C for 60 min also showed $Cu_6Sn_5$ rather than the expected stable $Cu_3Sn$ IMC. EDS analysis of the bond pad's top surface for each experiment (taken arbitrarily) with corresponding Cu and Sn atomic percentages are shown in Fig. 5. IMC thicknesses were then measured by cross-sectional analysis and IMC compositions were confirmed via EDS analysis. The experimentally observed atomic fractions of Cu and Sn in $Cu_6Sn_5$ and $Cu_3Sn$ in annealed samples were in close agreement with the theoretical values (Table I).

Bond pad's cross-sectional SEM micrograph showing IMC thicknesses are shown in Fig. 6. Non-uniform scalloped shaped $Cu_6Sn_5$ IMC and comparatively uniform $Cu_3Sn$ IMC can be clearly seen in the SEM micrograph. These scallop shaped growths can be attributed to difficulty in IMC nucleation at the Cu-Sn interface, since Cu, Sn, $Cu_6Sn_5$ and $Cu_3Sn$ have different crystal lattices. Another reason can be the anisotropic growth of metastable $Cu_6Sn_5$ in the Cu-Sn couple due to its hexagonal lattice structure. It was observed that for a given annealing temperature, total IMC thickness increases with the increasing annealing time durations, e.g., for 250°C (Fig. 6a, c, and e). IMC growth behavior in the samples annealed at 275°C (Fig. 6b, d, and f) and 300°C (Fig. 6g and h) showed $Cu_3Sn$ formation by consuming $Cu_6Sn_5$. It is observed that

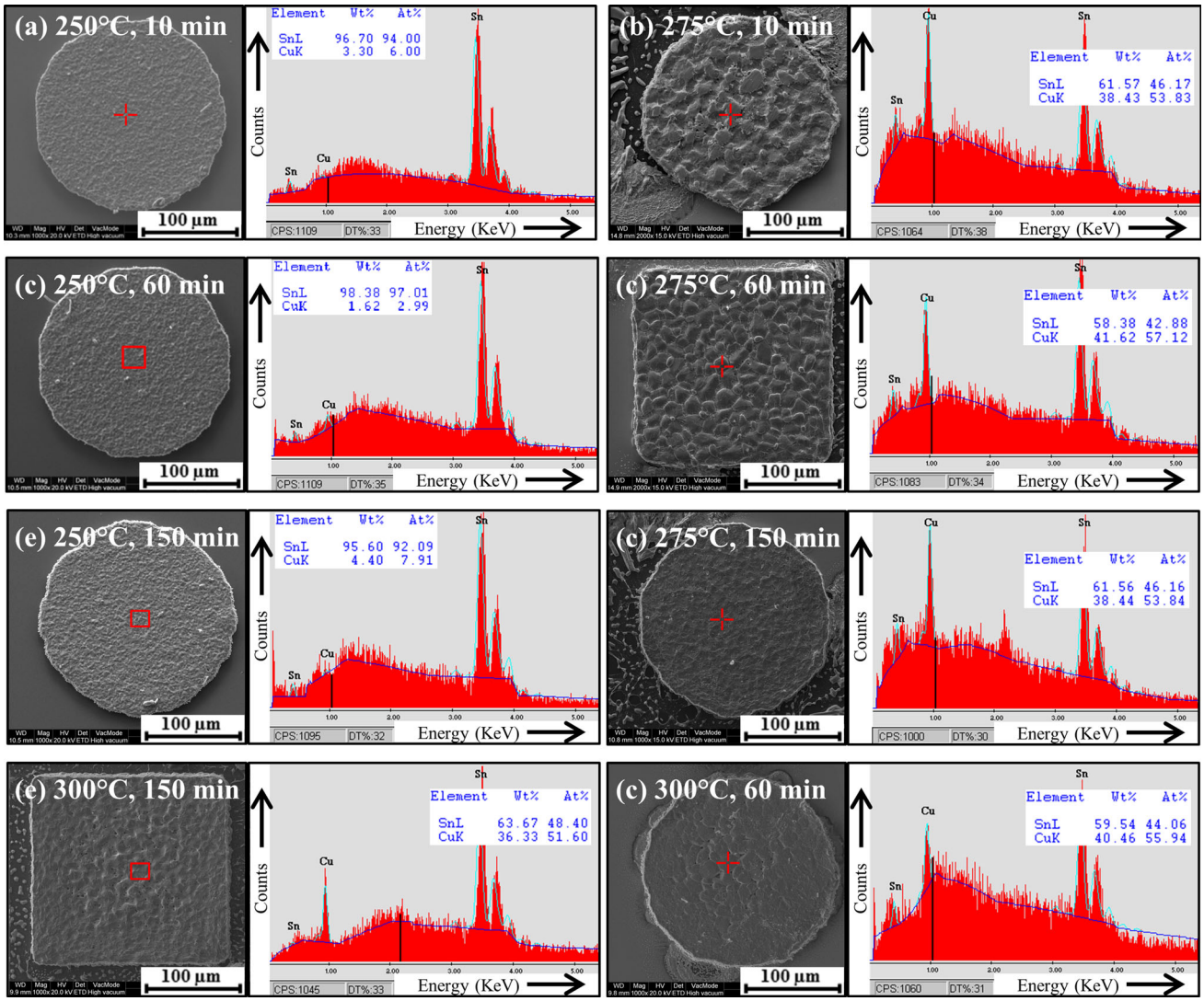



Fig. 5. Top surface EDS analysis for samples annealed at (a) 250°C for 10 min, (b) 275°C for 10 min, (c) 250°C for 60 min, (d) 275°C for 60 min, (e) 250°C for 150 min, (f) 275°C for 150 min, (g) 300°C for 10 min, and (h) 300°C for 60 min.

**Table I. Theoretical and experimentally observed Cu-Sn compositions in $Cu_6Sn_5$ and $Cu_3Sn$**

| | Theoretical atomic percentages (%) | | Experimentally observed atomic percentages (%) | |
|---|---|---|---|---|
| | $Cu_6Sn_5$ | $Cu_3Sn$ | $Cu_6Sn_5$ | $Cu_3Sn$ |
| Cu | 54.55 | 75.0 | 54–57 | 72.5–76.9 |
| Sn | 45.45 | 25.0 | 43–46 | 23.1–27.5 |

initially $Cu_6Sn_5$ grows, and then it gets consumed by reacting with Cu to yield thermodynamically more stable $Cu_3Sn$ IMC. This was not observed in samples annealed at 250°C, since the annealing time duration would have been very low for this transition to occur. Using image processing software "ImageJ", corresponding $Cu_6Sn_5$ and $Cu_3Sn$ IMC thicknesses were calculated from SEM micrographs (i.e., Fig. 6). Comparison of IMC thicknesses as predicted by the numerical simulation model and

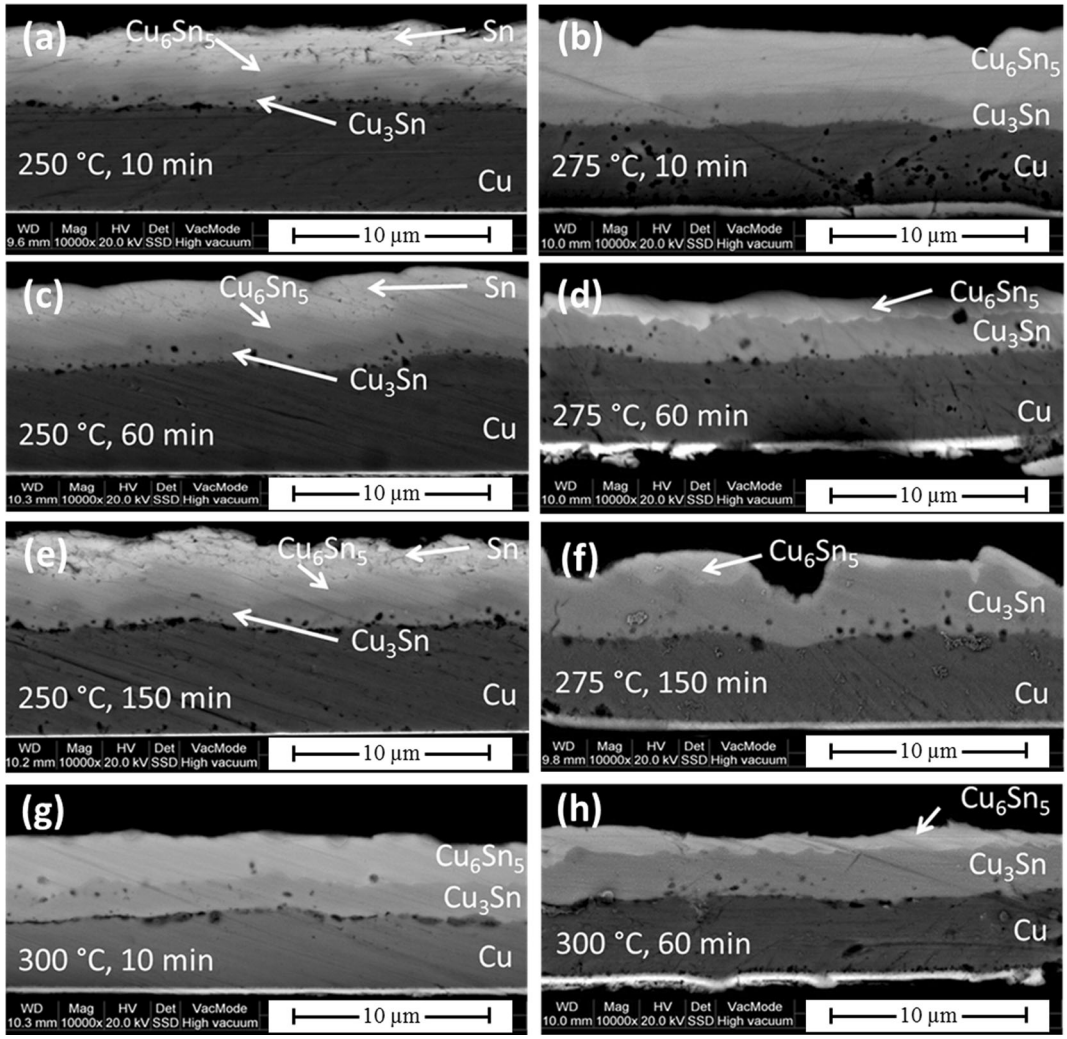



Fig. 6. Cross-sectional SEM micrograph with EDS data of samples annealed at (a) 250°C for 10 min, (b) 275°C for 10 min, (c) 250°C for 60 min, (d) 275°C for 60 min, (e) 250°C for 150 min, (f) 275°C for 150 min, (g) 300°C for 10 min, and (h) 300°C for 60 min.

**Table II. Comparison of predicted and experimentally measured IMC and remaining Sn thicknesses**

| | | Numerical simulation predicted thickness (µm) | | | Experimentally measured thickness (µm) | | |
|---|---|---|---|---|---|---|---|
| **Temperature (°C)** | **Time (s)** | **$Cu_6Sn_5$** | **$Cu_3Sn$** | **Remaining Sn** | **$Cu_6Sn_5$** | **$Cu_3Sn$** | **Remaining Sn** |
| 250°C | 600 | 2.06 | 1.99 | 0.40 | 1.34 | 1.81 | 1.79 |
| | 3600 | 1.81 | 3.21 | 0 | 1.58 | 1.51 | 1.65 |
| | 9000 | 0.83 | 4.67 | 0 | 1.78 | 1.85 | 1.55 |
| 275°C | 600 | 2.40 | 3.39 | 0 | 2.99 | 1.54 | 0 |
| | 3600 | 1.46 | 5.10 | 0 | 0.87 | 1.90 | 0 |
| | 9000 | 0 | 5.92 | 0 | 0.24 | 2.69 | 0 |
| 300°C | 600 | 1.35 | 5.27 | 0 | 1.90 | 1.67 | 0 |
| | 3600 | 0 | 7.29 | 0 | 1.55 | 2.64 | 0 |

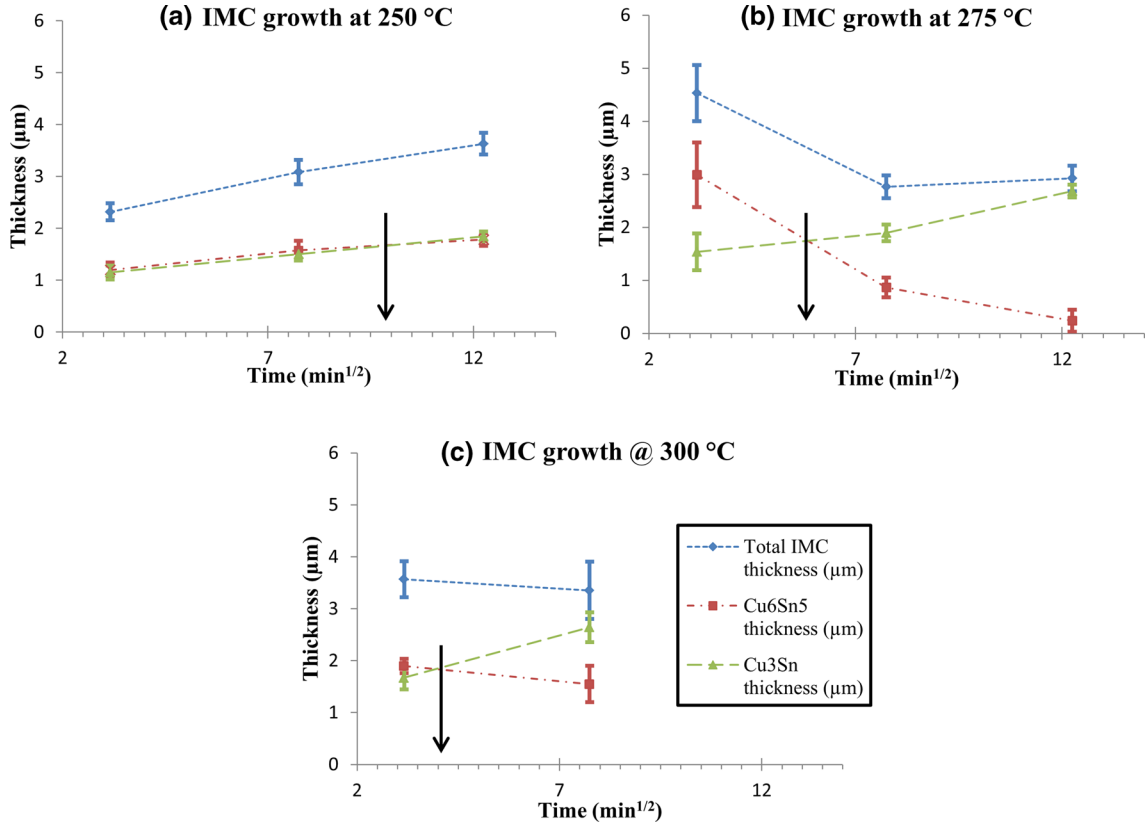
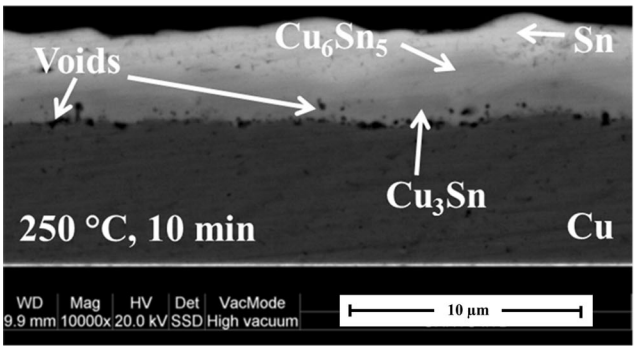



Fig. 7. Variation of IMC thickness as a function of square root of annealing time showing IMC growth with critical time duration at (a) 250°C, (b) 275°C and (c) 300°C.




| | |
|---|---|
| Avg. void size in $Cu_3Sn$ | : 0.02 µm$^2$ |
| Void fraction in $Cu_3Sn$ | : 1.17 µm$^{-1}$ |
| Avg. void size at Cu-$Cu_3Sn$ interface | : 0.074 µm$^2$ |
| Void fraction at Cu-$Cu_3Sn$ interface | : 1.10 µm$^{-1}$ |

Fig. 8. Voids in Cu-Sn metal stack bond pad with characteristic voiding parameters.

experimentally measured mean IMC and remaining Sn are listed in Table II. These IMC thicknesses are plotted as a function of square root of time to verify parabolic behavior of Cu-Sn IMC growth as shown in Fig. 7.

### *Void Growth in IMC*

Results are compiled to illustrate the void propensity with respect to annealing temperature and time durations. As an illustration of voids, a SEM micrograph of a bond pad annealed at 250°C for 10 min is shown in Fig. 8. The evaluated characterizing voiding parameters, i.e., average void size and average void fractions for the given micrograph are also presented in Fig. 8. As a whole observation, a significant level of microvoids was observed at the Cu-$Cu_3Sn$ interface and within the $Cu_3Sn$ IMC layer. A few or negligible voids were observed at the $Cu_3Sn$-$Cu_6Sn_5$ interface and within $Cu_6Sn_5$ IMC. Few to no voids were observed at the $Cu_6Sn_5$-Sn interface. Observed data is presented in terms of two characteristic parameters, i.e., variation of average void size and average void fractions.

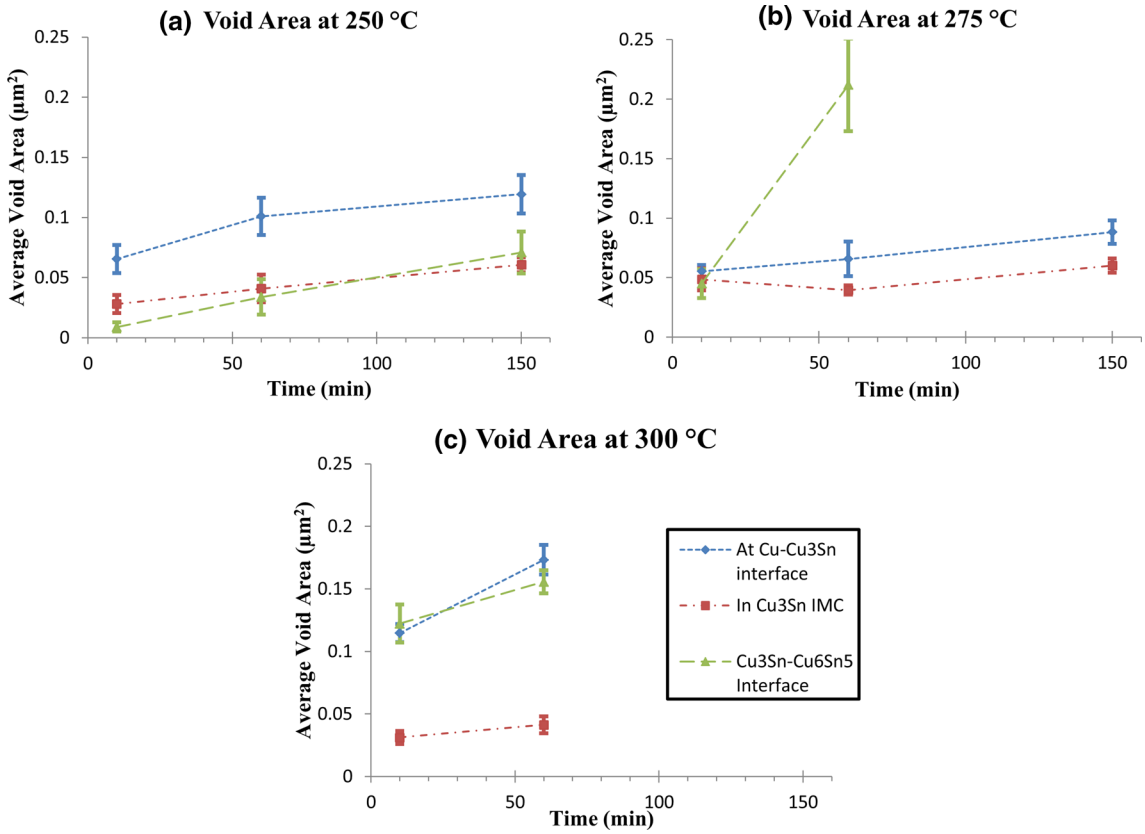



Fig. 9. Variation of average void area as a function of annealing temperature and time durations at (a) 250°C, (b) 275°C and (c) 300°C.

(a) Average void size

Figure 9 presents the variation of average void size as a function of annealing temperature and time durations. The average void size or area of all voids, i.e., voids at Cu-$Cu_3Sn$ interface, within $Cu_3Sn$ and $Cu_3Sn$-$Cu_6Sn_5$ interface, was observed to increase with increasing annealing time durations at given annealing temperature. For Cu-$Cu_3Sn$ interface voids, samples annealed at 300°C showed the highest average void sizes. The largest individual void at the Cu-$Cu_3Sn$ interface was encountered for the sample annealed at 300°C for 60 min, which was 1.44 $\mu m^2$. For voids within $Cu_3Sn$ IMC, samples annealed at 250°C showed the highest average void size having a largest individual void size of 0.283 $\mu m^2$ for 150 min of annealing. Samples annealed at 275°C showed minimum average void sizes for both Cu-$Cu_3Sn$ interface voids and $Cu_3Sn$ voids with the smallest individual void size being 0.002 $\mu m^2$. Void sizes of $Cu_3Sn$-$Cu_6Sn_5$ interface void were minimal for samples annealed at 250°C. No voids were seen at $Cu_3Sn$-$Cu_6Sn_5$ interface for samples annealed at 275°C for 150 min (Fig. 6f).

(b) Average void fraction

Variation of void fraction with respect to annealing temperature and time durations is presented in Fig. 10. It is observed that for a given annealing temperature, void fraction decreases with increasing annealing time durations. Samples annealed at 275°C for 10 min (Fig. 10b) showed out of trend variation, i.e., lower void fraction than the samples annealed at the same temperature for higher time durations. The reason for this behavior is not completely clear and requires further investigation. The highest and lowest void fraction for voids at the Cu-$Cu_3Sn$ interface and within $Cu_3Sn$ were observed in samples annealed at 250°C for 10 min and 300°C for 60 min, respectively. The highest and lowest void fraction were observed to be 1.39 $\mu m^{-1}$ and 0.40 $\mu m^{-1}$, respectively. Void fractions of $Cu_3Sn$-$Cu_6Sn_5$ interface voids were observed to be negligible as seen in Fig. 6.

## CHARACTERIZATION OF Cu-Sn STACK TEST VEHICLES

Images of wafers having top RDL dies with pillars and substrate dies along with their singulated individual dies are presented in Fig. 11. The shiny milky white color of RDL shows the presence of electrodeposited Sn on the Cu pillars (Fig. 11a and c). The individual dies (Fig. 11c and d), were bonded using Flip chip bonder and then the fabricated test vehicles (Fig. 11e) were electrically characterized by

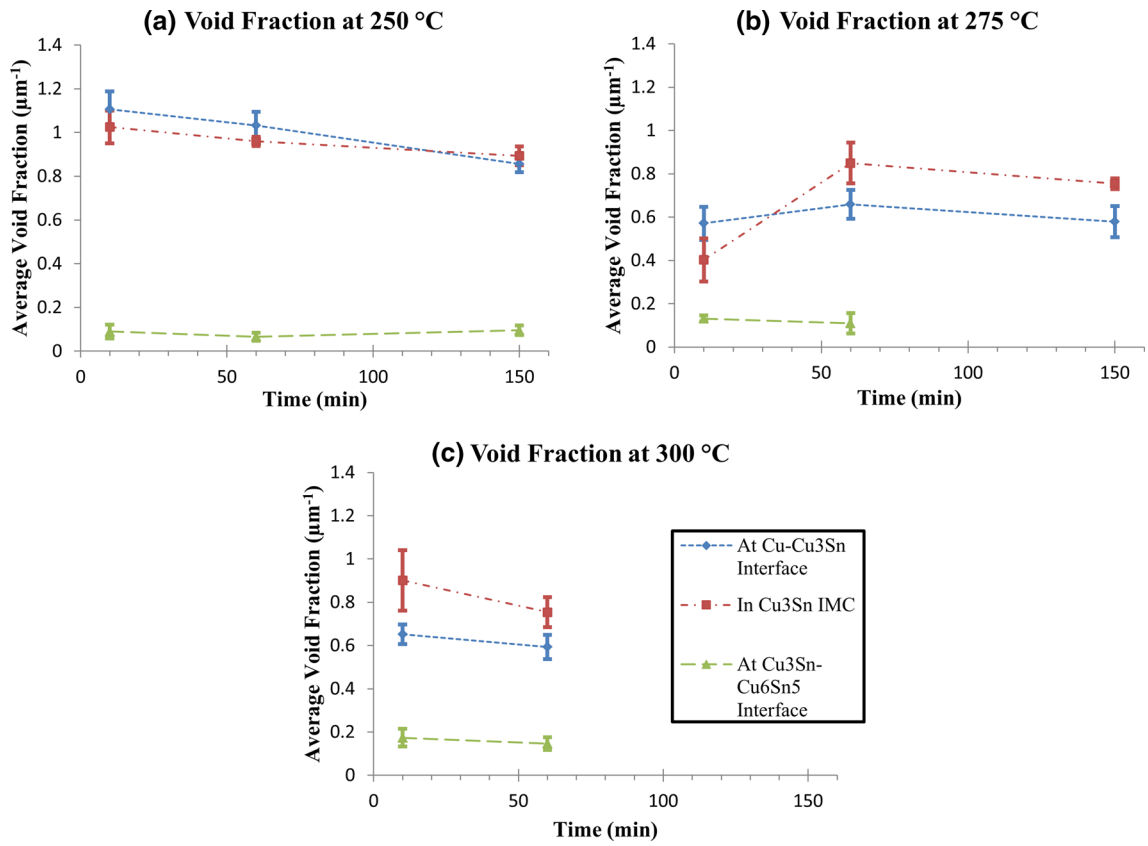



Fig. 10. Variation of average void fraction as a function of annealing temperature and time durations at (a) 250°C, (b) 275°C and (c) 300°C.

measuring the resistance of kelvin and daisy chain structures in bonded samples in order to show continuous connections in daisy chains. The measured electrical resistance of daisy chain includes all resistances, i.e., bottom RDL, contact resistance, copper pillar, interface, IMC and the top RDL.

The electrical resistance of daisy chain structures showed a linearly increasing trend (Fig. 12). The maximum resistance for a single kelvin structure and the longest daisy chain in the samples having 100 $\mu$m diameter Cu pillars (i.e., 138 pillars) were observed to be 30 mΩ and 2.9 Ω, respectively, whereas for samples having 80 $\mu$m diameter Cu pillars (i.e., 240 pillars) those were 47 mΩ and 5.84 Ω, respectively. Few bonded samples showed very high daisy chain resistances, i.e. $>$ 1 kΩ due to the daisy chain discontinuity, which can be due to the fabrications issues. Samples bonded at 250°C showed higher resistance than those bonded at 300°C (Fig. 12, plot 1 and plot 2), since samples annealed at 250°C had higher void fraction than that in 300°C as observed in void growth results (Fig. 10). Bonding pressure is observed to influence the electrical resistance of the daisy chain which requires further experiments for better understanding.

## DISCUSSION

### Intermetallic Growth

Intermetallic growth between Cu and Sn showed non-uniform scallop shaped $Cu_6Sn_5$ and uniform $Cu_3Sn$ IMC growth (Fig. 6). Intermetallic growth in this study reveals that at the beginning of annealing, $Cu_6Sn_5$ dominates the IMC growth, which is followed by $Cu_3Sn$ IMC growth by consuming the already formed $Cu_6Sn_5$ IMC. The regime or time duration of $Cu_6Sn_5$ dominant growth is decided by the annealing temperature. The transition from $Cu_6Sn_5$ dominant growth to $Cu_3Sn$ dominant growth is referred as *critical time duration* (Fig. 7). It was observed that at 250°C, there is continuous rise in both $Cu_6Sn_5$ and $Cu_3Sn$ IMC thicknesses, attributed to mainly two reasons. First the thickness of $Cu_3Sn$ was very low in the beginning, and; hence, Cu could easily diffuse through $Cu_3Sn$ IMC to react with Sn and yield $Cu_6Sn_5$. Second, an ample amount of Sn was available in these samples to react with the diffusing Cu to form $Cu_6Sn_5$ even though $Cu_6Sn_5$ was getting transformed into $Cu_3Sn$ at the $Cu_6Sn_5$-$Cu_3Sn$ interface. Thus, $Cu_6Sn_5$ thickness did not reduce drastically and remain comparable to that of $Cu_3Sn$, being an

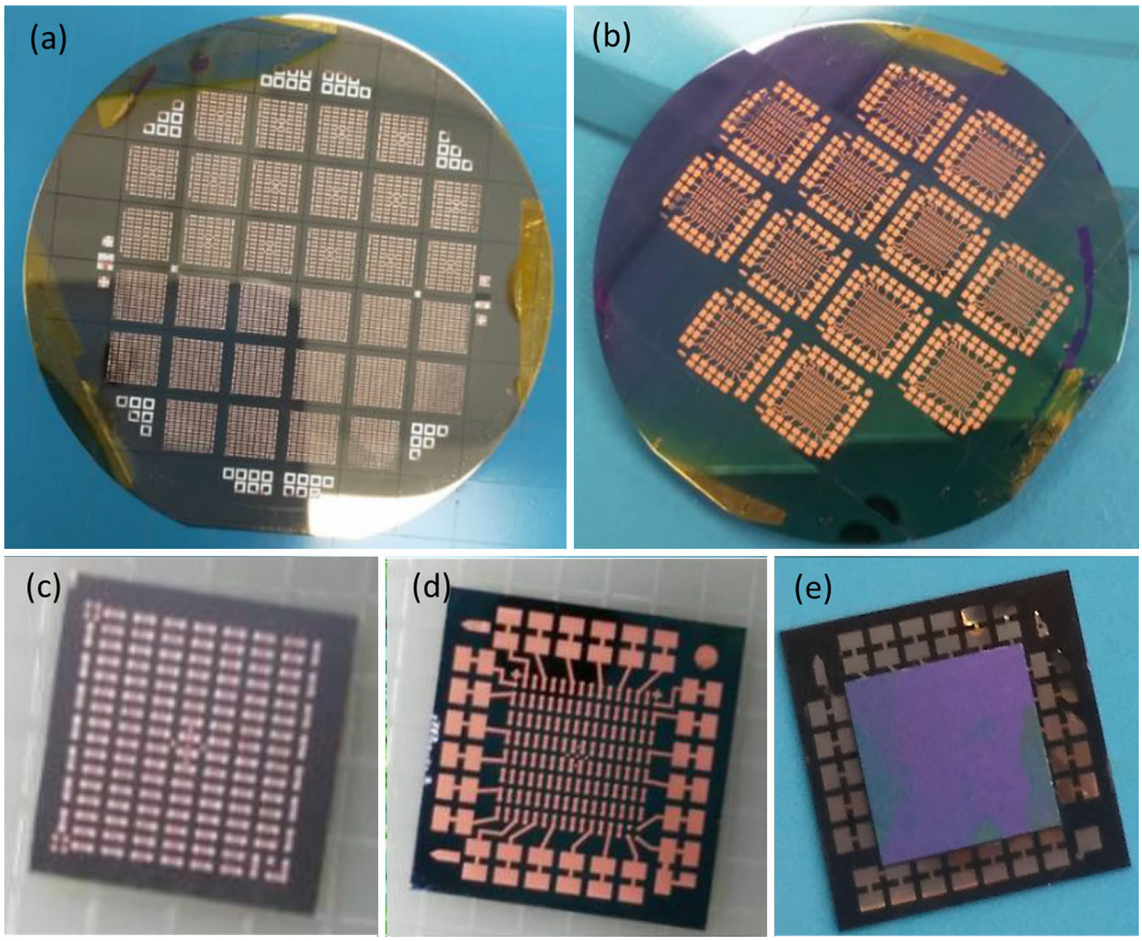



Fig. 11. Optical images of (a) device wafer having bottom RDL and Sn capped Cu pillar, (b) substrate wafer having top RDL and electrical measurement pad, (c) single die after dicing, (d) substrate die, and (e) flip-chip bonded die.

exception to that observed in samples annealed at 275°C and 300°C. Further, the shift of dominant IMC formation was also not very sharp in samples annealed at 250°C. Upon critical observation of IMC growth at 250°C (Fig. 7a), it is observed that the $Cu_6Sn_5$ and $Cu_3Sn$ thicknesses showed crossover at around 110 min of annealing, and the samples annealed for 150 min at 250°C had higher $Cu_3Sn$ thickness than that of $Cu_6Sn_5$. Thus, it can be concluded that at 250°C, there is a transition from $Cu_6Sn_5$ dominant growth to $Cu_3Sn$ dominant growth, but it occurs very slowly. Also the IMC thicknesses were lesser than those expected from the numerical simulations (Table II).

Observing the IMC growth at 275°C, it can be clearly observed that the $Cu_6Sn_5$ IMC growth rate was very high in the initial stage of annealing, but later it slowed down with time as pure Sn got fully consumed and thus $Cu_3Sn$ thickness increased. On the contrary, $Cu_3Sn$ growth rate is lower at the beginning but as annealing proceeds, it starts to dominate the IMC growth and grows by consuming $Cu_6Sn_5$ IMC. A similar trend is observed in samples annealed at 300°C. The critical time durations for 275°C and 300°C were 35 min and 16 min, respectively (Fig. 7b and c). It is observed that as annealing temperature increases, $Cu_3Sn$ IMC growth dominates rapidly over the $Cu_6Sn_5$ IMC growth rate. The experimentally observed IMC thicknesses were not in very good agreement with those predicted by numerical simulations (Table II). The reason for this deviation was investigated, and it was observed that pure Sn available while annealing at the given temperature was reduced due to the fact that it flowed away from the bond pads once the temperature was above the melting point of pure Sn. This argument was confirmed by observing the Sn flowing in dies as shown in Fig. 13.

However, this argument does not completely explain the reason for reduced IMC thickness observed in experiments because the samples annealed at 250°C showed reduced IMC thicknesses, too. Therefore, the second reason for this is attributed to voids at the Cu-$Cu_3Sn$ interface, which retards the Cu influx diffusion towards the IMCs and result in reduced IMC growth. The void fraction was observed to be maximal for samples annealed at 250°C, which fairly explains the reduced IMC

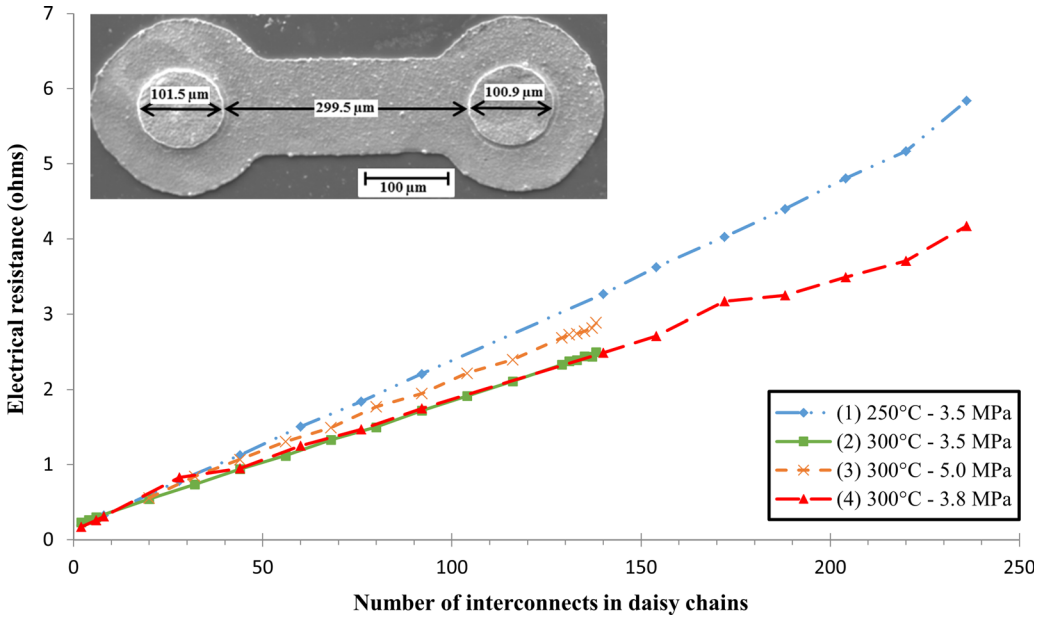



Fig. 12. Electrical resistance of daisy chain having increasing number of electrodeposited Cu-Sn bonded structures. The inset shows SEM image of a Cu RDL with perfectly aligned Cu pillars used in daisy chain structures.

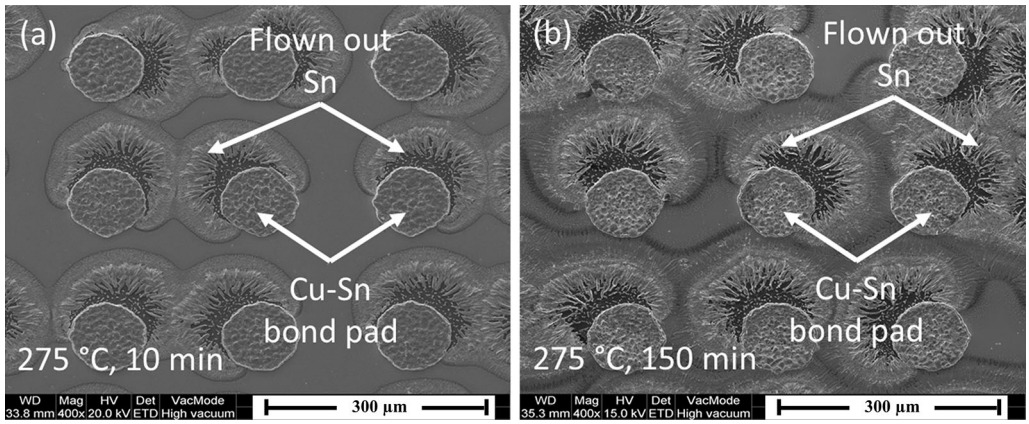



Fig. 13. Pure Sn flowing out of the bond pads while annealing for different time durations, i.e., samples annealed at (a) 275°C for 10 min and (b) 275°C for 150 min.

growth by acting as a diffusion barrier. Moreover, a major reason for reduced IMC growth could be completely different diffusion parameters than those taken in numerical simulations from the literature.

## Void Growth

Increasing void size and decreasing void fraction with increasing annealing time is mainly due to the coalescence of small sized voids to form larger voids. As annealing proceeds, initially voids tend to nucleate at thermodynamically favored locations like grain boundaries and in the vicinity of impurities, which are incorporated in the metal while electrodeposition. Once all the thermodynamic prospective locations are accumulated by voids, the void size tends to increase due to the movement and accumulation of diffused vacancies (i.e., due to the Kirkendall effect) at the pre-existing voids. This is followed by coalescence of nearby voids to form larger voids. This results in larger voids for longer annealing time duration and at the same time the number of voids decreases too, since smaller voids coalesce to form bigger voids. Thus, void size shows an increasing trend and void fraction shows decreasing trend with increasing annealing time durations for each annealing temperature.

The voiding data for samples annealed at 275°C for 150 min is not presented in the plots, since there were nearly no $Cu_3Sn$-$Cu_6Sn_5$ interfaces itself in these samples and, even if some small amount of

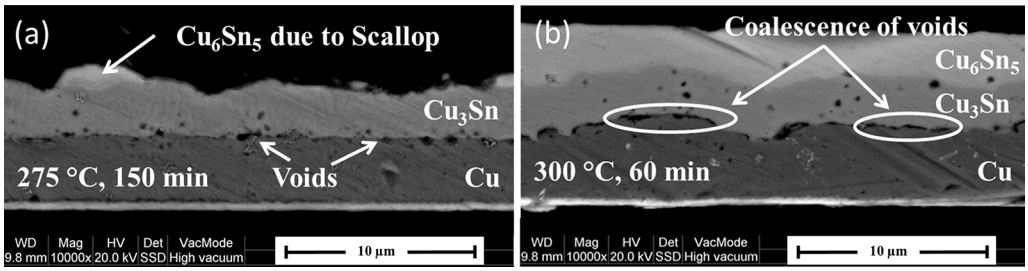



Fig. 14. SEM micrograph of bond pad structures annealed at (a) 275°C for 150 min, showing no $Cu_3Sn$-$Cu_6Sn_5$ interface voids, (b) 300°C for 60 min, showing high voiding level at Cu-$Cu_3Sn$ interface.

interface was there, then there were no voids present, as previously shown in Fig. 6. Absence of the $Cu_3Sn$-$Cu_6Sn_5$ interface is attributed to unavailability of sufficient pure Sn at annealing temperature. Pure Sn flowed away from the bond pad structures while annealing since the temperature was higher than the melting temperature of Sn ($T_{m,Sn}$ = 232°C). This resulted in reduced $Cu_6Sn_5$ thickness which, in turn, got completely converted to $Cu_3Sn$ in 150 min of annealing at 275°C. In some samples, a small amount of $Cu_6Sn_5$ was observed (shown in Fig. 14a) which are attributed to non-uniform scallops of $Cu_6Sn_5$ at some locations, but even then $Cu_3Sn$-$Cu_6Sn_5$ interfaces did not contain any voids at all. Few arbitrary bond pads (specifically annealed at 300°C) showed excessive voiding levels at the Cu-$Cu_3Sn$ interface that $Cu_3Sn$ IMC layer was separated from the base Cu metal at some locations, for instance, a bond pad having high voiding level is shown in Fig. 14b. It can be observed that at some locations, $Cu_3Sn$ was almost completely separated from the base Cu layer.

Intermittent voids formation at the Cu-$Cu_3Sn$ interface is mainly due to the following two reasons. First, the impurities incorporated in electrodeposits while electroplating[18–20] and second, the Kirkendall effect,[21] i.e., void formation due to difference in the diffusion rate of metals into another metals or their intermetallic. This imbalanced diffusion results in vacancies movement to compensate for the extra material diffused away and these atomic vacancies accumulate at thermodynamically favored locations to form voids. Experimental results in the literature have shown that void growth is more rigorous and severe in electroplated Cu than that in high quality Cu foils, e.g. rolled Cu or oxygen free high conductive (OFHC) Cu.[22,23] This is due to the presence of chlorine and sulphur, which gets incorporated in the electrodeposit, and contributes to the void formation. Recent studies have also shown that impurities incorporated while electroplating depends upon electroplating solution composition and age[24] as well as electrodeposition current density.[19] Thus, impurities incorporated while in electrodeposition is the major reason for void formation at the Cu-$Cu_3Sn$ interface rather than the Kirkendall's effect being the only reason.

Void formation in $Cu_3Sn$ IMC and $Cu_3Sn$-$Cu_6Sn_5$ interface is attributed to vacancy accumulation at thermodynamically favorable sites, i.e., impurities, dislocations and grain boundaries since these locations have higher free energies and vacancy accumulation decrease the free energy. Therefore, the vacancies, moving towards the Cu-$Cu_3Sn$ interface due to Kirkendall's effect, partially get entrapped at these locations to form microvoids. A significant part of the voids formed at $Cu_3Sn$-$Cu_6Sn_5$ interface did not move with the moving $Cu_3Sn$-$Cu_6Sn_5$ interface and gets incorporated within the $Cu_3Sn$ IMC resulting in $Cu_3Sn$ voids. And at the $Cu_3Sn$-$Cu_6Sn_5$ interface, none to negligible voids are observed (Fig. 6) having void fraction $< 0.15\ \mu m^{-1}$.

## CONCLUSION

IMC formation and void growth in electrodeposited Cu and Sn metal stacks at 250°C, 275°C and 300°C has been presented for hermetic encapsulation of MEMS devices. Scallop-shaped non-uniform $Cu_6Sn_5$ ($\eta$-phase) and comparatively uniform $Cu_3Sn$ ($\varepsilon$-phase) are observed at the Cu-Sn interface. $Cu_6Sn_5$ growth is observed to dominate over $Cu_3Sn$ growth at the beginning of annealing and thus initially has higher $Cu_6Sn_5$ thickness than that of $Cu_3Sn$. As annealing proceeds, $Cu_3Sn$ growth dominates over $Cu_6Sn_5$ growth since $Cu_3Sn$ forms by consuming the already formed $Cu_6Sn_5$. The time duration of $Cu_6Sn_5$ dominant growth (critical time duration) is controlled by annealing temperature, i.e., at lower temperature it was observed to be high and at higher temperature it was low. Sn thickness is observed to be a very critical parameter since excess Sn available at the melting point of Sn flowed away from the bond pad structures. Experimental results of void and IMC growth clearly imply that void formation and IMC growth are correlated and void formation precludes IMC growth by acting as a diffusion barrier for diffusion species. Void growth in this study showed minimum voiding level at samples annealed at 275°C.

Based on the findings of this study, a test vehicle having daisy chains containing a large number of Cu pillars was fabricated. Electrical resistance of individual kelvin vias and daisy chains were measured to be 30 mΩ and 6 Ω, respectively, which are

lower than the conventional bonding materials. This study gives IMC and voids growth, which will be applied in Cu-Sn assisted, SLID bonding for hermetic encapsulation of MEMS devices.

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