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Joining Using Reactive Films for Electronic Applications: Impact of Applied Pressure and Assembled Materials Properties on the Joint Initial Quality

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The use of local and rapid heating of electronic assemblies can significantly reduce the degradation of temperature-sensitive materials and substrate bowing commonly encountered in electronic applications during the high temperature reflow process. It can also allow assembling electronic packages on a non-planar surface and/or on massive structures that are very complex using a conventional oven for soldering. In order to attach electronic components to substrates, a rapid soldering process using an exothermic reactive foil sandwiched between solder preforms was evaluated. Once the film was activated and reacted, the solder preforms were melted to ensure the adhesion between the assembled materials. The effect of applied pressure on the joint quality, the reactive film thickness, as well as the attached material thickness and physical properties were assessed. Using a 60 μm thick reactive foil with two 25 μm thick SnAgCu305 preforms, results show that the fraction of void-free interfacial area between a metallized diode and an active metal braze substrate increased from 34% to 74% with pressure values between 0.5 kPa and 100 kPa, respectively. At a constant pressure of 13 kPa, increasing the reactive foil thickness from 40 μm to 60 μm leads to an increase in the void-free interfacial attach area ratio from 20% to 40%, and a value of 54% was achieved by using two 60 μm foils under the same conditions. The substrate metallization and solder thickness also affect the joint quality. The experimental results are analyzed and correlated with the duration of liquid solder using thermal models.

Key words: Reactive film, nanolayers, soldering, joint quality, melting duration, high temperature electronics

INTRODUCTION

The development of wide band gap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) power devices operating at high temperature (> 200°C)[1,2] as well as the large demand for their use in various industries, drive the electronics applications toward harsher thermal environments. New packaging materials suited to more severe thermal constraints is mandatory to achieve high performance and reliability of systems employing such new high operating temperatures power semiconductor dice. Among others, die attaching materials must be developed to meet these requirements. Conventionally, the electronic components (power semiconductor devices, capacitors, resistors…) of the power module are attached to the substrate by the use of solder paste or solder preform combined in a reflow process in an oven. High temperature lead (Pb), gold (Au), zinc (Zn) and bismuth (Bi) based solders with an operating temperature above

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200°C are commercially available on the market. Each of those solders has its drawbacks. In fact, Bi based solders suffer from poor thermal conductivity and wetting behavior on copper surfaces, Zn based solders present issues related to Zn oxidation and brittle ZnCu intermetallic creation, Au based solders have high cost and are considered as hard solders with limited thermomechanical reliability and finally the Pb compounds threaten human life and the environment.[3] As a rule of thumb, in order to achieve a reliable joint under thermal cycles, solders should be used below 80% (temperature in Kelvin units) of their melting temperature before creep effects lead to a fast degradation of the joint.[4,5] Hence, for an operating temperature of 200°C, the melting temperature of the solder should be higher than 320°C. Such high temperatures reached during the reflow cycle can affect the electronic components reliability.[6,7] In addition, since the whole package includes various materials with different coefficients of thermal expansion (CTE), mechanical stresses are induced during the soldering and can lead to the bowing of the substrate or even more pronounced failures such as cracks apparition.[8,9] To prevent issues related to the heating of the whole package above 300°C, local heating techniques using laser source or other local heating sources can be advantageously used.

In this paper, we will focus on the use of reactive foil soldering technique that can be performed at room temperature without the need for any external heat sources (oven, microwave, laser…). When the reactive foil is activated, an exothermic reaction occurs. The rapid and localized heating allows the joining of temperature sensitive materials and components without thermal induced damage using high temperature melting point solders. This process is also advantageous for making assemblies with materials having a large difference in the CTE without induced bowing or cracking. Moreover, the process can allow assembling of electronic packages on a non-planar surface and/or on massive structures and can be useful for plastronic applications. However, when the reactive film is activated, complex physical mechanisms are taking place.[10] Predicting the quality of the achieved joint in terms of basic materials physical properties is difficult, because there are many intrinsic physical and chemical properties that contribute to the final obtained result. The aim of this paper is to study the effect of process parameters (applied pressure, amount of foils) as well as the assembled materials physical properties and dimensions on the final quality of the joint. All the chosen materials are commonly used in electronics applications like power semiconductor components, printed circuit board PCB, metallized ceramic substrates…. Experimental results are correlated to the finite element transient thermal model in order to extract an output parameter that can be used to predict the quality of the joint using virtual prototyping considering adequate assumptions. This paper is expected to represent a cornerstone for researchers and industrials working on the development of harsh environment reliable electronic modules, smart motors with integrated electronic components as well as plastronic applications.

ALTERNATIVE TECHNOLOGIES WITH LOW TEMPERATURE PROCESS AND HIGH OPERATION TEMPERATURE

New high temperature die attach technologies have emerged during the last decade and the low temperature micro and nano-particles sintering of metals (mainly copper and silver) seems to be one of the most promising and attractive technologies. This is due to the high thermal and electrical conductivity of the sintered joint, its low process temperature (about 250°C), its high operating temperature that corresponds in theory to the silver or copper melting temperature (960°C and 1085°C, respectively), and its low elastic modulus.[11,12] However, some drawbacks related to this process have been identified limiting thereby its use. For example, the need of high pressure (> 1 MPa) during the process for the micro-silver particles and micro- and nano-copper particles (due to the requirement of a special equipment and the process complexity if the devices that should be assembled have various thickness), the oxidation issues of copper nanoparticles,[13,14] and the high porosity level in the pressure free low temperature (< 260°C) realized joint using silver nanoparticles as well as its high cost.[15] Recent progress in process, particle and paste development has allowed to solve the oxidation issues for copper paste by using laser rapid sintering,[13] inert atmosphere[16] and shell protected copper particles.[17,18] However, we should note that a high porosity level in a pressure free low temperature sintered joint can help in relieving internal stresses in the joint.[19]

Transient liquid phase bonding (TLPB) is another potential technology that can meet the high temperature application requirement. The first metal owning a low melting temperature (In, Sn) is sandwiched between two layers of a base metal with high melting temperature (Cu, Au, Ag).[20] During the bonding process at a temperature above the liquidus of the first metal, sandwiched structure is held under low static pressure (several kPa) to ensure direct contact. The first melted element reacts with the base metals and creates intermetallic compounds until its complete consumption. The main advantage of this technology is that the remelting temperature of the joint rises from the melting point of the inter-layer to the melting point of the intermetallic compound. TLPB allows a joint with medium thermal conductivity (20–60 W/mK), low electrical resistance, reasonable cost and limited density of voids by controlling the process. However, the process remains complex due to the

long time and the pressure need to ensure good contact. In order to reduce the process time, preforms using Cu micro-particles of 30 μm diameter encapsulated with thin Sn layer (< 5 μm) and pressed together have been developed and evaluated.[21]

Organic die attach are composed from matrix polymer filled with high conductive fillers (Ag, carbon fiber, graphene…). Generally, Ag filled organic die attach materials can be used for applications ranging from − 60°C to potentially + 300°C according to the manufacturer data sheets. However, to the best the of authors' knowledge, those adhesives have not been investigated for operating temperature above + 200°C. Apart from the thermal degradation of the organic die attach, one of the main disadvantages of those materials is their low thermal and electrical conductivity (about ten fold lower than conventional Pb based solders).

EXPERIMENTS AND MODELING

Infineon IDC51D120T6 M 100A (7.00 mm × 7.30 mm × 110 μm) silicon diodes with Al/Ti/Ni/Ag back metallization were attached on Cu/Si_3N_4/Cu active metal brazed (AMB) substrate with Ni/Au finishing purchased from Curamik. The thickness of Cu metallization and Si_3N_4 ceramic was 300 μm each. Direct bonded aluminum (DBA) Al/AlN/Al (300 μm/635 μm/300 μm) substrates with Ni/Au finishing purchased from Denka have been also used to evaluate the effect of the metallization material on the joint quality. PCB using FR4 material and Ni/Au finished copper metallization with a thickness of 35 μm and 70 μm were tested as substrate to evaluate the impact of metal thicknesses. The use of the same finish layer on the different substrates allows us to neglect the effects related to the surface energy that can significantly affect the solder wettability. Reactive films composed of alternatively stacked nanolayers of Ni and Al are commercialized under the trademark NanoFoil® by Indium Corporation where 40 and 60 μm thickness were used. When one reactive film was used, the latter was sandwiched between two solder preforms that are in contact with the assembled components. The reactive film can be activated by different techniques, and we have used the electric discharge activation process for simplicity reasons. After activation, the film formed from consecutive nanolayers on Ni/Al, and an exothermic reaction takes place and allows the solder preform melting. In case of the use of two reactive films, an additional solder preform between the two reactive films was used and accordingly each of them was sandwiched between two solder preforms. The 25 μm and 50 μm thick SAC305 and 50 μm thick $Au_{80}Sn_{20}$ solder preforms were evaluated. Once the assembly is prepared, a small pressure was applied on the top of the dies by using a stainless steel weight and then the reactive film was activated using an electrical power source. Stainless steel weights were thermally decoupled from the die by using a 250 μm porous Teflon film on the top of the die. The process steps and the final assembled sample are illustrated in Fig. 1a and b, respectively.

The joint initial quality was evaluated using scanning acoustic microscopy coupled to image treatment software. The test conditions with different used parameters are presented in Table I. The impact of pressure was evaluated by varying the pressure parameter of the condition number C2.

From a purely thermodynamic point of view, the needed energy by surface unit to melt the solder SAC305 and $Au_{80}Sn_{20}$ by considering a room temperature of 25°C can be calculated using the following equation:

$$Q = \rho.e.(T_m - T_a)Cp + \rho.e.hf, \quad (1)$$

where T_m is the solder melting temperature, T_a is ambient room temperature, ρ is the solder density, Cp is the specific capacity, e is the thickness and hf is the heat of fusion.

For 50 μm $Au_{80}Sn_{20}$ and SAC30 (25 μm each layer in contact with the reactive film) the energy needed

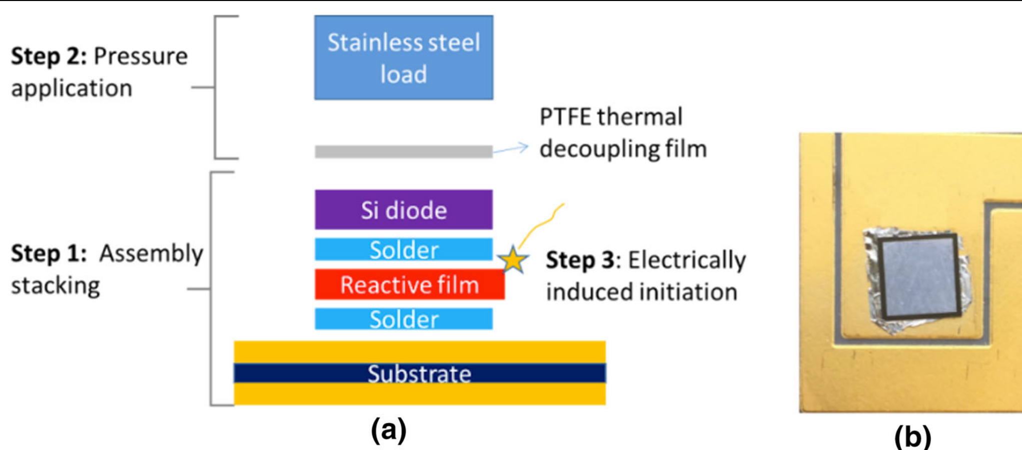


Fig. 1. Schematic illustration of the process steps (for clarity reasons dimensions are not to scale) (a) and top view of the assembled sample (b).

Table I. Synthesis of various test conditions using a constant pressure of 13 kPa and silicon die of 100 μm thicknesses

Condition number	Substrate nature	Reactive film thickness (μm)	Metallisation thickness (μm)	Solder nature	Solder thickness (μm) × number	Pressure (kPa)
C1	$Cu/Si_3N_4/Cu$	40	300	SAC	25 × 2	13
C2	$Cu/Si_3N_4/Cu$	60	300	SAC	25 × 2	13
C3	$Cu/Si_3N_4/Cu$	40 × 2	300	SAC	25 × 3	13
C4	$Cu/Si_3N_4/Cu$	60 × 2	300	SAC	25 × 3	13
C5	$Cu/Si_3N_4/Cu$	60	300	AuSn	50 × 2	13
C6	$Cu/Si_3N_4/Cu$	60	300	SAC	50 × 2	13
C7	Al/AlN/Al	60	300	SAC	50 × 2	13
C8	FR4/Cu	40	35	SAC	25 × 2	13
C9	FR4/Cu	40	70	SAC	25 × 2	13
C10	FR4/Cu	60	35	AuSn	50 × 2	13
C11	FR4/Cu	60	35	SAC	25 × 2	13

for melting was calculated to be 57 kJ/m^2 and 41 kJ/m^2, respectively. The dissipated power generated by the reactive foil has been calculated for various film thicknesses using an enthalpy value of 1180 J/g deduced by considering an Al/Ni bilayer of 80 nm thick from Ref. 22. The energy dissipated by the 40 μm and the 60 μm reactive films was calculated to be 260 kJ/m^2 and 390 kJ/m^2, respectively, which is largely sufficient to melt the solders. However, in a real case, other parameters should be considered like the joining materials physical properties that governs the heat transport equation, the melted solder properties (viscosity, surface energy,...) as well as the interfaces properties (thermal contact conductance, surface wettability and roughness).

The temperature evolution in the package can be obtained by integration of the energy conservation equation, which is independently solved within layers constituting the final assembly:

$$\rho \frac{\partial h}{\partial t} = \nabla \emptyset + Q, \tag{2}$$

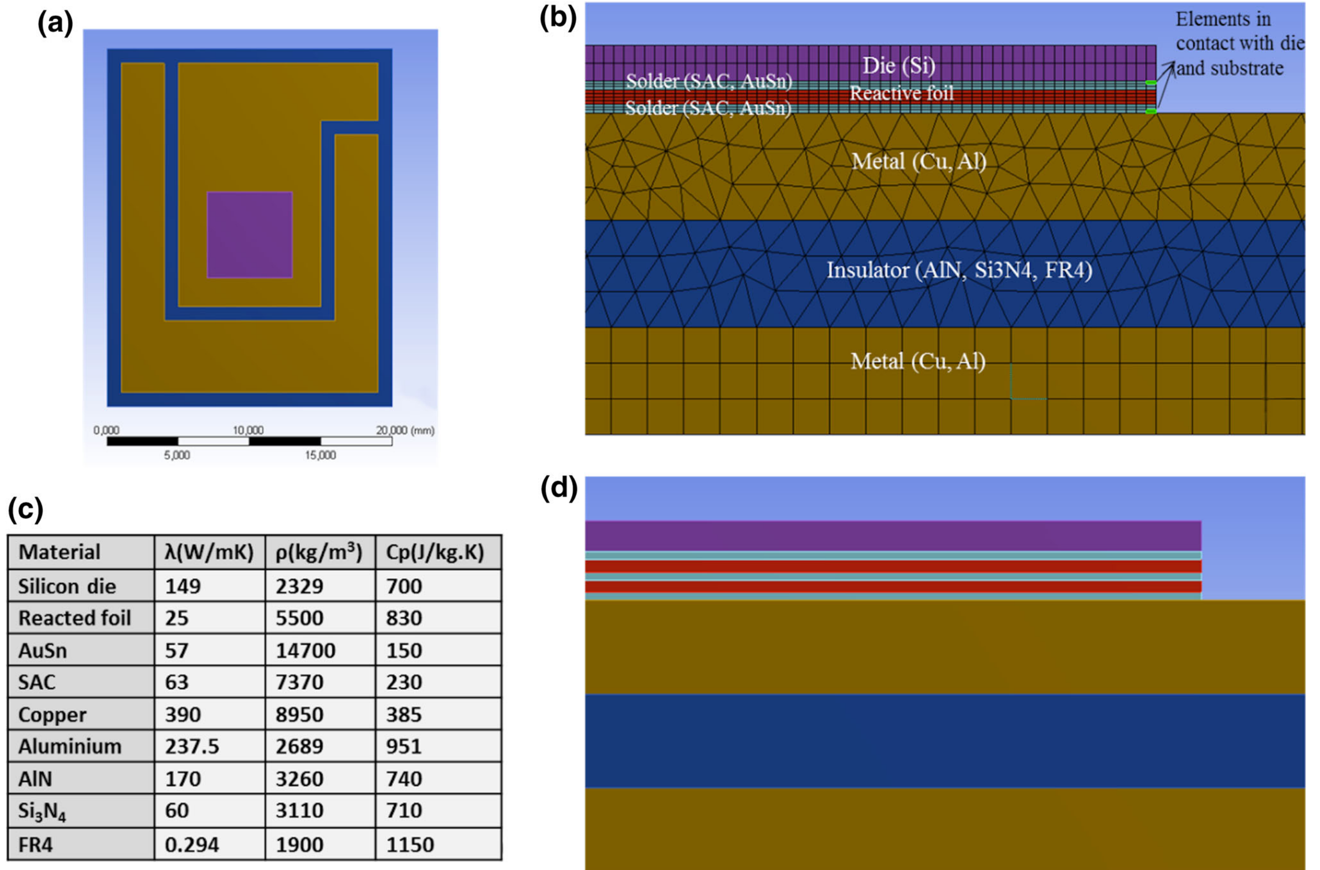
where ρ and h are the density and enthalpy, respectively, t is time, $\emptyset$(W/m^2) is the heat flux density and Q (W/m^3) is the power density generated by the reactive film. The enthalpy h is related to the temperature through the equation including the heat of fusion hf and the specific capacity C_p. In the layers where no phase change materials are considered, the simplified equation can be written as follows:

$$\nabla(\lambda \nabla T) + Q = \rho C_{th} \frac{\partial T}{\partial t}, \tag{3}$$

where the thermal capacitance of the material C_{th} (J K^{-1}) = $C_p \rho V$, V the volume, and λ (W/mK) is the thermal conductivity. For the thermal transient simulation, simulation were performed using Ansys final element software, and a natural convection was applied on the surface of the non-joined surfaces with a heat transfer coefficient value of 20 W m^{-2} K^{-1} and a room temperature of 25°C. The contact resistance between the layers is considered to be non-significant, and the interface effects are neglected. The reaction speed in the reactive film was not considered. In fact, the effect of this parameter on the solder melting duration was found to be negligible for a short distance of several mm.[23] The schematic top and the cross-section views of the assembly used for experimental tests and for modeling are presented in Fig. 2a, b, and d. Physical properties of the assembled materials used in the simulation are presented in Fig. 2c.

An example of the temperature distribution as a function of the distance has been simulated for a duration up to 1 s after the reactive film initiation by using the condition number C1 and the results at various times are illustrated in Fig. 3. The first presented value corresponds to the temperature distribution after 10^{-2} ms after the foil initiation. The maximum temperature value in the 40 μm thick reactive films can exceed the 1000°C and the maximum temperature at the semiconductor surface can reach 400°C for durations less than 0.5 ms. This latter temperature drops below 250°C, 1 ms after the initiation. The maximum temperature reached in the ceramic of the metallized substrate is below 100°C which remains significantly lower and shorter than the temperature obtained during a conventional reflow process (about 300°C for several tens of seconds). This can allow a drastic reduction in the residual stresses in the package during the joining process. Additionally, the joining process duration is significantly reduced since one second after the initiation; the assembly temperature is about 30°C.

The melting duration of the solder is an important parameter that can be related to the joint quality. In fact, a short melting duration during the assembly process will reduce the ability of the solder to flow as well as its surface wettability and will lead to large nonwetted surface. Simulations show that the melting duration in the solder in contact with the substrate is lower than the one which is in contact



Material	λ(W/mK)	ρ(kg/m³)	Cp(J/kg.K)
Silicon die	149	2329	700
Reacted foil	25	5500	830
AuSn	57	14700	150
SAC	63	7370	230
Copper	390	8950	385
Aluminium	237.5	2689	951
AlN	170	3260	740
Si_3N_4	60	3110	710
FR4	0.294	1900	1150

Fig. 2. Top view of the modeled sample (a) and cross-section view using one reactive foil (b) and two reactive foils (d) of the simulated package. The elements used to extract the solder melting duration are pointed out by the arrows (b). The material physical properties used in the transient thermal simulation are illustrated on (c).

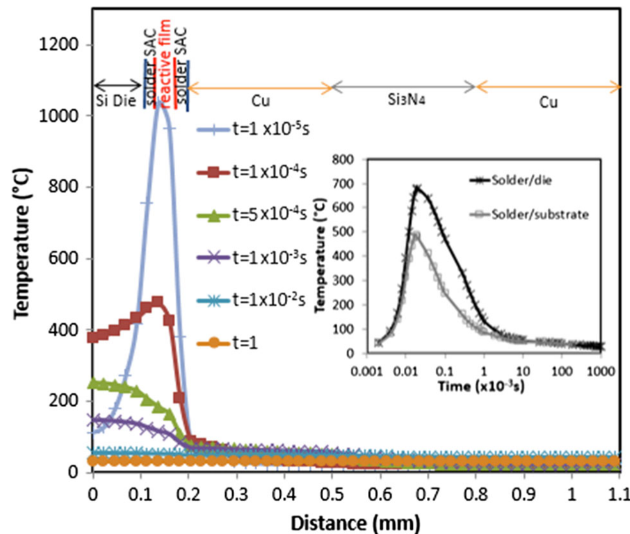


Fig. 3. Temperature distribution in the assembly at different times after the reactive foil initiation. The inset shows the temperature variation as a function of time of the two solders elements in contact with the substrate and the die.

with the die as presented in the inset of the Fig. 3. The results were considered on the pointed solder elements in contact with the substrate and die shown in Fig. 2b. Accordingly, since the solder melting duration is more critical for the solder in contact with the substrate, its value was considered next. The melting duration was simulated as a function of reactive foils thickness and amount, the solder nature and thickness, substrate metal and insulator materials and their thicknesses.

RESULTS AND DISCUSSION

Effect of Applied Pressure

For oven conventional soldering, it has been reported that increasing the pressure during the reflow process can enhance the flow of the solder and helps to eliminate voids by using reduced temperature and reflow process duration.[24] In addition, the effect of pressure during a reactive foil soldering to join bulk stainless steel and Al materials shows a positive impact on the joint mechanical strength until a critical value above which the pressure impact becomes negligible.[25] In our case, the pressure effect on the void free surface ratio between 100 μm thick Si diodes and $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) AMB substrates was evaluated for pressure values in the range of 0.5 kPa to

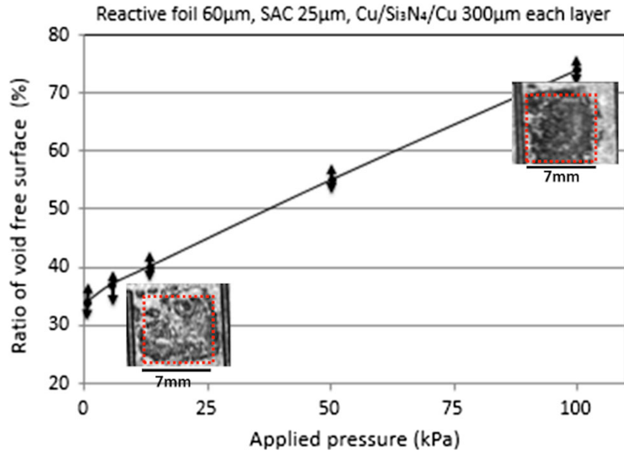


Fig. 4. Effect of the applied pressure on the ratio of the void-free surface using 60 μm reactive films with 25 μm SAC305solder preforms, 100 μm thick silicon diode and $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) substrate. Double headed arrows indicate the standard deviation which remains less than 4% for all conditions. The SAM images are inserted for 13 kPa and 100 kPa, and the red lines denotes the die borders.

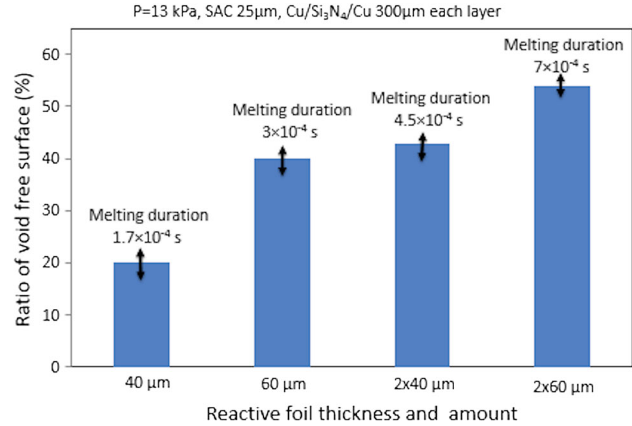


Fig. 5. Impact of the reactive film thickness and amount on the ratio of void free surface and the melting duration using a pressure of 13 kPa, 25 μm SAC solder preforms, 100 μm thick silicon diode and $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) substrate. Double headed arrows indicate the standard deviation which remains less than 4% for all conditions.

100 kPa by using a 60 μm reactive foil thickness sandwiched between 25 μm SAC305 preforms. As presented in Fig. 4, the pressure increase induces a strong improvement on the joint initial quality and the ratio of void-free surface varies from 34% to 74% for pressure between 0.5 kPa and 100 kPa, respectively. In the mentioned pressure range, the relationship between the pressure and the ratio of joint free surface is linear with a calculated slope of 0.39%/kPa. This can be explained by the improvement of the solder flow under higher pressure leading to a better surface wettability and void elimination. In addition, it has been reported that the contact conductance is increased by increasing the pressure.[26] Higher thermal conductance values induce a better thermal transfer and fewer losses during the joining process that can also improve the joint quality. In the next sections, a pressure of 13 kPa was used since it remains simple to apply manually by using weights on components and does not impact potential pressure sensitive components of the assembled parts.

Effect of Reactive Foil Amount and Thickness

Increasing the foil thickness as well as the amount of the foil allow for improving the ratio of void free attached surface. As presented in Fig. 5 for 100 μm thick silicon diode, $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) substrate, a pressure of 13 kPa and 25 μm SAC305 preforms, the ratio of void-free attached surface is doubled when the reactive film thickness varies from 40 μm to 60 μm. Doubling the foil amount lead to 100% and 40% improvement in the joint initial quality for the 40 μm and 60 μm thickness films, respectively. The additional power induced by increasing the thickness and the amount of reactive foil increases the duration of melting as mentioned in Fig. 5 (data is extracted from the aforedescribed model as a function of reactive film thickness and amount), and; hence, it improves the solder flowing and a better surface wettability is obtained.

Effect of the Nature of Solder, Substrate Metallization and Insulator

While the heat of fusion of the used $Au_{80}Sn_{20}$ (34.2 J/g) is lower than SAC305 (67 J/g), which can be advantageous from a thermodynamic point of view, its fusion temperature as well as the product of its density and its specific capacity are higher and lead to a lower duration of melting compared to SAC. For experimental results, a 13 kPa applied pressure was used to attach 100 μm Si die to the $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) substrate using 50 μm $Au_{80}Sn_{20}$ and SAC305 solder preforms. When a 60 μm reactive film thickness is used, the ratio of the attached surface is 0% and 25% for gold and tin based solders, respectively.

Varying the substrate metallization nature can also have an impact on the solder preform melting duration and the joint quality. This was evaluated by comparing an aluminum metallized substrate (Al/AlN/Al (300 μm/635 μm/300 μm) compared to a copper metallized substrate ($Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm)). Since the ceramic insulator is different between the two substrates, and in order to decouple the effect on metallization nature from the insulator one, various insulators with different metal thicknesses have been modeled. It is clear from the results presented in Fig. 6, that for thin metal layers, the substrate electric insulators physical properties (FR4, AlN and Si_3N_4) drastically affect the solder melting duration. Since the $Cp \times \rho$ product is very close between AlN and FR4

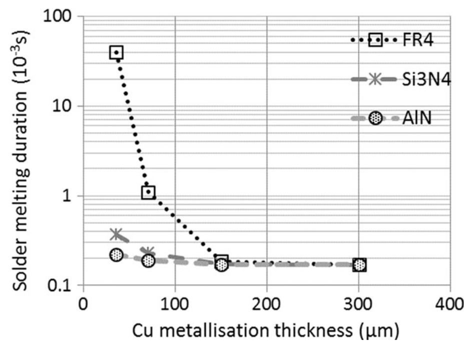


Fig. 6. Variation of solder melting duration as function of copper thickness for various insulated substrates.

insulation layers, their thermal conductivity is the main parameter that can explain the observed variation in the solder melting duration. Results show also that for thick copper thickness (above 150 μm) the nature of the insulator did not affect the melting duration of the solder. Accordingly, the impact of thick metallization can be compared on different insulators while this comparison is not valid for thin metallization. Under an applied pressure of 13 kPa and by using an 60 μm reactive film and 50 μm SAC solder preforms to join 100 μm silicon die on the Cu/Si_3N_4/Cu and Al/AlN/Al substrates, the measured ratio of the void free surface attach were 25% and 50%, and the calculated solders melting duration was 0.25 ms and 0.5 ms, respectively. The higher melting duration and, consequently, the higher ration of void-free surface attach on the Al metallization can be explained by its lower thermal conductivity as well as its lower $Cp\times \rho$ product compared to copper, which strongly impacts the heat transfer mechanisms in the package (Eq. 3).

Effect of Solder and Substrate Metal Thicknesses

In order to evaluate the impact of the solder preform thickness on the ratio of void free surface attach, 25 μm and 50 μm SAC preforms were used. At 13 kPa applied pressure, and by using a 60 μm reactive film to join 100 μm silicon die on the Cu/Si_3N_4/Cu substrate, the value of the ratio of void-free surface was 40% and 25% for 25 μm and 50 μm preform, respectively. This dependence can be explained by the fact that when using a constant energy source (produced by the reactive film), the increase of the solder thickness will consume additional energy in order to reach the melting temperature as well as for phase changing. Accordingly, the maximal temperature attended in the thicker solder as well as the melting duration were expected to be lower. The calculated maximum temperature and the solders melting duration were 364°C/0.25 ms for the 50 μm SAC solder preforms and 483°C/0.3 ms for the 25 μm ones, respectively. As already mentioned, longer melting duration combined with higher solder temperature will improve the solder flow and its substrate wettability and can explain the better joint initial quality observed for thinner solder preforms.

Since the effect of the copper substrate metallization thickness on the solder melting duration is more pronounced using low thermal conductivity substrate (like FR4) and can be neglected when using high conductive ceramics like AlN (see Fig. 5), the FR4 based substrate was used for low thickness metallization. Simulation results also show that the insulator nature has no impact on the melting duration for metal thicknesses ≥ 150 μm. Hence, the comparison of the metallization thickness effect using both Si_3N_4 and FR4 substrate for thick and thin metallization, respectively, can be allowed. Using a reactive film of 40 μm thickness and SAC solder preform of 25 μm thickness under a pressure on 13 kPa, the ratio of void free surface in the joint between Si diodes and the substrates was found to be 85%, 75% and 20% for 35 μm, 70 μm and 300 μm copper thicknesses, respectively. The strong increase of the solder melting duration from 0.17 ms to 40 ms, when thinner copper is used, can explain the improved joint quality. In addition, 80% of void free attached surface was obtained using 13 kPa with 60 μm reactive film and 50 μm $Au_{80}Sn_{20}$ solder preform on PCB with 35 μm copper thickness, while there was no attach under the same conditions when AMB 300 μm copper thickness substrate was used.

Void Free Surface to Melting Duration Relationship

Figure 7 illustrates the ratio of void-free attached surface versus the solder melting duration for test conditions presented in Table I. A critical melting duration of about 1 ms can be considered. Below this value, the ratio of void-free attached surface is strongly dependent on the melting duration and varies from 0% to 75% for duration between 0.1 ms to 1.1 ms, respectively. Above 1.1 ms, it seems that the effect of melting duration is very limited, and the highest ratio of 85% is reached using SAC305 solder under a pressure of 13 kPa (test condition 8). According to the net relationship between the solder melting duration and the ratio of void free surface obtained at a constant pressure, the use of the described model seems to be relevant and useful for joint initial quality optimization. However, it is believed that by increasing the applied pressure during the process, the critical value of melting duration can be significantly reduced, and this assumption is currently under investigation. On the other hand, it has been reported that increasing the solder temperature could be advantageous for the joint initial quality, since it can allow a reduction of the solder viscosity and surface tension and, hence, a better flow ability and wettability.[27] This

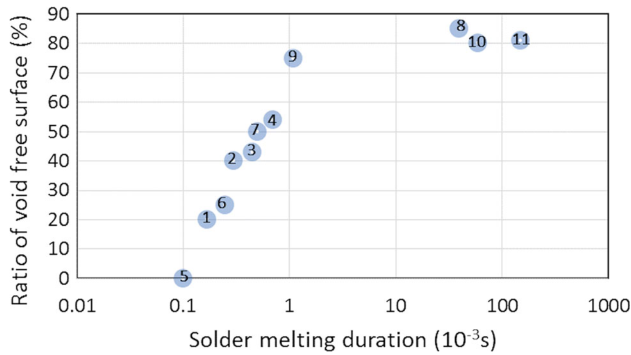


Fig. 7. Variation of the ratio of void free joint surface as a function of solder melting duration. The applied pressure was fixed at 13 kPa. The numbers filling the markers are the condition number detailed in Table I.

assumption seems not valid when the solder melting durations are different and very short. In fact, by plotting the maximum reached temperature in the solder as a function of the ratio of void free surface, results do not show any evidence relation between the two parameters.

CONCLUSION

Joining electronic components using reactive films and solder preforms is a promising and economically viable technology for high temperature electronics applications and for assembling electronic packages on non-planar surfaces and/or on massive structures. The impact of various parameters on the joint initial quality has been investigated such as the applied pressure, the thicknesses and the amount of reactive films, the solder preform and substrate metallization as well as the nature of the solder, the metallization and the insulator of the substrate. Since the flow ability of the solders is related to the pressure and to its melting duration, it was shown that increasing those two parameters allow the achievement of better joint quality. Finite element modeling was found to be a powerful and low cost tool to estimate the joint quality. Hence, increasing the foil thickness and amount, reducing the solder and the metal thickness, reducing the thermal conductivity and the product of the density by the specific capacity of the substrate metallization and insulator (when fine metallization is used) led to a higher ratio of void free attached surface. Under 100 kPa the ratio of the void free surface using 60 μm reactive film with 25 μm SAC solder preforms, 100 μm thick Si diode and $Cu/Si_3N_4/Cu$ (300 μm/300 μm/300 μm) substrate was about 75%. At a fixed low pressure of 13 kPa, the best joint initial quality with a void free surface ratio of about 85% was reached when using thinner metallization and low thermal conductivity insulator (35 μm thick copper on FR4) with 40 μm reactive film thickness and 25 μm solder preform. Under the same test conditions and by varying the copper thickness to 300 μm, the void-free surface ratio was limited to 20%. The authors are aware that for power electronics applications and in order to allow a good heat transfer between the dies and the heat sink and to prevent local heating, the void ratio should be less than 5%.[28] Those values have not been achieved under the described test conditions. However, according to the military standard 883 method 2030, the ultrasonic inspection of die attach requires that a single void should be smaller than 15% of the total solder joint area.[29] Hence, when 20% void level is achieved with multiple voids, the assembly can be certified, but an estimation of temperature rise of about 40% should be considered.[30] Otherwise, increasing the pressure above 13 kPa, preheating of the substrate, increasing the foil thickness as well as the initiation of the foil in vacuum can allow further improvement in the joint quality.

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