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Temperature and Interfacial Layer Effects on the Electrical and Dielectric Properties of Al/(CdS-PVA)/p-Si (MPS) Structures

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In the present study, cadmium sulphide (CdS) nanopowders were prepared by using a simple physical ball milling technique, and their x-ray diffraction (XRD) analysis confirmed the formation of hexagonal wurtzite structure of CdS. The morphology of CdS nanopowders was characterized by scanning electron microscope (SEM). Dielectric and electrical properties of the manufactured Al/(CdS-PVA)/p-Si (MPS) type structures were investigated by capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements as functions of temperature and applied bias voltage at 500 kHz. Some main parameters of the structure such as real and imaginary parts of complex dielectric constants, $\varepsilon'(=\varepsilon'-j\varepsilon'')$, loss tangent (tan δ), a.c. electrical conductivity (σ_{ac}), and real and imaginary parts of complex electric modulus, $M^*(=M'+jM'')$ of the structure were investigated in the temperature range between 230 K and 340 K. $\mathrm{Ln}(\sigma_{ac})$–q/kT curve showed a linear behavior. The value of activation energy (E_a) was obtained as 0.0601 eV at 5.0 V from the slope of this curve. Moreover, argand diagrams of complex modulus were studied to determine relaxation process of these structures.

Key words: CdS-PVA composites, nanostructures, thermal properties, electrical properties, dielectrical properties, conductivity

INTRODUCTION

Semiconductor–polymer nanocomposites films have significant roles in the fabrication of electronic and optoelectronic devices such as metal-polymer-semiconductor (MPS) type solar cells (SCs), light-emitting diodes (LEDs), organic field effect transistors (OFETs) and sensors.[1–7] II–VI semiconductor materials mixed with polymers can easily be enforceable for all semiconductor devices based on thin films.[8–10] Among these semiconductor materials, cadmium sulphide (CdS) shone through as an attractive compound for semiconductor device applications.[11] In particular, cadmium sulphide nanoparticles have aroused interest in the past two decades since they have useful physical and chemical properties such as their bulk band gap energy that varies from 2.17 eV to 2.48 eV at room temperature.[12–18] The band gap can be increased by modifying the nanoparticle sizes in different quantum confinement regimes. CdS has three types of crystal structures, namely wurtzite, zinc blend and rock-salt phase.[19,20] Among these, wurtzite is the most stable of the three phases and can easily be synthesized. In between the various polymeric materials, poly(vinyl alcohol) (PVA) embedded CdS which provides a good control over deposition and

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morphology in the material is a semi-crystalline and water soluble polymer. PVA also exhibits very important applications due to the role of the OH group and hydrogen bonds that steers the growth and morphology of embedded nanoparticles. In addition, it is also a good insulating material with low conductivity. However, high conductivity, high dielectric constant and low dielectric loss can be acquired by doping appropriate materials into the PVA such as nickel (Ni), zinc (Zn), cobalt (Co), and CdS.[21,22] In other words, their conductivity can be increased by doping some materials which are also protected by PVA against any oxidation. Recently, because of some properties such as the transparency in the visible range, good conglutination to hydrophilic surfaces and formation of good oxygen resistant films, PVA has become a more popular material, and it is preferred in the fabrication of numerous electronic devices.[23,24]

Especially, metal/(metal-doped polymer)/semiconductor (MPS) type structures have gained great significance due to their potential application areas in semiconductor technology, such as conventional metal/semiconductor (MS) contacts with and without interfacial insulator or oxide layer (MIS or MOS) structures.[21,25–29] The performance and stability of these devices are fairly affected by several factors, such as surface preparation, growth, thickness, and homogeneity of an interfacial polymer layer, doping concentration of donor or acceptor atoms in the semiconductor, series resistance (R_s), temperature of structure, applied bias voltage, and also the interface morphology, barrier height (BH), and surface states (N_{ss}) at the M/S interface.[30–32] Among these, especially the interfacial layer, the shape of BH, R_s, N_{ss} and sample temperature play significant roles in the electrical and dielectric behavior of MPS type structures. The polymeric layer may lead to interface state charges with voltage due to an external electric field in the dielectric layer and affect both the electrical and dielectric properties.[33,34] The temperature and voltage dependent impedance spectroscopy technique that includes C–V and G/ω–V measurements yield sufficient information on the electrical and dielectric characteristics of the MIS and MPS type structures. On the other hand, when these measurements were carried out, only one temperature or voltage is not able to supply sufficient information on the conduction mechanism, electric and dielectric properties. Therefore, to obtain more information on the electric and dielectric properties, the values of C and G/ω were measured in the temperature and voltage range of 230–340 K and (− 3 V)–(− 5 V), respectively.

In our previous study,[35] we published the frequency and voltage dependent electrical characteristics of Al/(CdS-PVA)/p-Si (MPS) type structures. The frequency dependence of C–V and G/ω–V characteristics of structure took into account the effects of N_{ss}, R_s and interfacial layer. Therefore, this study aims to measure the electric and dielectric properties of Al/(CdS-PVA)/p-Si (MPS) type structures as a function of temperature in the wide range of applied bias voltage in order to determine the variations of both the real and imaginary parts values of ε^* and M^*, tan δ and σ_{ac}. The value of E_a was obtained from the $\ln(\sigma_{ac})$–q/kT curve. Furthermore, argand diagrams of complex modulus were studied to determine the relaxation process in Al/(CdS-PVA)/p-Si (MPS) type structures.

EXPERIMENTAL DETAILS

In the present study, CdS crystals were used for the fabrication of diode materials. These were commercially purchased. PVA polymer was obtained from Merck. Relevant information on the structure of Al/CdS-PVA/p-Si SBDs and technical details of the manufactured stages can be found in our previous study.[35] For the measurements, the samples were mounted on a copper holder and then consequently electrical contacts were established with the upper electrodes by Cu wires using silver paste. The impedance measurements were performed by using the HP4192A impedance analyzer at 500 kHz and at a temperature between 230 K and 340 K.

RESULT AND DISCUSSION

The XRD characterization showed that peak broadening in CdS powder was ascribed to the formation of nanostructure which has no amorphous phase formed in milling conditions. The XRD image of CdS nanopowder prepared by the ball milling method is given in Fig. 1. The mean crystallite size of the CdS nanoparticles was calculated using the Debye–Scherrer's formula:

$$D = 0.94\,\lambda/\beta\cos\theta. \quad (1)$$

Here, D is the mean crystallite size, β is the full-width at half maxima of the prominent peak and other quantities are already well known in the literature.[17] The crystallite size of the sample was estimated below 30 nm. The morphology of the products was examined by SEM, for which the records are shown in Fig. 2. An overview of images for CdS nanoparticles showed that the product consists of nearly monodispersed spherical agglomerates of about 20-80 nm in diameter which aggregate in the form of big polydispersive clusters.

The C–V–T and G/ω–V–T characteristics in the temperature range of 230–340 K at 500 kHz are shown in Fig. 3a and b, respectively. It is obviously seen from Fig. 3a and b that both characteristics of C and G/ω increase with increasing temperature, particularly in the depletion region. The semi-logarithmic I–V plot of the device is also indicated in the inset of Fig. 3a and the main electrical parameters such as reverse saturation current (I_0), ideality factor (n), barrier height (Φ_{B0}), series

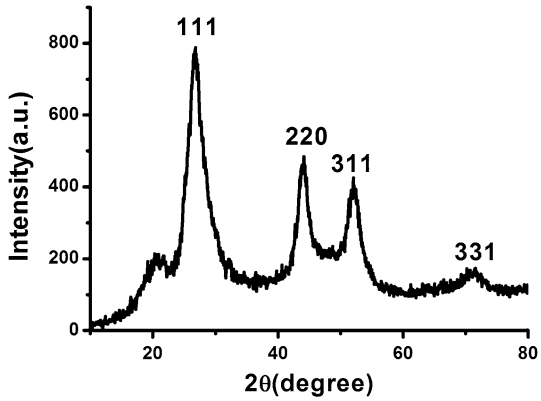

Fig. 1. XRD pattern of CdS nanopowder prepared by the ball milling method.

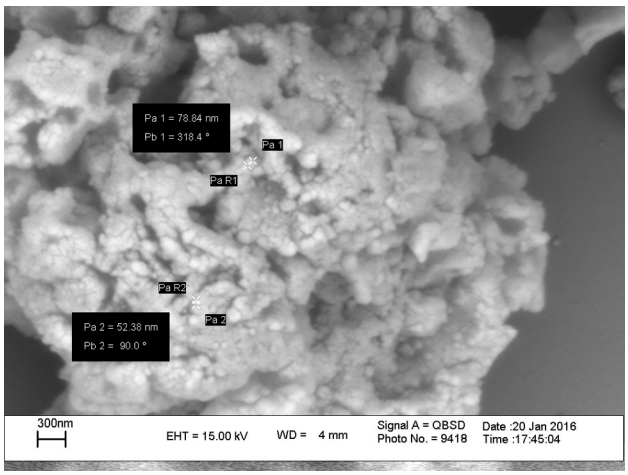

Fig. 2. SEM image of CdS sample prepared by the ball milling method.

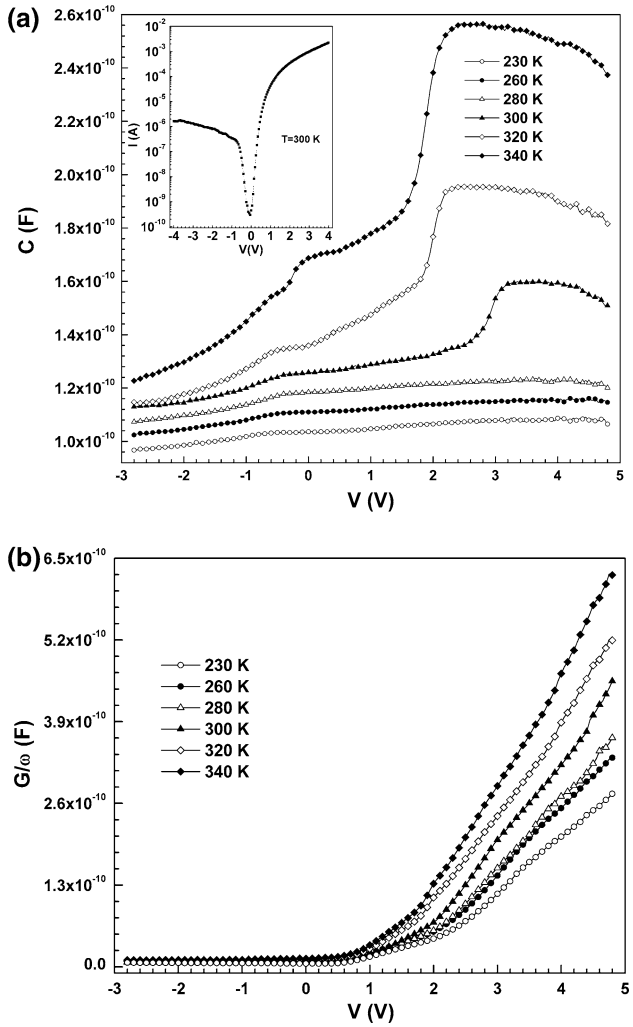

Fig. 3. Temperature-dependent plots of the (a) *C*–*V* and (b) *G*/ω–*V* characteristics at 500 kHz for Al/(CdS-PVA)/p-Si structure. The inset in (a) is the plot of the semi logarithmic *I*–*V* characteristic of the structures at 300 K.

resistance (R_s), shunt resistance (R_{sh}), and rectifier rate (RR) of the semi-logarithmic *I*–*V* plot of device were calculated in the inset of Fig. 3a. The obtained values are also given in Table I. As it can be clearly seen from Fig. 3b, there is an increase in the G/ω depending on temperature. This increase may stem from activated charge carrier mobility with temperature in the interfacial layer. The cause of this behavior may also be ascribed to the distribution in interfacial layer of the space charge.[35,36] Aside from that, the characteristics in the Fig. 3a indicate a concave peak in the accumulation region at temperatures that are higher than room temperature. The positions of the concave peak varied under the effect of temperature and voltage. In other words, peak positions shift towards lower voltage with increasing temperature owing to restructuring and reordering of charges that occur in traps with influence of temperature under the electric field. This peak of *C*–*V*–*T* can be ascribed to the presence of R_s and CdS-PVA at the interface and their inhomogeneities.

The real R_s of MPS structures can be extracted from the measured capacitance and conductance in the powerful accumulation region at 500 kHz with the following equation[37–39]:

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2}. \quad (2)$$

Here, C_m and G_m represent measured values of C and G at various bias voltages. R_s characteristics calculated by using Eq. 2 are given in Fig. 4 as a function of voltage for various temperatures.

Figure 4 shows that values of R_s decrease as temperature increases. At high temperatures, the trap charges have adequate energy to get rid of traps situated between the metal and semiconductor interface.[40] Figure 4 clearly reveals that R_s gives a peak in the voltage range of 2.0–3.0 V for 230 K, 260 K, 280 K and 300 K. On the other hand, it gives two peaks in the voltage ranges of 1.0–2.0 V (the

Table I. Main electrical parameters of Al/(CdS-PVA)/p-Si structure

I_0 (A)	n	Φ_{B0} (eV)	R_s (Ω)	R_{sh} (Ω)	RR
3.66×10^{-10}	1.93	0.885	1.78×10^3	2.44×10^6	1.37×10^3

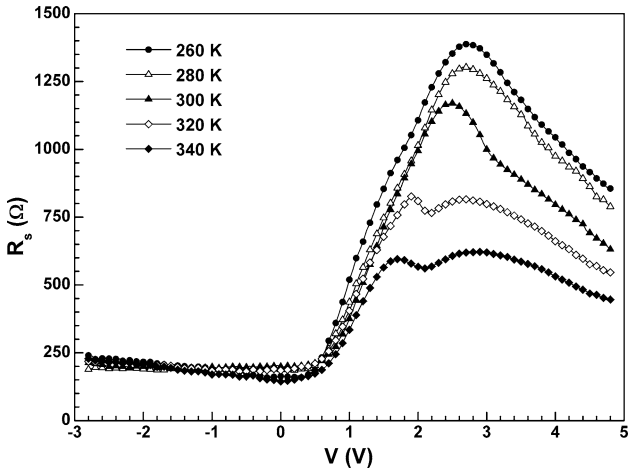

Fig. 4. Voltage dependent of R_s for Al/(CdS-PVA)/p-Si structure.

first peak) and 2.5–3 V (the second peak) for 320 K and 340 K, respectively. The peak observation in R_s versus V curve can be attributed to the existence of N_{ss} and their reordering and restructuring under the effect of an electric field.[21,33,37] The values of ε', ε'', tan δ, and σ_{ac} as a function of temperature were calculated from the experimental C_m and G_m data by using the following formulas, respectively[33,37]:

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \mathrm{Cd}/A\varepsilon_o - j\,(\mathrm{Gd}/\omega A\varepsilon_o), \quad (3)$$

$$\tan\delta = \varepsilon''/\varepsilon', \quad (4)$$

$$\sigma_{ac} = \omega C \tan\delta(d/A) = \varepsilon''\omega\varepsilon_o. \quad (5)$$

Here A, d, ε_o(= 8.85 × 10^{-12} F/m), j and ω (= $2\pi f$) represent the contact area, interfacial layer thickness, permittivity of free space, and the angular frequency, respectively.

The temperature response of ε', ε'', and tan δ at 500 kHz for MPS structure are shown in Fig. 5a, b, and c, respectively. As shown in these figures, both the values of ε' and ε'' increase with the increasing temperature and bias voltage. The increase of temperature and voltage leads to the form of defects in the periodic lattice and mobility of the majority charge carrier increases. The basic causes of rise in the values of ε' and ε'' may be both the ion jump and the orientation besides the changing concentrations of the charge carriers. Moreover, the increase in temperature triggers a widening of molecules which give rise to slight increase in the electric dipole polarization.[41] The values of ε'' give a peak at about 320 K for 2.0 V and 2.5 V, while the values of tan δ (Fig. 5c) give a peak about 300 K for 2.5 V, and the peak shifts toward high temperatures and disappears for lower applied voltages.[33,42] The variation in the values of ε', ε'' and tan δ emerging with temperature variations can be ascribed to the space charge polarization, surface states and dislocations in Si band-gap and electric field.[43]

Figure 6 indicates the temperature response of the σ_{ac} for Al/(CdS-PVA)/p-Si (MPS) type structure at 500 kHz. It is clear that the variation of σ_{ac} depending on temperature shows almost an exponential increase. The exponential increase of σ_{ac} stems from the decrease in R_s as temperature increases. In other words, charges in the interfacial layer gains thermal energy with increasing temperature. These results are compatible with the literature.[33,44] According to the literature,[45–49] the increase in the σ_{ac} at high temperatures is the due to defects of structure, which reside at the grain boundaries. These defects stretch out to the bottom of the conduction band (E_c) in the semiconductor; hence, they have small E_a. Once the electrical conduction in the structure is thermally activated, the temperature response of the σ_{ac} can be defined with the following formula[44]:

$$\sigma_{ac} = \sigma_0 \exp\left(\frac{-qE_a}{kT}\right). \quad (6)$$

Here, σ_0, k, and q embody electrical conductivity at endless temperature, the Boltzmann constant, and the electronic charge.[33]

Arrhenius plot (Ln(σ_{ac})–q/kT) of the ac conductivity at 500 kHz is shown in Fig. 7. The activation energy (E_a) value was obtained as 0.0601 eV from the slope of σ_{ac} versus q/kT.[49] The obtained activation energy value is at a low level. The reason for a low E_a value is the re-emergence of recombination causing more and more separations from thermionic-emission behavior increasing temperature. It is additionally stated here that the bulk-trap level reaches out above the internal Fermi energy level (E_F) and walks up to the E_c band border.[50]

Figure 8a and b demonstrate the M' and the imaginary M'' versus the temperature response for MPS structure at 500 kHz. According to the literature, complex electric modulus (M^*) formalism of MPS structures are inferred from dielectric properties of structures.[33,51,52] Hence, the complex permittivity ($\varepsilon^* = 1/M^*$) relation is turned into the M^* relation using the following formula:

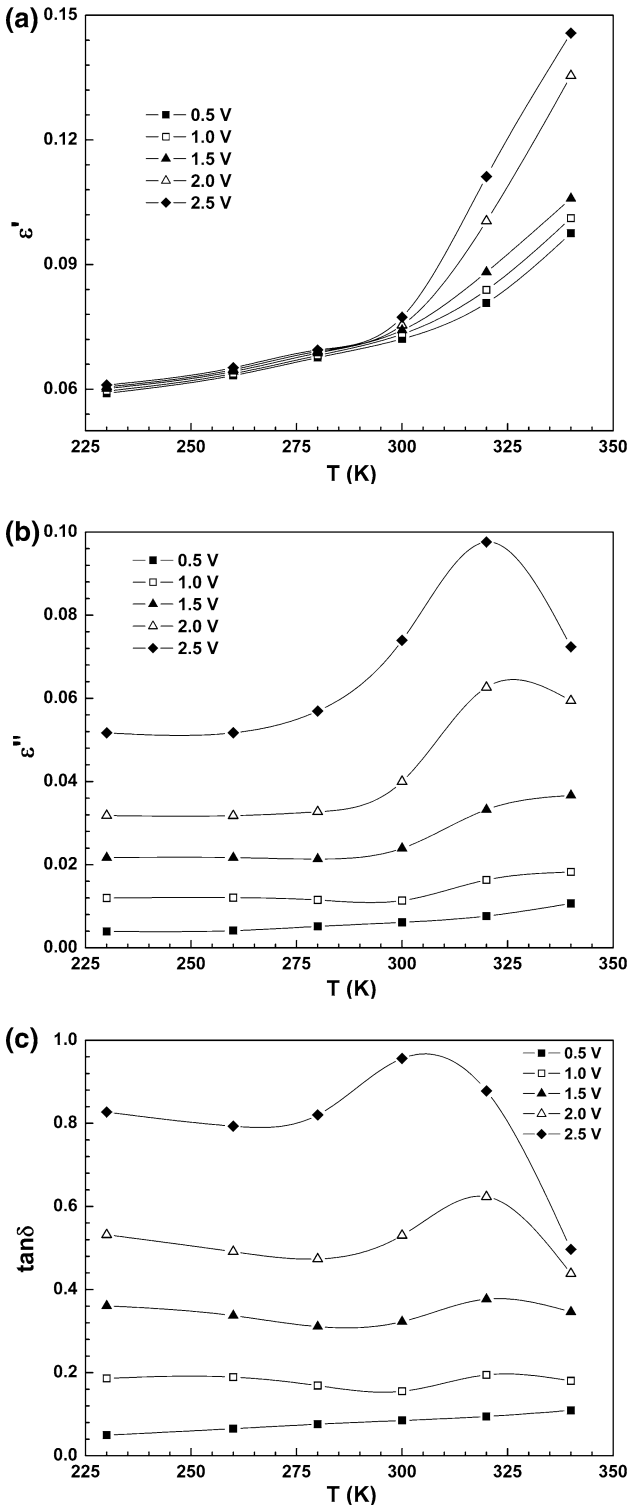

Fig. 5. Temperature dependence of the (a) ε', (b) ε'', and (c) tan δ for Al/(CdS-PVA)/p-Si structure at 500 kHz.

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2}. \quad (7)$$

It is clearly observed that the values of the M' decrease with increasing temperature and voltage.

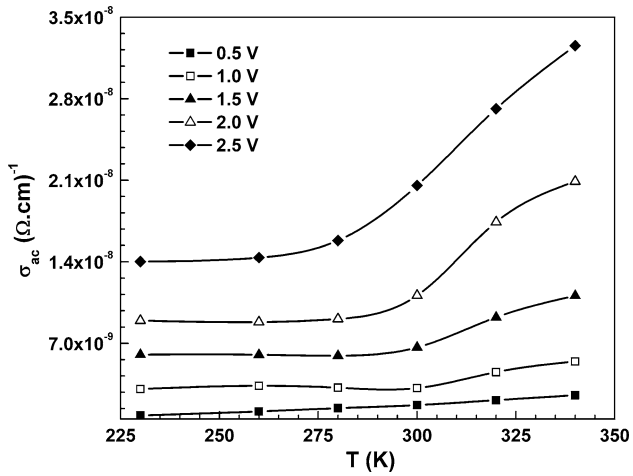

Fig. 6. Temperature dependence of σ_{ac} for Al/(CdS-PVA)/p-Si structure at 500 kHz.

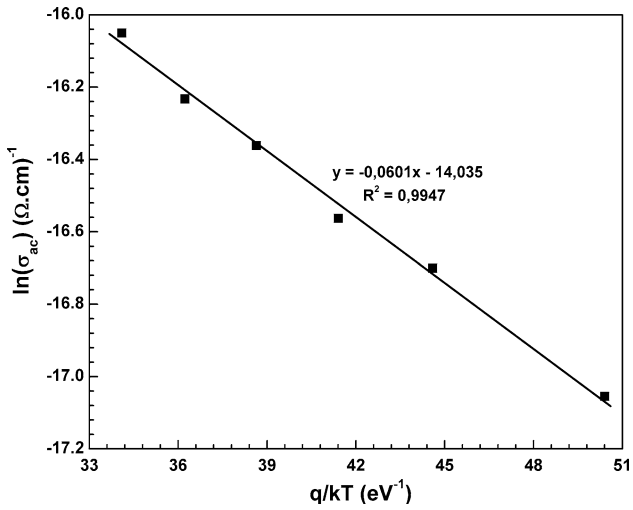

Fig. 7. Arrhenius plot (Ln(σ_{ac})–q/kT) at 500 kHz for Al/(CdS-PVA)/p-Si structure.

However, the values of the M'' decrease with increasing temperature, whereas its values increase with increasing voltage. Particularly the imaginary part of the electric modulus has become nearly temperature independent at 0.5 V. These results are compatible with the literature.[33,51,52]

The variation of M'' versus M' plots for the Al/(CdS-PVA)/p-Si structure is shown in Fig. 9. Argand diagrams of the complex modulus have the singular relaxation process at 230–280 K owing to one semicircle, while these diagrams have a double relaxation process at 300–340 K owing to a double semicircle. The double semicircle at the 300–340 K indicates more than one relaxation mechanism included in the Argand diagrams. This behavior of complex modulus resembles what is known as the Cole–Cole diagrams plotted for complex permittivity.[53] The origin of relaxation process can be ascribed to the surface and dipole polarization

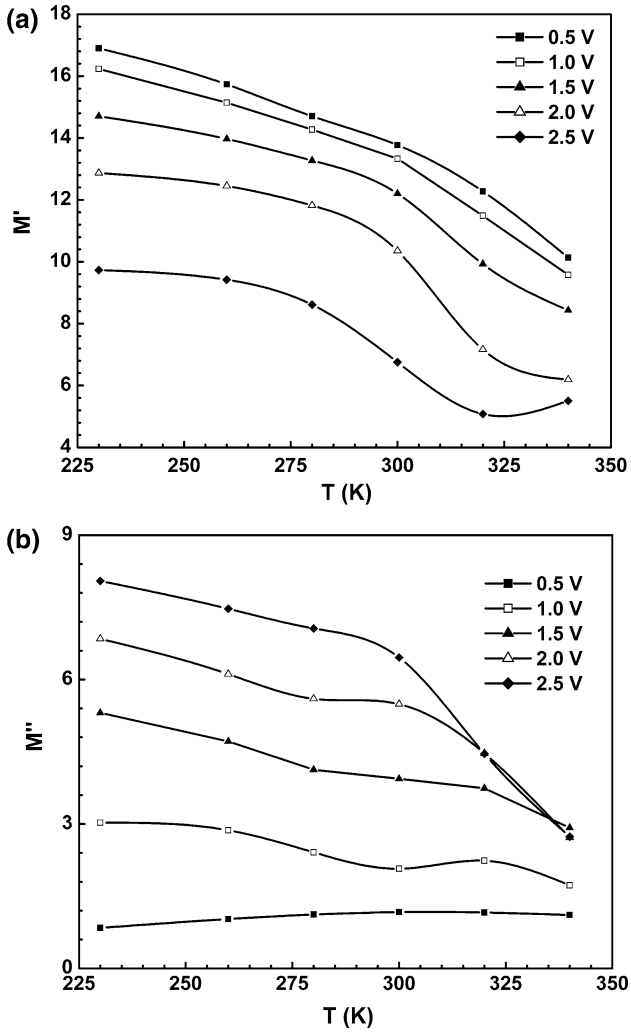

Fig. 8. The real and imaginary parts of electric modulus M' (a) and M'' (b) versus temperature for Al/(CdS-PVA)/p-Si structure at 500 kHz.

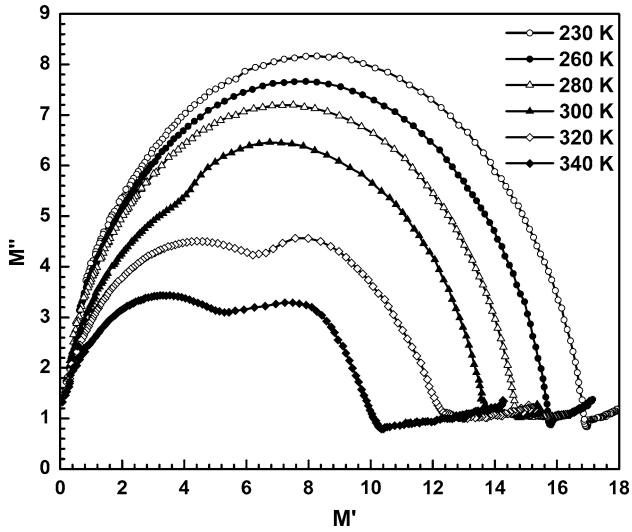

Fig. 9. Argand diagrams of electric modulus of the Al/(CdS-PVA)/p-Si structure in the temperature range of 230–340 K.

effects. The appearance of a double semicircle can also be evidence for the absence of co-contribution from the grain effect in the grain boundary.[54] These diagrams exhibit more of a semicircle as temperature increases because of the fact that the relaxation process for the Al/(CdS-PVA)/p-Si structures is better activated at room and higher temperatures than low temperatures, where a hopping process of charge carriers is predominant.[55,56] More recently, similar results have been observed in the literature.[57,58]

CONCLUSION

In the present study, firstly, CdS nano-powders were prepared by the physical ball milling method. The morphology of the sample was characterized by SEM. After that, we investigated the impedance spectra at the temperature range of 230–340 K and applied bias voltage range of (– 3 V) to (+ 5 V) at 500 kHz frequency to determine the effects of voltage, temperature and interfacial layer on the electrical and dielectric properties of the Al/(CdS-PVA)/p-Si (MPS) type structures. The electrical and dielectric properties of the prepared sample such as the ε', ε'', tan δ, M', M'', R_s and σ_{ac} were found to be as strong functions of voltage and temperature. In the depletion region, both the values of C and G/ω increase with increasing temperature. The values of capacitance start to increase rapidly in a forward bias region range of 1.5–3.0 V especially at room temperature and higher temperatures. This kind of characteristic is mostly ascribed to the molecular restructuring and reordering of the interface states and R_s. In addition, the σ_{ac} increases as voltage and temperature increase. These increases in σ_{ac} with increasing temperature were ascribed to the absence of sufficiently free charge carriers at low temperatures. The R_s decreases as voltage increases, while it increases with increasing temperature in the depletion region. The voltage and temperature dependences of R_s were ascribed to the particular distribution of interface states and interfacial layer. The results also indicate that the values of ε', ε'' and tan δ increase with increasing temperature and voltage. The basic causes of rise in the values of ε' and ε'' may be both the ion jump and the orientation besides the changing concentrations of the charge carriers. Moreover, the variation of the ε', ε'' and tan δ depending on temperature can stem from space charge polarization caused by impurities or defects at the metal/polymer interfacial layer. The values of E_a was obtained from the slope of $\ln\sigma_{ac}$ versus q/kT graph and calculated as 0.0601 eV for 230–340 K at 500 kHz. The M' decreases as temperature and voltage increase. Yet, the M'' decreases with increasing temperature, while it increases with increasing voltage. These variations with voltage and temperature in the electric modulus can stem from the space charge polarization

caused by impurities or interstitials in the structure. Finally, the relaxation behaviors were examined by considering modulus formalism. For the Al/(CdS-PVA)/p-Si (MPS) type structures, the double relaxation process, which is related to grains and grain boundaries, and hopping processes were demonstrated between the temperatures of 300–340 K. On the other hand, it was observed that only one relaxation process was in the range of 230–280 K. Both cases have different conductivity processes due to grain and grain boundary, since the grain has a higher conductivity than grain boundaries. On the other hand, grain boundaries have high resistance at the edges, at which charge carriers are collected.

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REFERENCES

1. P.K. Khanna and N. Singh, *J. Lumin.* 127, 474 (2007).
2. A. Dey, S. De, A. De, and S.K. De, *Nanotechnology* 15, 1277 (2004).
3. W. Cai, X. Gong, and Y. Cao, *Sol. Energy Mater. Sol. C* 94, 114 (2010).
4. A. Demir, S. Bağcı, S.E. San, and Z. Doğruyol, *Surf. Rev. Lett.* 22, 1550038 (2015).
5. A. Demir, A. Atahan, S. Bağcı, M. Aslan, and M.S. Islam, *Philos. Mag.* 96, 274 (2016).
6. S.K. Mishra, R.K. Srivastava, S.G. Prakash, R.S. Yadav, and A.C. Panday, *J. Alloys Compd.* 513, 118 (2012).
7. R.R. Navan, B. Panigrahy, M.S. Baghini, D. Bahadur, and V.R. Rao, *Compos. Part B Eng.* 43, 1645 (2012).
8. S.L. Hake, P.A. Chate, D.J. Sathe, P.P. Hankare, and V.M. Bhuse, *J. Mater. Sci. Mater. Electron.* 25, 811 (2014).
9. E. Maier, A. Fischereder, W. Haas, G. Mauthner, J. Albering, T. Rath, F. Hofer, E.J.W. List, and G. Trimmel, *Thin Solid Films* 519, 4201 (2011).
10. T.P. Nguyen, *Surf. Coat. Technol.* 206, 742 (2011).
11. Z. Han, J. Zhang, X. Yang, and W. Cao, *Sol. Energy Mater. Sol. C* 95, 483 (2011).
12. Y. Azizian-Kalandaragh, F. Sedaghatdoust-Bodagh, E. Alizadeh-Gheshlaghi, and A. Khodayari, *J. Nanoelectron. Optoelectron.* 12, 231 (2017).
13. P. Eskandari, F. Kazemi, and Y. Azizian-Kalandaragh, *Sep. Purif. Technol.* 120, 180 (2013).
14. Y. Azizian-Kalandaragh, U. Aydemir, and S. Altindal, *J. Electron. Mater.* 43, 4 (2014).
15. Y. Azizian-Kalandaragh, *Optoelectron. Adv. Mater. Rapid Commun.* 4, 1655 (2010).
16. D. Rezaei-Ochbelagh, Y. Azizian-Kalandaragh, and A. Khodayari, *Optoelectron. Adv. Mater. Rapid Commun.* 4, 881 (2010).
17. Y. Azizian Kalandaragh, M.B. Muradov, R.K. Mamedov, and A. Khodayari, *J. Cryst. Growth* 305, 175 (2007).
18. Y.A. Kalandaragh, M.B. Muradov, R.K. Mamedov, M. Behboudnia, and A. Khodayari, *Adv. Mater. Rapid Commun.* 2, 42 (2008).
19. V. Singh, P.K. Sharma, and P. Chauhan, *Mater. Charact.* 62, 43 (2011).
20. K. Susa, T. Kobayashi, and S. Taniguchi, *J. Solid State Chem.* 33, 197 (1980).
21. A. Kaya, İ. Yücedağ, H. Tecimer, and Ş. Altındal, *Mater. Sci. Semicond. Proc.* 28, 26 (2014).
22. H. Wang, P. Fang, Z. Chen, and S. Wang, *Appl. Surf. Sci.* 253, 8495 (2007).
23. S.R. Forrest, *Org. Electron.* 4, 45 (2003).
24. P.L. Burn, S.C. Lo, and I.D.W. Samuel, *Adv. Mater.* 19, 1675 (2007).
25. İ. Yücedağ, A. Kaya, and Ş. Altındal, *Int. J. Mod. Phys. B* 28, 1450153 (2014).
26. H. Tecimer, H. Uslu, Z.A. Alahmed, F. Yakuphanoğlu, and Ş. Altındal, *Compos. Part B Eng.* 57, 25 (2014).
27. İ. Yücedağ, G. Ersöz, A. Gümüş, and Ş. Altındal, *Int. J. Mod. Phys. B* 29, 1550075 (2015).
28. T. Tunç, Ş. Altındal, İ. Dökme, and H. Uslu, *J. Electron. Mater.* 40, 157 (2011).
29. V.R. Reddy, *Thin Solid Films* 556, 300 (2014).
30. S.M. Sze, *Physics of Semiconductor Devices* (New York: Wiley, 1981).
31. E.H. Rhoderick and R.H. Williams, *Metal–Semiconductor Contacts* (Oxford: Clarendon Press, 1988).
32. J.H. Werner and H.H. Güttler, *J. Appl. Phys.* 69, 1522 (1991).
33. A. Gümüş, G. Ersöz, İ. Yücedağ, S. Bayrakdar, and Ş. Altındal, *J. Korean Phys. Soc.* 67, 889 (2015).
34. Ç. Bilkan, S. Zeyrek, S.E. San, and Ş. Altındal, *Mater. Sci. Semicond. Proc.* 32, 137 (2015).
35. G. Ersöz, İ. Yücedağ, Y. Azizian-Kalandaragh, İ. Orak, and Ş. Altındal, *IEEE Trans. Electron. Dev.* 63, 2948 (2016).
36. İ. Dökme and Ş. Altındal, *IEEE Trans. Electron. Dev.* 58, 4042 (2011).
37. Ş. Altındal, İ. Yücedağ, and A. Tataroğlu, *Vacuum* 84, 363 (2009).
38. N. Baraz, İ. Yücedağ, Y. Azizian-Kalandaragh, and Ş. Altındal, *J. Mater. Sci. Mater. Electron.* 28, 1315 (2017).
39. İ. Yücedağ, *Optoelectron. Adv. Mater. Rapid Commun.* 3, 612 (2009).
40. B. Kınacı and S. Özçelik, *J. Electron. Mater.* 42, 1108 (2013).
41. D. Maurya, J. Kumar, and Shripal, *J. Phys. Chem. Solids* 66, 1614 (2005).
42. İ. Yücedağ, A. Kaya, H. Tecimer, and Ş. Altındal, *Mater. Sci. Semicond. Proc.* 28, 37 (2014).
43. M.R.R. Raju, R.N.P. Choudhary, and S. Ram, *Phys. Status Solidi B* 239, 480 (2003).
44. S.A. Awan and R.D. Gould, *Thin Solid Films* 423, 267 (2003).
45. C.V. Kannan, S. Ganesamoorthy, C. Subramanian, and P. Ramasamy, *Phys. Status Solidi A* 196, 465 (2003).
46. K.S. Moon, H.D. Choi, A.K. Lee, K.Y. Cho, H.G. Yoon, and K.S. Suh, *J. Appl. Polym. Sci.* 77, 1294 (2000).
47. A. Tataroğlu, Ş. Altındal, and M.M. Bülbül, *Microelectron. Eng.* 81, 140 (2005).
48. S. Maity, D. Bhattacharya, and S.K. Ray, *J. Phys. D Appl. Phys.* 44, 095403 (2011).
49. A. Tataroğlu, *Microelectron. Eng.* 83, 2551 (2006).
50. M.O. Aboelfotoh, A. Cros, B.G. Svensson, and K.N. Tu, *Phys. Rev. B* 41, 9819 (1990).
51. P. Pissis and A. Kyritsis, *Solid State Ionics* 97, 105 (1997).
52. K. Prabakar, S.K. Narayandass, and D. Mangalaraj, *Phys. Status Solidi A* 199, 507 (2003).
53. E. Barsoukov and J.R. Macdonald, *Impedance Spectroscopy* (Hoboken: Wiley, 2005).
54. Y.Ş. Asar, T. Asar, Ş. Altındal, and S. Özçelik, *Philos. Mag.* 95, 2885 (2015).
55. I.M. Hodge, K.L. Ngai, and C.T. Moynihan, *J. Non-Cryst. Solids* 351, 104 (2005).
56. K.S. Cole and R.H. Cole, *J. Chem. Phys.* 9, 3411 (1941).
57. A. Kaya, S. Alialy, S. Demirezen, M. Balbaşı, S.A. Yerişkin, and A. Aytimur, *Ceram. Int.* 42, 3322 (2016).
58. S.A. Yerişkin, M. Balbaşı, and A. Tataroğlu, *J. Appl. Polym. Sci.* 133, 43827 (2016).