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Effect of Macro-scale Mechanical Stress of Silicon Wafer on Room Temperature Photoluminescence Signals

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Mechanical stress was applied to single side polished and double side polished Si wafers in polypropylene wafer containers for different localized stress levels and durations. Room temperature photoluminescence (RTPL) spectra from Si wafers were measured before and after applying localized mechanical stress. Significant changes (up to 26% increase) in RTPL intensity were measured from areas under different stress levels even 1 year after the fixtures for mechanical stress generation were removed. Significant effects of localized mechanical stress on RTPL intensity variations were measured up to 49 days after the fixture removal. Nearly fully relaxed RTPL signatures for localized mechanical stress were measured 450 days after the fixture removal. RTPL intensity is found to be very sensitive to the externally applied macro-scale mechanical stress of Si wafers and residual (or memorized) internal stress even after removal of fixtures for external mechanical stress generation.

Key words: Silicon, mechanical stress, room temperature photoluminescence, stress relaxation

INTRODUCTION

Micro- and nano-scale localized stress in Si can modify electrical properties such as carrier mobility and bandgap.[1,2] To enhance electron mobility in n-type metal–oxide–semiconductor (NMOS) and hole mobility in *p*-type metal–oxide–semiconductor (PMOS) transistors, uniaxial tensile and compressive strain along channels are generated by either introducing a capping layer or introduction of strain generating materials along the channel region.[2] Strain engineered devices have been widely used for about a decade.[3] However, the effect of macro- or global-scale mechanical stress on electronic properties of Si did not receive great attention. Understanding the effect of macro- or global mechanical stress and its relaxation behaviors can provide meaningful insight into device reliability and packaging-related device performance variations and degradation over time.

In this study, we have studied the effect of macro-scale mechanical stress of Si wafers on their room temperature photoluminescence (RTPL) signal which indicates the electronic state of Si under mechanical stress. The effect of stress relaxation on the RTPL signal intensity was monitored up to 450 days.

EXPERIMENTAL

Fifteen (15) assorted Si wafers with 50 mm diameter with orientation flats were prepared. The wafers were single-side polished (SSP) and have a thickness of ~ 300 μm. Ten (10) assorted double-side polished (DSP) Si wafers with similar thickness were also prepared. Both p-type and n-type Si wafers with a resistivity range of 1–100 Ω cm were used in this study. Starting wafers were placed in containers as seen in Fig. 1a. Wafers are free standing and no external mechanical stress is applied in the container. For localized mechanical stress generation, single wafer carrier containers made of polypropylene $(C_3H_6)_n$ were used. Localized mechanical stress was applied through a polypropylene spring with or without additional parts (1 mm-

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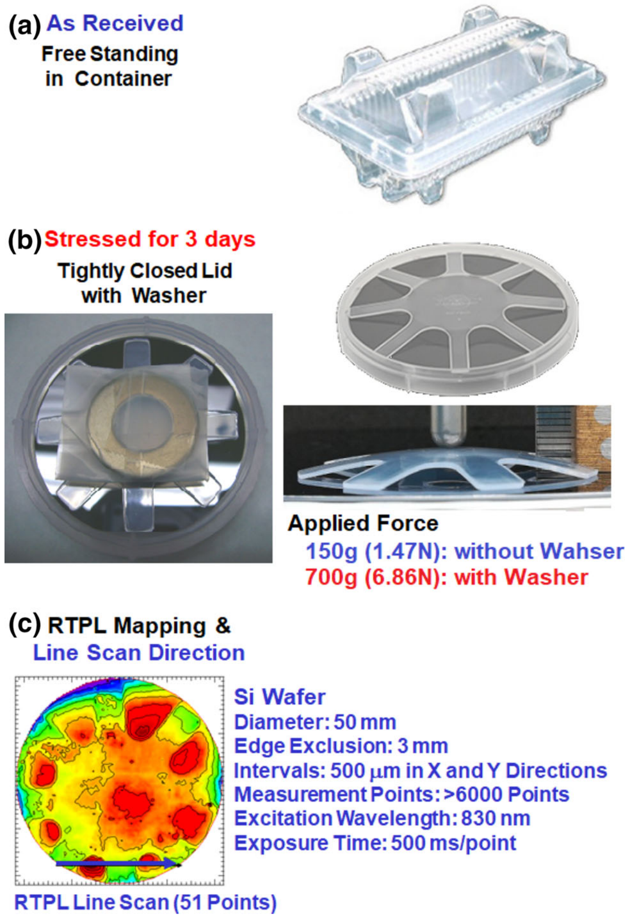

Fig. 1. (a) 50 mm diameter Si wafer container for as received wafer, (b) single wafer container with spring and washer for applying mechanical stress, and (c) details of RTPL wafer mapping and line scan conditions.

and 2 mm-thick stainless-steel washers) by tightly closing the container (Fig. 1b). The DSP Si wafer and polished side of the SSP Si wafer were either face up or face down to see the influence of polypropylene spring contact on RTPL intensity. Only one side of Si wafers made contact with the polypropylene spring in the container.

RTPL spectra in the wavelength range of 900–1400 nm were measured from the polished surface (contacting surface with the polypropylene spring) of either SSP or DSP Si wafers using a thermoelectrically (TE) cooled spectrograph system (WaferMasters MPL-300).[4–6] The RTPL system is designed for handling 200 mm and 300 mm diameter Si wafers. Thus, a special sample stage for adapting 50 mm diameter wafers was fabricated and placed on a 300 mm wafer stage. Two excitation wavelengths of 650 nm and 830 nm were used. The excitation laser power at the wafer surface was fixed at 20 mW for 650 nm and 50 mW for 830 nm. The exposure time for RTPL measurements was fixed at 500 ms per point. RTPL wafer mapping (> 6000 points) in 500 μm intervals in the X- and Y-directions with 3 mm edge exclusion was done for all wafers before and after applying localized mechanical stress (Fig. 1c). RTPL wafer mapping was periodically done after removing external mechanical stress. For easy comparisons, 51-point RTPL line scans were done in 500 μm intervals in the X-direction across the region of alternating mechanical stress. RTPL mapping and line scans were done periodically to monitor the change of RTPL intensity maps over time up to 450 days after removing stress generation fixtures.

To verify the possible effect of wafer bow, flatness and warpage on RTPL intensity maps, visual inspection of wafer edge flatness on flat surface and wafer bow measurements were performed. The wafer bow measurement was done using a FSM 128L system (Frontier Semiconductor, Milpitas, CA).

RESULTS AND DISCUSSION

RTPL mapping results under 650 nm and 830 nm excitation showed almost the same distribution over the wafer surface despite the difference in probing depth. The probing depth is excitation wavelength dependent due to the difference in absorption coefficient. Probing depths for 650 nm and 830 nm excitation are ~ 4.0 μm and ~ 10.0 μm, respectively.[4,5] RTPL spectra under 650 nm and 830 nm excitation are almost identical, other than the intensity. In general, the 830 nm excited RTPL signal was stronger and has a higher signal-to-noise (S/N) ratio due to its deeper probing depth (less sensitive to the surface condition of Si wafer) compared to 650 nm excitation measurements.[4–6]

As received Si wafers generally showed reasonably uniform RTPL intensity across the wafer except at a few mm from the wafer edge. When wafers were stored in a single wafer carrier container with polypropylene spring, all wafers (SSP and DSP Si wafers either face up or face down) are compressed against the bottom part of wafer carrier container under eight (8) fins of the spring to immobilize during transportation. If the container lid is closed tightly, the area and magnitude of localized external mechanical stress will increase accordingly. We have noticed the change of the RTPL intensity map from identical wafers taken directly from a 25 wafer container and single wafer carrier containers after a few days of storage, regardless of SSP or DSP Si wafers. The RTPL maps from Si wafers from single wafer carrier containers always showed polypropylene spring-shaped signature. Compressed areas showed weaker RTPL intensity. By increasing lid tightening force, the RTPL intensity variations became larger. Results were very consistent from other wafers as well. For demonstrating the effect of localized external mechanical stress on RTPL signal intensity from the bulk, rather than the surface of Si wafers, 830 nm excited RTPL wafer mapping and line scan results on a wafer are shown.

Figure 2 shows eight (8) fin marks and six (6) fin marks on RTPL intensity maps corresponding to the number and shapes of standard and modified polypropylene spring even without additional spacers (stainless washers). The wafers were double side polished (DSP) and stored in containers for 3 days. The edge of top surfaces was compressed by polypropylene springs, and the edge of bottom surfaces was forced against the concave polypropylene containers. We have measured RTPL intensity maps from both front side and backside of the DSP wafers to identify the effect of localized mechanical stress induced by polypropylene springs. RTPL intensity maps from the front side measurement clearly showed the trace of standard (8 fin) and modified (6 fin) springs. RTPL intensity maps measured from the backside showed almost perfect mirror image of RTPL intensity maps measured from the front side. The range of RTPL intensity from the front side was wider than that from the backside indicating strong correlation between RTPL intensity variation and polypropylene spring induced mechanical stress in containers during 3 days of storage. The RTPL intensity variations of Si wafer pressed by the standard 8 fin spring seemed to be larger than that for the modified 6 fin spring. It is due to the relative scale (minimum to maximum intensity) RTPL intensity mapping and the effect of RTPL intensity at the very top portion of the standard 8 fin configuration. The absolute RTPL intensity variations near the 51-point RTPL line scan region shown in Fig. 1c are almost the same.

The height of the free-standing propylene spring is 4 mm (Fig. 1b). When the lid of a single wafer carrier container is closed with the 300 μm-thick Si wafer, the spring is compressed against the Si wafer by about 1 mm, equivalent to 150 g (1.47 N). Additional 1 mm and 2 mm compression (2 mm and 3 mm compression in total) of the polypropylene spring against the Si wafer requires 350 g (3.43 N) and 750 g (7.35 N), respectively. The force for the polypropylene spring compression was measured to quantify mechanical stress against the Si wafer by tightening the lid of the single wafer carrier container. The uncertainty range of force measurement is approximately 50 g (0.49 N) or less.

To demonstrate the impact of localized mechanical stress on RTPL maps, we have placed a 2 mm-thick stainless-steel washer on top of the polypropylene spring and tightly closed the lid. This results in a total of 3 mm compression of the polypropylene spring and generates 750 g (7.35 N) of force against the 50 mm diameter Si wafer. Since the contact area between the polypropylene spring and Si wafer will vary with the degree of spring compression, accurate estimation of mechanical stress in g/cm^2 or N/cm^2 is not easy. The increase of total compression by adding stainless steel washers between the lid and polypropylene spring, the increase of external mechanical stress is expected.

Figure 3 shows the effect of external stress applied to a Si wafer on RTPL intensity; (a)

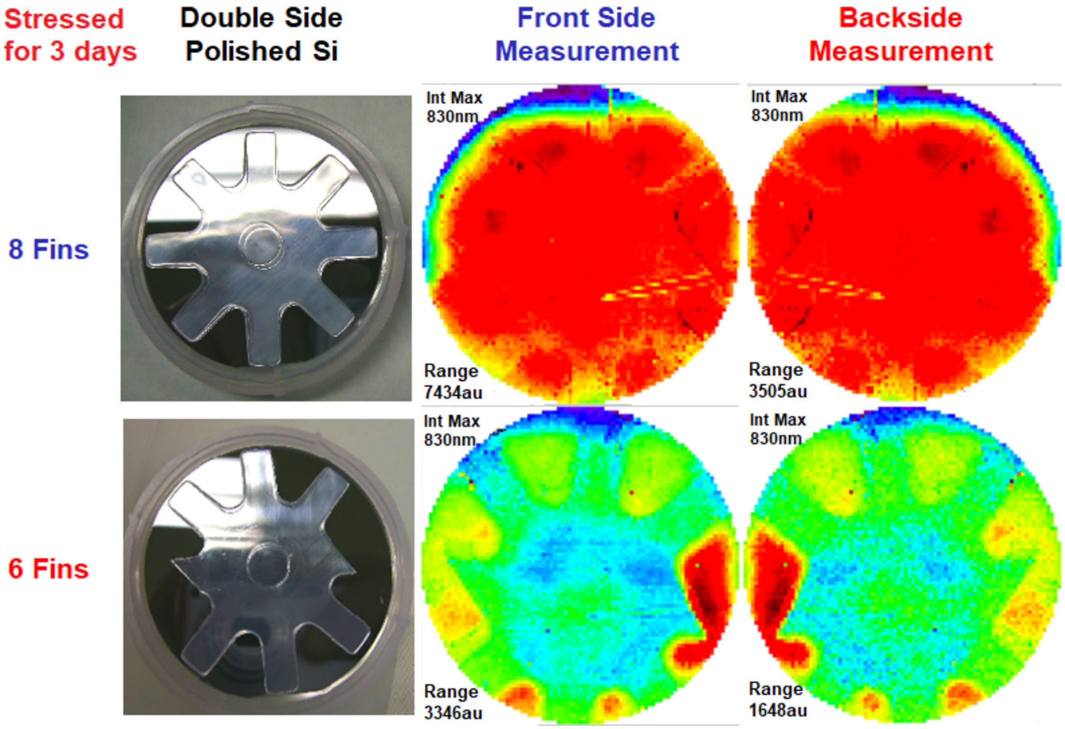

Fig. 2. The 830 nm excitation RTPL wafer mapping results from front side and backside of Si wafers stored in containers with standard (8-fin) spring and modified (6-fin) spring without additional washers for additional mechanical stress.

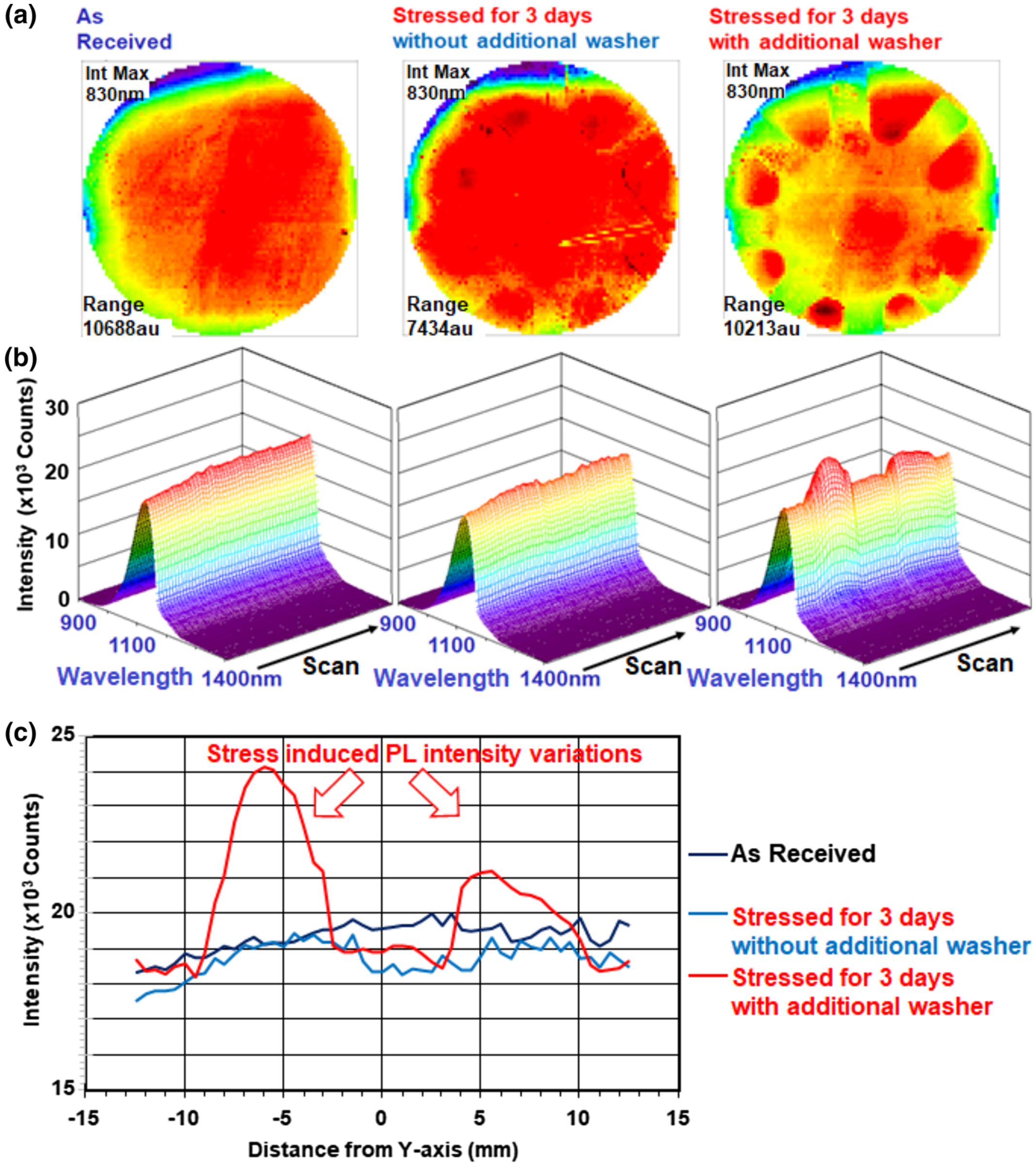

Fig. 3. (a) 830 nm excitation RTPL wafer mapping results, (b) 51-point RTPL spectra line scan measurement results and (c) 51-point RTPL intensity line scan measurement summary of as received and stressed Si wafers for 3 days in containers without and with an additional washer.

830 nm excitation RTPL wafer maps, (b) 51-point RTPL spectra line scan measurement results and (c) 51-point RTPL intensity line scan measurement summary of as received and stressed Si wafers for 3 days in containers without and with an additional washer. As received wafers showed fairly uniform RTPL intensity across the 51-point line scan region. The wafer stored for 3 days in a container with a standard 8 fin polypropylene spring showed slight increase in RTPL intensity where the surface was compressed. To verify the effect of external stress to a DSP Si wafer on RTPL intensity more clearly, we have measured a DSP Si wafer stored for 3 days in a container with a standard 8 fin polypropylene spring and a 2-mm thick, stainless steel washer (Fig. 1b). Significant increase of RTPL intensity was observed where the surface was compressed by the polypropylene spring with the additional washer. The magnitude of RTPL intensity increase seemed to be proportional to the external stress applied to the Si wafer (Fig. 3c).

To investigate the memory effect of external stress on Si wafers, time dependence of RTPL intensity wafer mapping and line scan measurements of intentionally stressed Si wafers were done after removing fixtures for external mechanical stress generation. Wafers became externally mechanical stress free before RTPL measurements. Figures 4–6 show the RTPL measurement results on a typical Si wafer. The wafer was stored in localized mechanically stressed condition (with an additional washer) for 3 days and measured RTPL

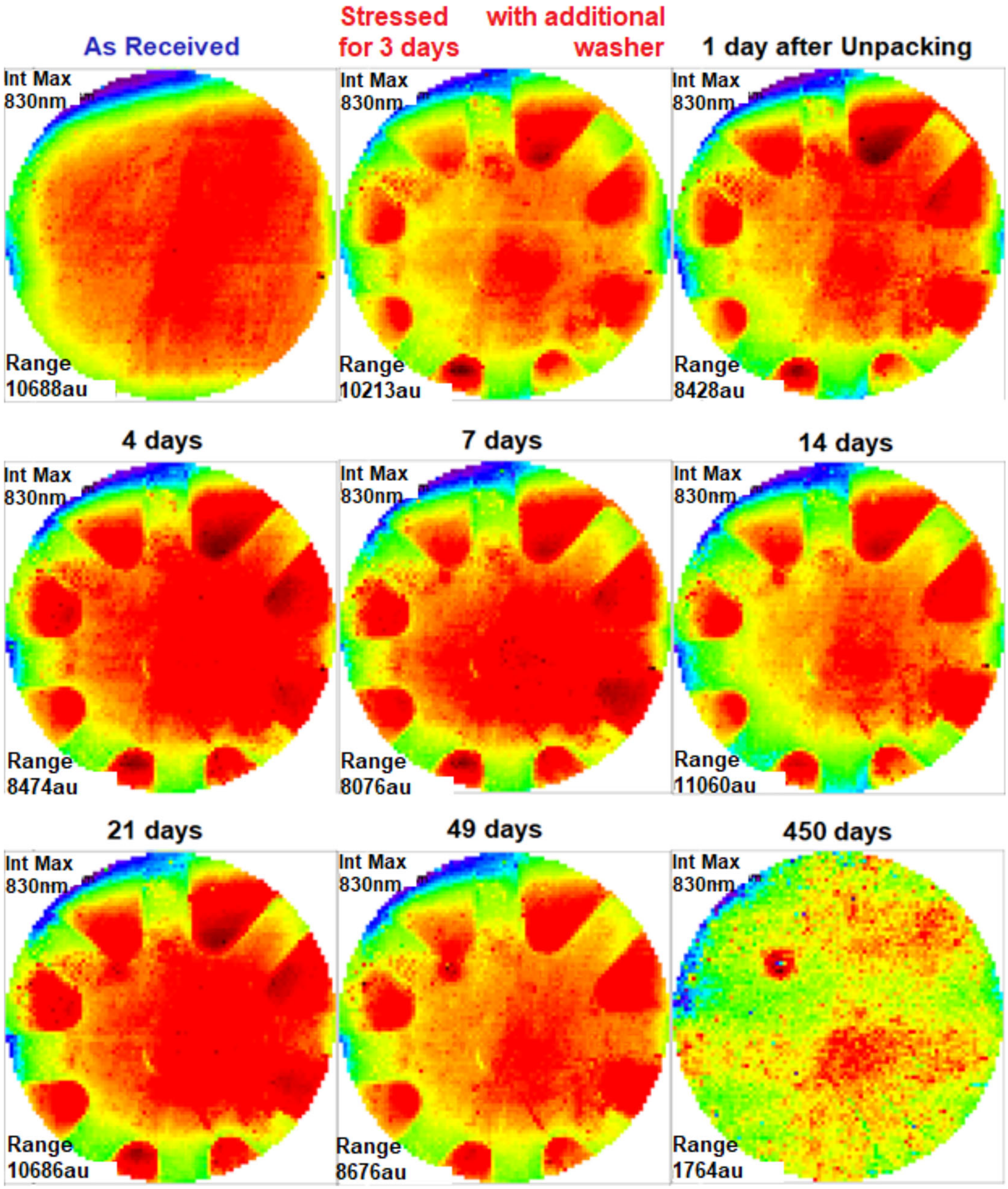

Fig. 4. The 830 nm excitation RTPL wafer mapping results from an identical Si wafer showing effect of mechanical stress on RTPL intensity variations and mechanical stress relaxation with time.

signal. The RTPL mapping and line scan measurements were done periodically up to 450 days without closing the lid again for monitoring mechanical stress relaxation over time (Figs. 4–6). No peculiar pattern on a RTPL wafer map was observed from the wafer in as received condition. After 3 days of storage in a single wafer carrier container under locally mechanically stressed condition, the polypropylene spring pattern of 8 fins appeared. The areas compressed by fins showed reduction of RTPL intensity. RTPL wafer maps showed very consistent patterns for up to 49 days. It appears the patterns may remain for even longer. After 450 days, RTPL intensity was decreased by a factor of 3 and most of the fin marks of the spring disappeared (Figs. 4–6).

From RTPL line scan measurement data, overall RTPL intensity increase was observed on the 14th day and 21st day after removal of the mechanical stress generation fixture. On the 49th day, RTPL intensity was decreased and returned to the intensity levels measured immediately after removal of the fixture. After 450 days, overall RTPL intensity was significantly reduced, by a factor of 3, and the "footprint" of the polypropylene spring used for mechanical stress generation was not very obvious. The overall decrease of RTPL intensity after 450 days may be due to possible organic

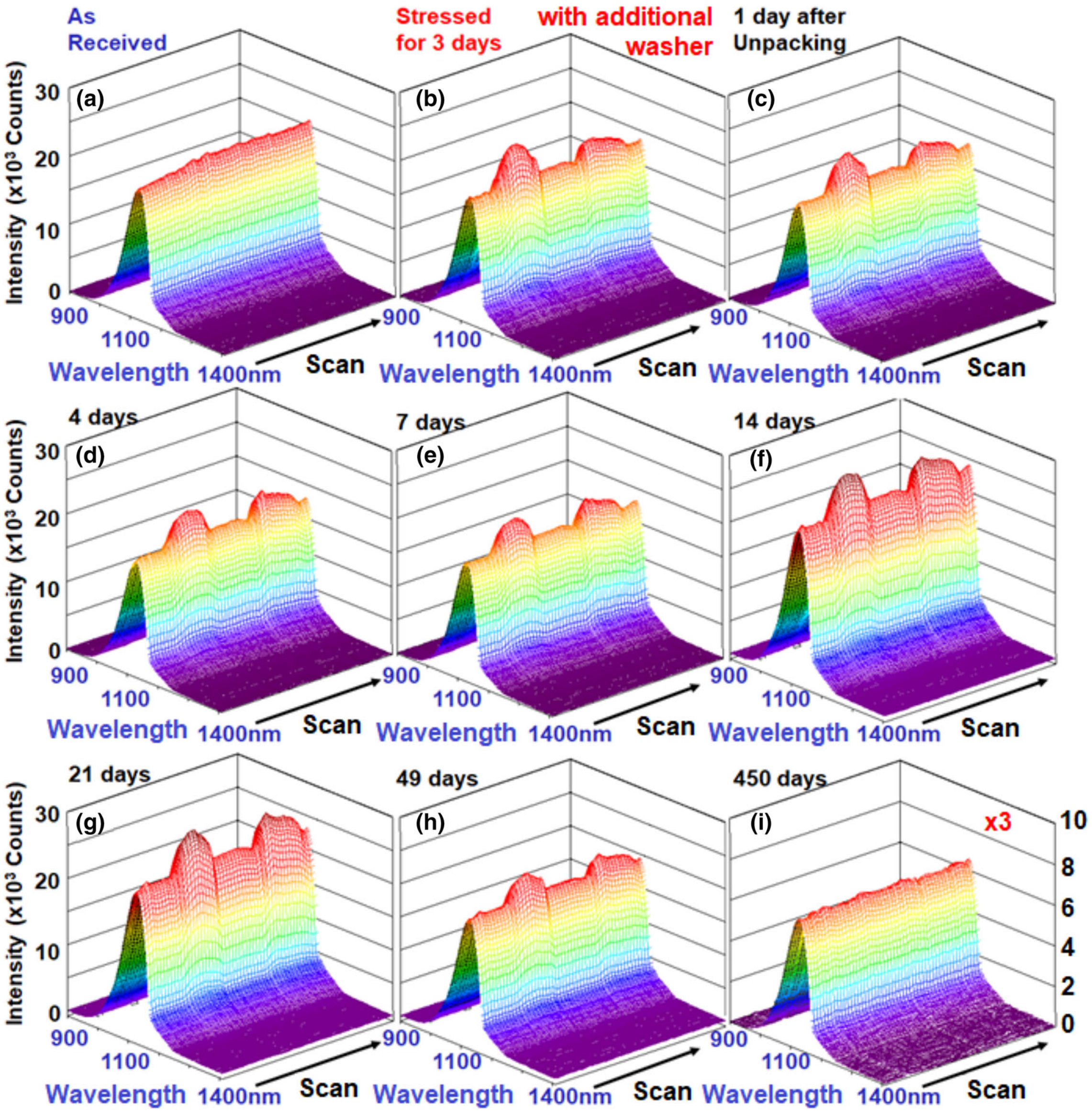

Fig. 5. The 830 nm excitation, 51-point RTPL spectra line scan measurement results from an identical Si wafer (see Fig. 1c for line scan location and direction).

contamination of the surface from the uncontrolled environment over a long period of time (450 days). When we carefully looked at the line scan spectra measured on the 450th day, however, slight variations in RTPL intensity were still noticeable near the fin boundaries. The localized mechanical stress was not completely relaxed even after 450 days of removing external stress. It was found that the Si wafer can “memorize” localized mechanical stress for a surprisingly long time from the RTPL measurements.

Performance and measurement repeatability of the RTPL measurement system was monitored daily using a reference Si wafer piece embedded in the wafer stage. The measurement repeatability over a two (2) year period was monitored. The range of RTPL intensity of the reference Si wafer piece was less than 0.5% of the average RTPL intensity. Since the RTPL measurement system was developed for in-line monitoring of Si wafers in advanced device volume production, the measurement system is very stable. Any intensity variation above 0.5% can be interpreted as variations in the Si properties. The 32.8% change of average RTPL intensity (18.9×10^3 counts on the seventh day to 25.1×10^3 counts on the 14th day) is due to the property change of the Si wafer. The average intensity of 24.6×10^3 counts on the 21st day also strongly suggests possible property changes of the Si between the 14th day and the 21st day.

Besides the RTPL intensity change, within wafer RTPL intensity uniformity (i.e., degree of variation within wafer) can indicate the effect of external mechanical stress induced by the polypropylene

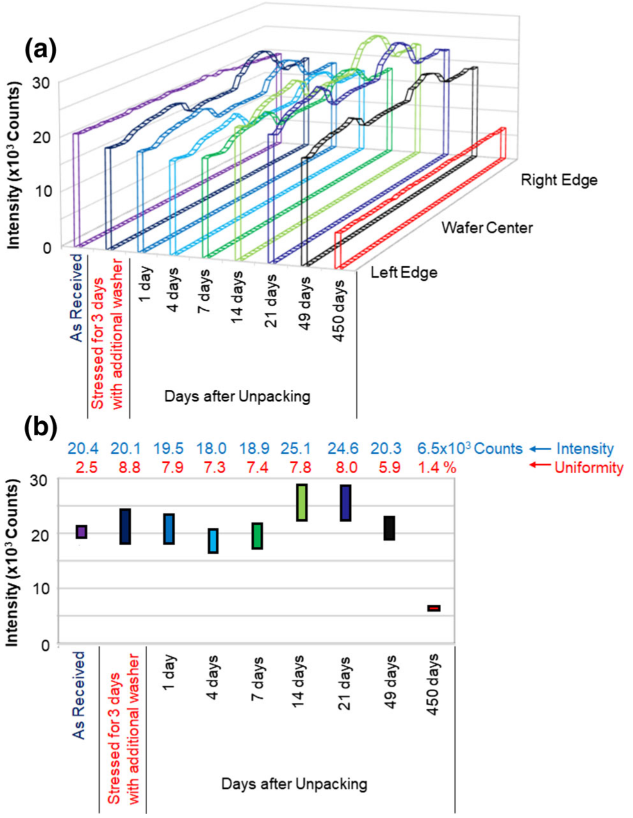

Fig. 6. (a) Changes in RTPL intensity line scan results (830 nm excitation, 51-point line scan) and (b) RTPL intensity variations of line scans (see Fig. 1c for line scan location and direction).

spring in the single wafer carrier container. The as-received wafer showed the RTPL intensity uniformity (standard deviation (1σ) of RTPL intensity over average RTPL intensity) of 2.5% worsened significantly (more than tripled) after being stressed in the single wafer carrier container and even after unpacking (Fig. 6b). On the 450th day after unpacking, the RTPL intensity uniformity decreased down to 1.4% (better than that of the as-received wafer) suggesting the mechanical stress originated RTPL intensity variations within the wafer had almost vanished.

To be sure, we have cut two (2) and four (4) out of eight (8) fins of the spring and repeated the experiment on other wafers. Only six (6) and four (4) fin marks were observed from those wafers. We also suspected the contamination of the Si surface from the polypropylene spring as another possibility. However, we did not see a similar spring fin pattern from wafers stored in a single wafer carrier container with a loosely closed lid. If the change of the RTPL wafer map is merely surface contamination related, recovery of uniformity of the RTPL wafer map after 450 days cannot be clearly explained. Stress relaxation after removing the external source of stress by opening the lid and removal of the polypropylene spring and the additional washer played an important role. Mechanical stress non-uniformity within wafer was responsible for the RTPL intensity non-uniformity. It was found that the RTPL technique is quite useful for detecting macro- or global-scale residual mechanical stress in Si.

We have visually inspected the possible Si wafer deformation and warpage by placing wafers on flat surfaces and observing the gap between Si wafers and the flat surface along the wafer edge. No visible gap was between Si wafers and the flat surface suggesting the potential wafer deformation by external mechanical stress through polypropylene spring compression was observed. Wafer bow was also measured using the FSM 128L system before and after applying mechanical stress to Si wafers. The wafers were nearly flat and almost no local bow or deformation was measured.

The force of polypropylene spring compression can provide external mechanical force to the Si wafer over the contacting area. However, the accurate measurement of contact area with the spring for external stress calculation is quite difficult. It was difficult to quantify mechanical stress generated by the polypropylene spring in a single wafer carrier container using only RTPL measurement data without a calibrated database. To determine the effect of external stress and relaxation over time, quantification of mechanical stress from wafer surface deformation measurement and/or Raman spectroscopy should be performed and compared with RTPL characterization results.[6] It will provide additional insights into the impact of macro- or global-scale residual mechanical stress in Si on electronic properties such as band bending, bandgap change and carrier mobility modification.[6–8]

SUMMARY

Effects of macro- or global-scale mechanical stress on RTPL intensity and spectra from Si wafers was investigated. For preparation of the experiment, SSP and DSP Si wafers were stored under different localized stress levels and durations in polypropylene single wafer carrier containers. RTPL spectra from Si wafers were periodically monitored for up to 450 days after the mechanical stress generation fixture was removed. Judging from RTPL wafer map signatures, it was determined that mechanical stress can be “memorized” in Si for an extended period of time and may affect electronic properties. RTPL intensity increases up to 26% were detected from stress memorization. The result emphasizes the importance of stress management in storing and packaging finished devices so as not to induce electronic property variations after device fabrication steps.[7,8]

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REFERENCES

1. N.P. Singh, *Phys. Status Solidi A* 1, 259 (1970).
2. Y. Song, H. Zhou, Q. Xu, J. Luo, H. Yin, J. Yan, and H. Zhong, *J. Electron. Mater.* 48, 1584 (2011).
3. P. Packan, S. Cea, H. Deshpande, T. Ghani, M. Giles, O. Golonzka, M. Hattendorf, R. Kotlyar, K. Kun, A. Murthy, P. Ranade, L. Shifren, C. Weber, and K. Zawadzki, *IEDM Conference Technical Digest* (San Francisco, CA, December 15–17, 2008), pp. 63–66. https://doi.org/10.1109/IEDM.2008.4796614.
4. W.S. Yoo, T. Ishigaki, and K. Kang, *ECS J. Sold State Sci. Technol.* 5, P3064 (2016).
5. W.S. Yoo, B.G. Kim, S.W. Jin, T. Ishigaki, and K. Kang, *ECS J. Solid State Sci. Technol.* 3, N142 (2014).
6. J.H. Kim, S.M. Han, and W.S. Yoo, *ECS J. Solid State Sci. Technol.* 5, P438 (2016).
7. X. Xu and V. Moroz, *Mater. Res. Soc. Symp. Proc.* 863, B8.25.1 (2005).
8. V. Sukharev, A. Kteyan, J.-H. Choy, H. Hovsepyan, A. Markosian, E. Zschech, and R. Huebner, in *AIP Conference Proceedings* (2012), p. 249.