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Hydrogenated Nano-/Micro-Crystalline Silicon Thin-Films for Thermoelectrics

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Thermoelectric technology has not yet been able to reach full-scale market penetration partly because most commercial materials employed are scarce/-costly, environmentally unfriendly and in addition provide low conversion efficiency. The necessity to tackle some of these hurdles leads us to investigate the suitability of n-type hydrogenated microcrystalline silicon (μc-Si: H) in the fabrication of thermoelectric devices, produced by plasma enhanced chemical vapour deposition (PECVD), which is a mature process of proven scalability. This study reports an approach to optimise the thermoelectric power factor (PF) by varying the dopant concentration by means of post-annealing without impacting film morphology, at least for temperatures below 550°C. Results show an improvement in PF of more than 80%, which is driven by a noticeable increase of carrier mobility and Seebeck coefficient in spite of a reduction in carrier concentration. A PF of 2.08×10^{-4} W/mK^2 at room temperature is reported for n-type films of 1 μm thickness, which is in line with the best values reported in recent literature for similar structures.

Key words: Thermoelectric, microcrystalline silicon, thin films, highly doped, annealing, power factor

INTRODUCTION

Nearly two thirds of worldwide primary energy is released into the atmosphere in the form of waste heat. Thermoelectric devices (TEDs) constitute an attractive option to recycle waste heat and improve energy efficiency by direct conversion of this waste into electricity. Nonetheless, the relative low efficiency, toxicity, and scarcity of materials used in the fabrication of commercial TEDs have narrowed down their application to niche areas; hence the need for environmentally friendly and abundant materials with suitable thermoelectric properties have gained importance in materials research. The potential of a material for the direct conversion of heat into electricity is determined by the dimensionless figure of merit (ZT) defined as

$$\mathrm{ZT} = \frac{S^2 \sigma T}{k} \quad (1)$$

where S, σ, k and T are the Seebeck coefficient, electrical conductivity, total thermal conductivity and absolute temperature, respectively. The total thermal conductivity is compounded of a lattice k_l and electronic k_{el} contribution. Therefore, the optimisation of ZT requires the maximisation of thermoelectric power factor (PF) $(= S^2\sigma)$ and reduction of thermal conductivity to the least possible value. However, difficulty in decoupling these interconnected parameters has resulted in low conversion efficiencies with a benchmark for ZT around unity for current commercial materials, e.g., Bi_2Te_3.

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Single crystal silicon, which unlike most commercial materials, is abundant, low cost, has low toxicity, and has a high PF, yet its ZT (~ 0.01 at 300 K) is unattractive as a result of its high intrinsic thermal conductivity (~ 150 W/m K).[1] Nonetheless, the already established technology for scalable production of this material has kept the attention of material scientists to investigate novel approaches to optimize ZT. Boukai et al.[2] reported a ZT of about 0.4 at 300 K and close to unity at 200 K for silicon nanowires by achieving k of about 0.76 W/m K at room temperature, below the amorphous value in bulk silicon (~ 1 W/m K). Likewise, Hochbaum et al.[3] achieved a ZT of 0.6 at room temperature for rough silicon nanowires, attributed mainly to the 100 fold-suppression of thermal conductivity. Tang et al.[4] proposed an effective nanostructure formed by creating nanoholes in single crystalline silicon membranes reporting a ZT of around 0.4 at room temperature achieving a k in the range from 1.14 W/m K to 2.03 W/m K. Likewise, studies employing more conventional pellet-fabrication routes have also produced reasonable ZTs such as the work by Vining[5] and Bux et al.[6] More recently, defect engineering has proven to be an efficient method to reduce k in Si nano-films alongside insignificant deterioration of carrier transport,[7] i.e., the incorporation of lattice vacancies decreased k 20-fold, attaining a ZT of 0.2 at 360 K.

While all of these previous studies have taken Si in a form possessing high thermal conductivity and high thermoelectric power factor and have attempted to lower the former without affecting the latter, in this study we reverse this approach by using a Si-based starting material known to possess a very low thermal conductivity and aim to engineer a usable power factor. Our starting material is heterogeneous mixed-phased hydrogenated microcrystalline silicon (μc-Si: H), which consists of small silicon crystallites embedded in amorphous tissue. Such material structures are known to have low thermal conductivity, as evidenced by the extraordinarily low k demonstrated in various studies, with values < 0.1 W/m K previously shown.[6] The low k is primarily a result of the amorphous "tissue", which normally contains a large void fraction that hinders phonon propagation. The size of these voids is strongly dependent on the hydrogen content; hence the presence of this gas contributes to reduction of k in as-deposited films.[8] Even for highly-crystalline material with low porosity k remains relatively low, e.g., Wang et al.[9] reported a measured k of about 7.8 W/m K for poly-crystal grain sizes of 64 nm and porosity of 17% for undoped nano-crystalline silicon, which has a similar material structure to μc-Si: H. Measurements of k on the samples in this study (published elsewhere[10]) showed values in this same range. As a result, a relatively low k, if combined with good electrical transport, would mean μc-Si: H films could provide an attractive ZT to be used in thermoelectric applications.

Promising PF values have already been reported in nano-crystalline silicon. A PF ≈ 4.4 mW K^{-2} m^{-1} was reported by Kurosaki et al. in bulk nanostructured silicon which was attributed to the coherent or semi-coherent connection of a second phase precipitation of Phosphorus within the silicon matrix.[11] Similarly, a PF around 2.5 mW K^{-2} m^{-1} at 700°C was obtained by Kessler et al.[12] in nano-silicon pellets via rapid thermal annealing containing silicon oxides precipitates. Uchida worked on highly doped composite films of silicon nanocrystals and Ni silicide nanocrystals achieving maximum PFs of 1.1 and 1.9 mW K^{-2} m^{-1} at room temperature for n and p-type respectively after thermal annealing.[13] Most recently, high PFs in heavily boron-doped nano-crystalline silicon was reported with a concurrent increase of electrical conductivity and Seebeck coefficient by Narducci et al.[14] complemented by a theoretical study by Neophytou et al.,[15] and finally Loureiro et al.[16] with interesting PF trends observed as a function of doping concentration. In anticipation of similar effects in this work, we have investigated the PF of highly doped μc-Si: H thin films produced by plasma enhanced chemical vapour deposition (PECVD) as a function of post-annealing temperature and consequently, doping concentration. A high Seebeck coefficient, along with a favourable trade-off in thermal and electric properties would produce a promising material for Si thermoelectrics. Moreover, the deposition technique employed to produce μc-Si: H allows high, conformal and reproducible growth rates of deposition for relatively low-cost-fabrication at large industrial scales, as demonstrated already in the photovoltaics sector.[17]

EXPERIMENTAL SECTION

The samples used in this study consisted of n-type μc-Si: H thin films of 1 μm thickness deposited on Corning Glass of 1 mm thickness via the PECVD technique. n-type μc-Si: H samples were fabricated using RF (13.56 MHz), a power of 26 W at a substrate temperature of 185°C and total pressure of 0.4 kPa, using a gas flow mixture of 1 sccm of 2% PH_3 in SiH_4 and 200 sccm of H_2.

A thermal annealing treatment was applied on a selected set of highly homogeneous samples in terms of electrical conductivity. Six samples were subjected to annealing in air for 1 h under six different temperatures, i.e., 250°C, 300°C, 350°C, 430°C, 500°C, and 550°C. One additional sample was kept as-grown. The annealing was performed on a hot plate equipped with a programmable controller which permitted a stable temperature for a pre-defined time (1 h), reached in a ramp time of 8 min. During the cooling, all samples were left on the hot plate until they reached a temperature of about 30°C, which took approximately 2 h. A

thermocouple placed close to the sample was used to confirm the accuracy of the hot plate pre-set temperature during the entire treatment.

The electrical transport properties at room temperature, namely the carrier concentration, carrier mobility and electrical conductivity were obtained using a Bio Rad HL 5900 based on the Van der Pauw resistance measurement configuration, in combination with the Hall effect, which is suitable for in-plane characterisation of electrical conductivity and Hall coefficient measurement of thin films.

The Seebeck coefficient measurements were performed also in-plane using an LSR-3 instrument from Linseis, which is based on a four point configuration and records the variation of Seebeck coefficient with temperature. In our experiments the Seebeck variation was measured up to a temperature of 150°C from room temperature.

The structural study of n-type μc-Si: H was carried out employing complementary techniques for morphology characterisation. Micro-Raman spectroscopy was used to determine the crystalline volume fraction and crystallite size. The crystallinity was obtained by deconvolution of the Raman spectra into three parts. First, a broad band corresponding to the amorphous phase centred at ~ 480 cm^{-1}, a second peak of ~ 518 cm^{-1} corresponding to crystalline silicon, and an intermediate peak at ~ 510 cm^{-1} due to grain boundaries.[18] The crystalline volume fraction analysis is obtained based on the transverse optical phonon mode in the range 400–600 cm^{-1}. The average grain size is determined based on the peak shift and broadening dependence of Raman spectra with crystallite size. The apparatus used in our test was a Jobin–Yvon Horiba LabRAM 800 spectrometer equipped with an Olympus microscope (100× objective) and a 488 nm Ar + laser as the excitation source. The measurements were performed at room temperature and using a low laser power in order not to induce excessive local heating to avoid changes in the structure. The effects of annealing on surface morphology were analysed via scanning and transmission electron microscopy (SEM and TEM). SEM images were obtained with a Quanta FEG 650 SEM equipped with a concentric backscatter detector using backscatter imaging at low vacuum (~ 0.11 kPa) at 12 kV and magnification of 50,000× and TEM was carried out on a Jeol JEM-2000FX system with an acceleration voltage of 120 kV.

RESULTS AND DISCUSSION

Electrical Transport Properties

The evolution of carrier concentration, Hall mobility and electrical conductivity with annealing temperature for all six samples and the control sample, measured at room temperature, are shown in Fig. 1. The values of carrier concentration, 4.17×10^{20} cm^{-3}, and Hall mobility, 1.5 cm^2/Vs, plotted at a temperature of 20°C corresponds to the as-grown sample both stored and measured at room temperature. Similar silicon nano-structures for thermoelectric applications report the same level of carrier concentration,[16,19] which is close to the solid solubility limit of phosphorus in silicon, showing that the attempt to grow samples as highly doped as possible was realised. Likewise, carrier mobility is consistently lower than bulk silicon at the same carrier concentration, due mainly to the presence of large crystal disorder, void regions, potential barriers at grain boundaries, localized point- and extended-defects, in addition to ionized impurity scattering from phosphorous atoms, although it is in good agreement with values reported for highly n-doped thin films of this material structure.[20] A trend of decreasing carrier concentration with increasing annealing temperature in the range from 250°C to 550°C is observed. It starts at a value of 4.17×10^{20} cm^{-3} at room temperature and progressively falls to a minimum of 1.93×10^{20} cm^{-3} at 550°C. Since P solid solubility in Si at the annealing temperatures used is more than an order of magnitude below 4×10^{20} cm^{-3} dopant deactivation was expected during post-annealing. In contrast, Hall mobility increases in the same temperature range, opposing the trend in carrier concentration,[16,21,22] and is coherent with the high crystalline volume fraction determined in the next sections[16,21,22] such that the variation in electrical conductivity is much less pronounced, but reaching its maximum 14,204.5 $(\Omega m)^{-1}$ after annealing at 430°C, and is relatively constant across the post-annealing range. Electron Hall mobility starts at 1.5 cm^2/Vs for the as-grown sample at room temperature before reaching a peak of 3.1 cm^2/Vs at 500°C, before an abrupt drop to < 1.5 cm^2/Vs at 550°C. The opposing trend of Hall mobility is consistent with the large reduction experienced by the carrier concentration after annealing as less ionized atoms reduce electron scattering. The sample annealed at 550°C is not included in the trend line as the abrupt drop in electrical conductivity is accompanied by the appearance of cracks in the film structure, i.e., crack-like defects in the microstructure similar to those observed in Fig. 2, showing a thicker sample (3 μm) annealed with the same conditions. The crack creation is likely due to the increasing stress between the film and glass produced as a result of differences in coefficient of thermal expansion (CTE) during annealing. In the range from 0 to 300°C these values do not significantly differ.[23] Above 550°, however, this difference is expected to increase since silicon's rate of expansion decreases,[24] while the expansion rate of the glass is expected to increase rapidly, if considered to have similar behaviour to Borosilicate, which is the main component.[25]

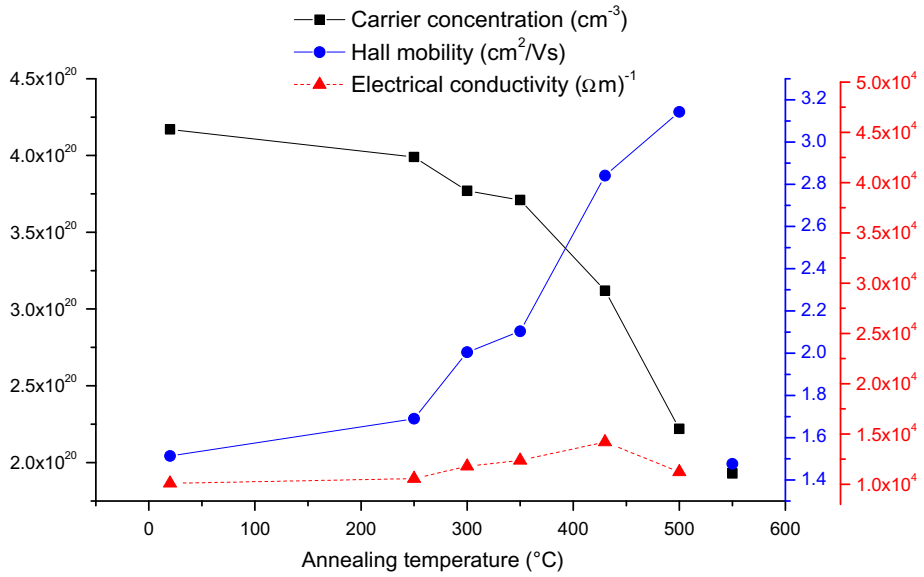

Fig. 1. Evolution of carrier concentration (closed squares), Hall mobility (closed circles) and electrical conductivity (closed triangles) with post-annealing treatment from 250°C to 550°C. An opposite trend of Hall mobility consistent with decrease of carrier concentration and the corresponding reduction of electron scattering by impurity phosphorous atoms is observed.

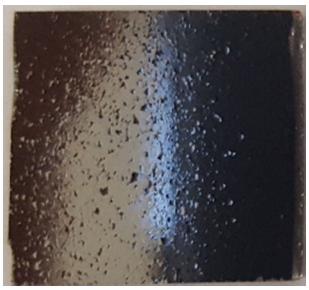

Fig. 2. Crack-like defects produced in μc-Si: H thin films with post-annealing at 550°C for 1 h in air. Similar cracks appeared in samples of both 1 μm and 3 μm thickness which produced an abrupt drop in electrical conductivity.

Seebeck Coefficient

Figure 3 shows the evolution of S with post-annealing treatment. The absolute Seebeck value for the as-grown sample is about -106 μV/K at room temperature. Higher S values have been published in undoped μc-Si: H (-900 μV/K) although in that particular study σ (= 0.05 Ω^{-1} m^{-1}) is far below that from their highly doped counterparts.[21] For lowly phosphorous doped μc-Si: H, Sellmer, et al.[22] reported S values between -600 μV/K to -800 μV/K at room temperature which establishes a close relation with crystalline volume fraction. The lower S measured in our samples can be explained due to the higher carrier concentration ($\sim 10^{20}$ cm^{-3}) in a highly crystalline structure (> 70%). A rather constant S of about -107 μV/K is observed in samples at the annealing steps from 250°C up to 350°C if we consider the standard error of 5% for the equipment in question. Then S progressively increases in the two subsequent annealing steps (430°C and 500°C) to -121 μV/K and -136 μV/K, respectively. The Seebeck data points for the sample annealed at the highest temperature (550°C) present wide variation as a function of measurement temperature and are, therefore, not included in the graph. This is likely due to the creation of crack-like defects as already identified. The rise of S is coherent with the Pisarenko relation[26] in the observation that the increase of S occurs due to the fall of carrier concentration, and with the assumption that the crystalline-dependent effective density of states in the conduction band may remain invariable[22] as the crystalline volume fraction obtained from Raman analysis shows no change with post-annealing treatment. A similar increase of S after annealing was demonstrated by Uchida et al.[13] in highly P-doped films based on silicon nanocrystals. This effect is attributed to passivation of mid-gap defects. It is known that μc-Si: H has plenty of localized defects states at the mid-gap,[27] and we cannot rule out that energy filtering due to potential barriers formed at the grain boundaries of this material[28] contributes to the rise of S, as was suggested by Narducci et al.[14,29]

Power Factor

Figure 4 shows the thermoelectric power factor at room temperature resulting from the combination of σ and S with post-annealing treatment. The as-grown sample provides a PF of about 1.13×10^{-4} W/mK^2. Although higher Seebeck coefficients have been reported in this material when it is intrinsic or lowly doped, if we compare with the resulting PF for undoped material (= 4.05×10^{-8} W/mK^2)[21] and an

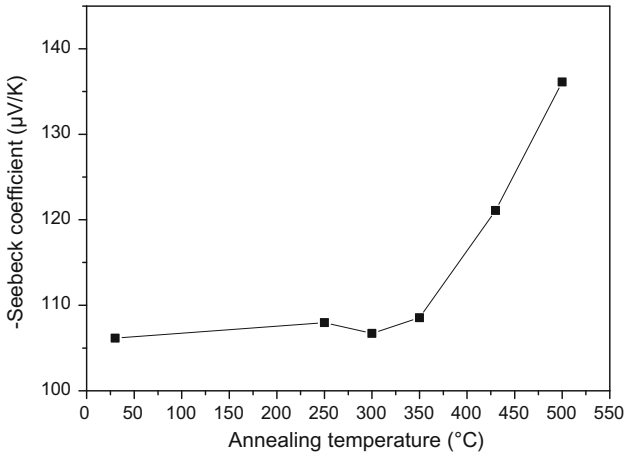

Fig. 3. Evolution of Seebeck coefficient measured at room temperature with post-annealing treatment. A constant S is observed for annealing steps from 250°C to 350°C, while a progressive increase takes place at the two subsequent annealing steps reaching a maximum of $-$ 136 μV/K. Sample annealed at the last step (550°C) presents an inconsistent reading as a result of crack formation in the sample.

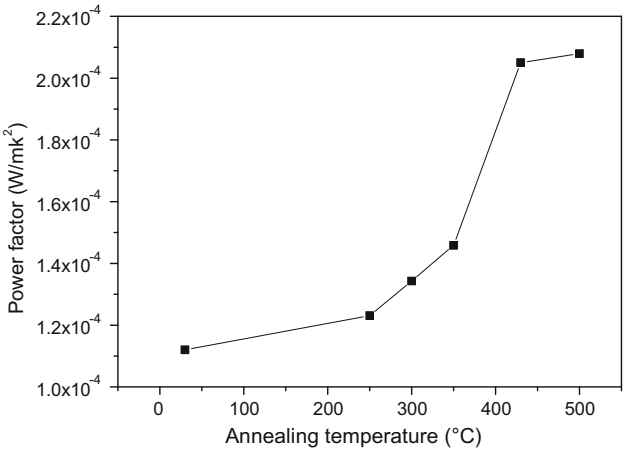

Fig. 4. Evolution of PF measured at room temperature in μc-Si: H samples with post-annealing treatment in the range from 250°C to 500°C. PF is maximised after post-annealing at 500°C. Sample annealed at 550°C is not included in the plot due to anomalous trend of S with temperature.

estimation for low n-doped μc-Si: H (= 6.9×10^{-5}–1.2×10^{-4} W/mK^2),[22] the as-grown PF in our highly doped n-type μc-Si: H is larger, or at least at the same level, of the sample with the highest S ($-$ 800 μV/K) due to the trade-off between S and σ. The post-annealing treatment we applied proved to improve the PF by more than 80%. PF depicts a progressive increase up to a maximum of 2.08×10^{-4} W/mK^2 after post-annealing at 500°C, which is comparable to the best results published recently for n-type hydrogenated nano-crystalline silicon.[16] Thus, an optimised trade-off between S and σ is approached via post-annealing treatments up to 500°C. Even though this value is comparable to the state-of-the-art for this material, it should be noted that the PF rise clearly continues to increase as the doping concentration reduces. This suggests that the best current PF can be exceeded by producing samples with a lower initial carrier concentration. Indeed, in bulk Si the optimum doping concentration to maximise the PF is 6–7×10^{19} cm^{-3}[30] about half the value in the best samples here. Post-annealing for dopant deactivation could have been further explored in our current study; however, for higher annealing temperatures, sample cracking was expected. Indeed, data points from the sample annealed at the highest temperature are not included in the plot due to unexpected trend of S and σ due to the creation of cracks.

Film Structure

The structural characterisation of n-type μc-Si samples was performed via Raman spectroscopy. In order to distinguish any change in structure with post-annealing treatment, the crystalline volume fraction and crystallite size was determined using the relationship $X_c = (I_c + I_m)/(I_c + I_m + yI_a)$ where I_c, I_a, I_m correspond to the integrated intensities of the crystalline, amorphous and intermediate phases whilst (y) is the ratio of the integrated Raman cross section for the amorphous to crystalline phase. This parameter is still under debate; it varies depending on the crystallite size and excitation wavelength from $\sim$ 1 to 0.4[18,31] and is taken as 0.8 in our study. The deconvolution of Raman spectra is carried out by the superimposition of three Gaussian components centred at each phase. Figure 5 shows an example of deconvolution following this criteria.

The crystalline volume fraction and crystallite size of the as-grown and post-annealed samples are shown in Fig. 6. It can be observed that all samples have a crystalline fraction over 70%. The small difference between the as-grown (74.6%) and the sample annealed at 350°C (70.6%) is within the standard error induced in the calculation method, which depends on the degree of crystallinity. For highly crystalline μc-Si: H, the error is not larger than 5%.[23] This crystalline volume fraction is in good agreement with similar μc-Si: H produced for solar cells, which ranges from about 60 to 70%.[23] It would mean the post-annealing treatment has not affected the crystallinity, implying the material has reached saturation. The average crystallite size is determined based on the correlation length model,[32,33] which predicts satisfactory results for crystallite sizes larger than 5 nm. This model is preferred as the expected crystallite size for μc-Si: H structures should be $>$ 5 nm.[23] In order to isolate the effect of crystallite size on the Raman line, a low laser power was used to not induce local heating and crystallization, and on the other hand, the roughly similar CTE of Corning Glass (0.355×10^{-5} K^{-1}) and silicon (0.3×10^{-5} K^{-1}) allows negligible stress on the films.[23] This model permits to estimate the

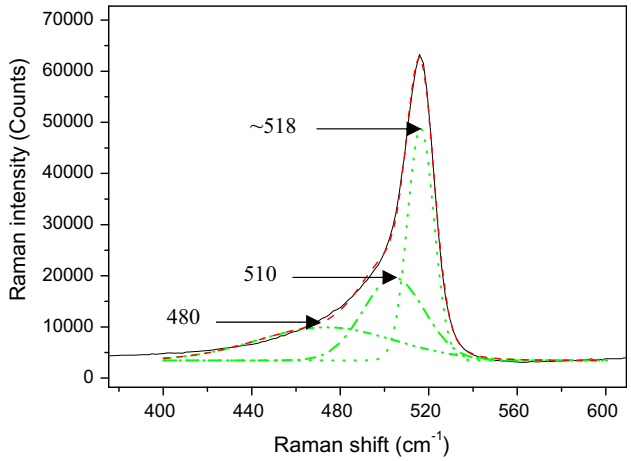

Fig. 5. Example of deconvolution (dash lines) of the Raman spectrum obtained from a μc-Si: H sample of 1 μm thickness. Three Gaussian curves centred at $\sim$ 518 (dot line), 510 (dash-dot line) and 480 (dash-dot-dot line) cm^{-1} are used to fit the experimental Raman spectra (solid line), which corresponds to the crystalline, intermediate and amorphous phases, respectively.

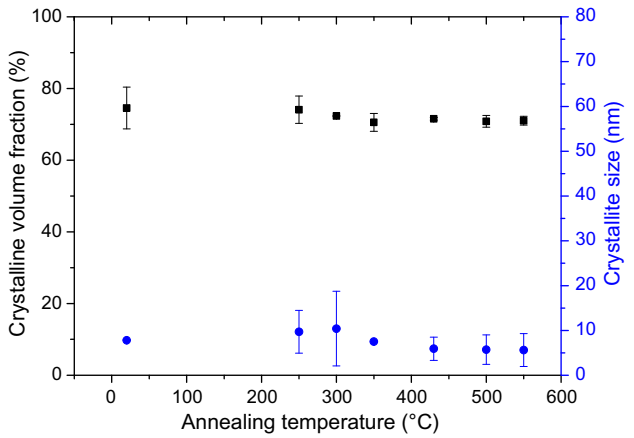

Fig. 6. Crystalline volume fraction (closed squares) and crystallite size (closed circles) in as-grown and annealed μc-Si: H samples of 1 μm thickness. Crystallinity remains unchanged after annealing at a value of about 70%, while crystallite size ranges from 6 nm to 10 nm with no clear growth trend following annealing. Error bars represent the standard deviation for measurements on the same sample.

crystallite size based on the peak shift. Figure 6 shows the values of crystallite size ranging from 6 nm to 10 nm which will be corroborated with TEM micrographs (discussed later).

Figure 7 shows the SEM top-down micrographs of (a) an as-grown sample, (b) annealing at 350°C, (c) annealing at 430°C and (d) annealing at 550°C. Micrographs show that these films emerge at the surface as "hillock-like" conglomerates of crystallites of similar size and shape. These reflect the tops of the columnar structures that grow upwards from the underlying glass substrate. Clusters of grains with an average size of about 110 nm were statistically estimated to be present in the surface of all samples using image processing. Most of the brighter (conglomerates) areas are surrounded by a dark material, which probably represents the amorphous tissue and inter-columnar space. Some overlapping of conglomerates are observed in all samples which give a "cauliflower-like" appearance similar to those reported in.[34] The surface crystalline fraction was obtained through the comparison of the bright regions which represent the conglomerates of crystallites and the dark areas surrounding these which constitute the amorphous tissue giving an estimate of $\sim$ 72%. The crystallinity and cluster size in the as-grown and annealed samples do not show a large variation, which signifies that post-annealing treatment has not had a major effect on the surface morphology.

TEM cross-section micrographs for a sample annealed at 550°C are shown in Fig. 8. It is observed in Fig. 8a that columnar structures of crystallites grow upwards, perpendicular to the substrate and are separated by incoherent boundaries. The columns, elongated from bottom to top, show little variation in size with a length roughly the same as the sample thickness. The estimated thickness of the annealed sample is about 885 nm, which is in good agreement with the pre-determined value expected based on the deposition rate. A number of narrow crack-like structures (incoherent boundaries) are visible in-between the crystal columns with an average width of 3.5 nm. A higher density of cracks is noticeable near the substrate,[35] which implies the columns are loosely packed, while towards the top the structure looks more compact. In the enlarged micrograph (Fig. 8b), crystallographic texture with crystals oriented in different directions is observed. The enlarged image permits to appreciate that the cracks are not an empty volume, but filled with a low-density material (brighter features). The absence of an amorphous incubation layer, commonly described for this material in the literature, confirms a microcrystalline structure starting from the glass-silicon interface up to the top surface. The crystalline volume fraction was estimated from the contrast comparison of the dark (crystalline phase) and bright (amorphous phase) regions resulting in a value of $\sim$ 74%, which is in good agreement with Raman crystallinity. The good correlation between the surface crystalline fraction estimated by SEM and the volume crystalline fraction obtained via TEM has its foundations in the length of the grown columnar crystallites, which is about the same as the film thickness. A statistical analysis provides an average crystallite size of about 10 nm, which is in good agreement with Raman values obtained based on the peak shift.

The structure of μc-Si: H thin films, which are a heterogeneous systems composed of small crystallites embedded in amorphous tissue and separated by interfaces of disordered material and narrow voids, is confirmed by TEM micrographs. These features make it difficult to predict the electronic

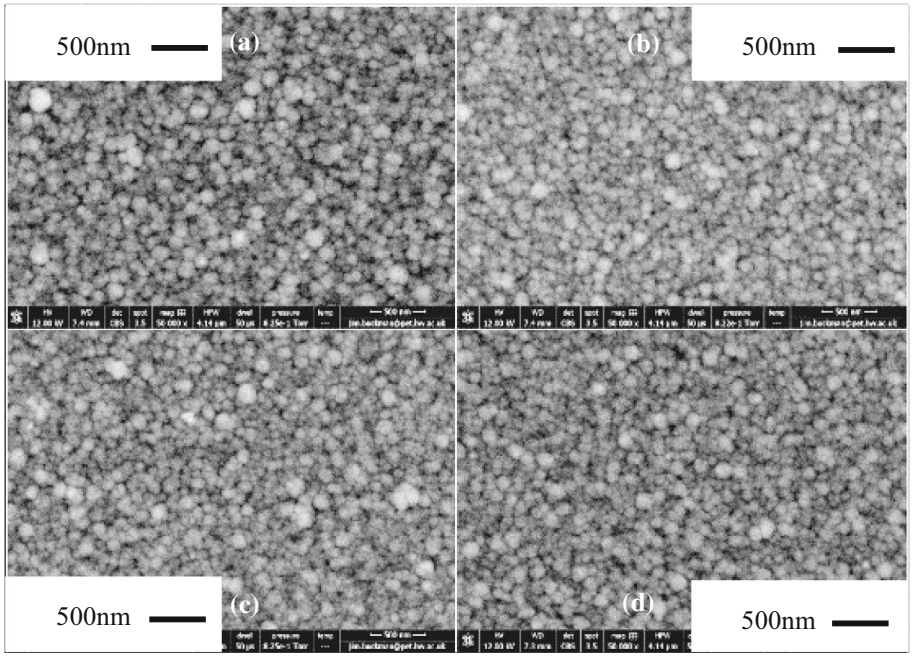

Fig. 7. SEM micrographs (top-down) obtained with a magnification of 50,000× at 12 kV for μc-Si: H samples: (a) as deposited, (b) 350°C, (c) 430°C and (d) 550°C.

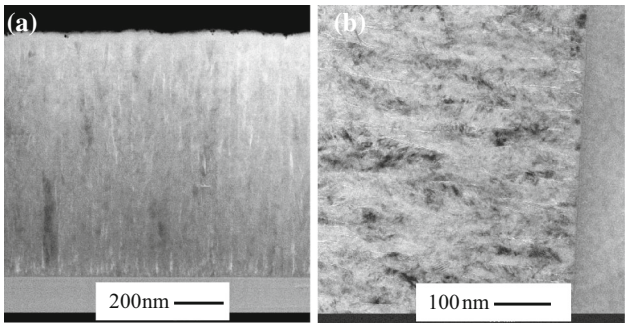

Fig. 8. Cross-sectional TEM micrographs of sample annealed at 550°C. (a) Micrograph showing a columnar growth separated by narrow cracks filled with low-density material. (b) Enlarged micrograph (oriented by 90°) showing a crystallographic texture with crystals oriented in different directions.

transport mechanism. Hence, the increase of electrical conductivity and Seebeck coefficient with post-annealing treatment will be further discussed in terms of morphological changes observed after annealing.

The increase of Hall mobility after annealing is likely to be explained by the reduction of scattering impurity atoms given the accompanying drop in carrier concentration. Thus, it is reasonable to associate the increase of mobility due to the reduction of ionized impurity scattering, which constitutes the dominant scattering mechanism and considering the unmodified microstructure evidenced in the morphological study. In particular, any increase of mobility due to an increase of crystallite size can be ruled out as demonstrated in the Raman results.

The fall in carrier concentration after annealing can be explained by a number of mechanisms. The first is the formation of P-H complexes, because of the large availability and atomic mobility of *H* within the material, deposition of μc-Si: H requires a high dilution of hydrogen for the transition of amorphous into microcrystalline structure. Only a small amount of this gas acts in the transformation process, so that a non-negligible amount of this gas remains in the microstructure, in particular in voids, inter-columnar spaces and forming Si-H preferentially at grain boundary regions.[23,36] Since P is initially electrically active in concentrations above its solid-solubility limit, it is also likely that P clusters or P-Si complexes also form.

The Seebeck coefficient behaviour is in agreement with the expected relationship, where a fall of carrier concentration leads to an increase of *S* with the assumption of an invariable effective density of states based on the roughly constant crystallinity determined on as-grown and annealed samples by Raman and TEM.

As a result of the changes in electrical properties with post-annealing treatment, a significant improvement of PF is obtained. This approach provides an alternative path to achieving optimised values by a simple post-processing with no impact on the mechanical stability of μc-Si: H thin films; however, the production of as-grown films with a lower doping concentration may be a better route to optimise the PF and ultimately the ZT.

CONCLUSION

This study has investigated the potential of μc-Si: H thin-films for thermoelectric applications, based on existing knowledge suggesting that this form of Si film possesses extremely low thermal conductivity, which is a prerequisite for thermoelectrics. In contrast, an extremely high electrical conductivity is necessary, and this study has found that highly-doped n-type films with reasonable electron mobility are realisable. The Seebeck coefficient of the films was relatively low, but improved following post-annealing, accompanying a fall in carrier concentration, but with little overall change in electrical conductivity. This allowed thermoelectric power factors to be demonstrated in line with the best previously found for nc-Si: H thin-films. Since the best power factor was found with the lowest carrier concentration, there is significant scope to reduce the concentration further as a means to fully optimise the power factor. Also of promise was the fact that the films remained thermally and mechanically stable for post-annealing up to 500°C. After exposure at 550°C, cracks appeared that were visible to the naked eye and damaged film integrity; however, degradation of the microstructure was not evident.

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