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Frequency Dependent Electrical and Dielectric Properties of Au/P3HT:PCBM:F4-TCNQ/n-Si Schottky Barrier Diode

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In this study, poly(3-hexylthiophene):[6,6]-phenyl-C_{61}-butyric acid methyl ester: 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (P3HT:PCBM:F4-TCNQ) organic film was deposited on *n*-type silicon (n-Si) substrate by spin coating method. The electrical and dielectric analysis of Au/P3HT:PCBM:F4-TCNQ/n-Si Schottky barrier diode was conducted by means of capacitance–voltage (*C*–*V*) and conductance-voltage (G/ω–*V*) measurements in the frequency range of 10 kHz–2 MHz. The *C*–*V*–*f* plots exhibit fairly large frequency dispersion due to excess capacitance caused by the presence of interface states (N_{ss}). The values of N_{ss} located in semiconductor bandgap at the organic film/semiconductor interface were calculated by Hill–Coleman method. Experimental results show that dielectric constant (ε') and dielectric loss (ε'') decrease with increasing frequency, whereas loss tangent ($\tan\delta$) remains nearly the same. The decrease in ε' and ε'' was interpreted by the theory of dielectric relaxation due to interfacial polarization. It is also observed that ac electrical conductivity (σ_{ac}) and electric modulus (M' and M'') increase with increasing frequency.

Key words: Organic film, frequency and voltage dependence, density of interface states, electrical conductivity

INTRODUCTION

Organic materials have been attracting considerable attention of the scientific community due to their favorable features and unique applications. These materials can be chemically tailored to adjust separately the band gap, valance and conduction band energies.[1] The polymer-fullerene blends would provide future scope of their applicability in the field of organic photovoltaics. The fullerene derivative, [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM) acts as an electron acceptor and a conducting polymer, poly(3-hexylthiophene) (P3HT), as an electron donor.[2] P3HT/PCBM has the advantage over other organic compounds because of its promising possibilities such as low-processing cost, large-area devices, light weight, and flexible substrate deposition.[3–8]

Recent studies have shown that it is possible to obtain high-quality SBDs by the deposition of a proper organic interfacial layer between metal and semiconductor.[1,9–11] The presence of an interfacial layer with non-uniform thickness or composition causes non-uniform voltage drop across the interface, thus leading to deviation from ideal behavior of SBD. In this context, the interface quality has fundamental importance for the controlled modification of charge transport and extraction process, which determines the device performance and long term stability. The charge transport properties of conjugated polymers depend on the packing of the chains and the ordering in the solid films, as well as on the density of impurities and structural defects.[12] Since most organic polymers do not have intrinsic charge carriers, doping is a common way to

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provide additional charge carriers which contributes to improve the observed p or n type conductivity. Among numbered dopants, F4-TCNQ is one of the strongest known molecular electron acceptors and exhibits high electron affinity.[13,14] Doping P3HT with F4-TCNQ has recently been used in solar cell[13,15] and field effect transistor[16] applications.

Research on the modification of the conventional metal–insulator–semiconductor (MIS), metal–polymer–semiconductor (MPS) types of SBDs or metal–oxide–semiconductor (MOS) capacitors to increase the specific capacitance is also in progress. A larger capacitance ($C = \varepsilon'\varepsilon_o A/d_{il}$) of these structures can be obtained by either increasing dielectric constant (ε'), increasing the electrode surface area (A) or by decreasing the thickness of interfacial layer (d_{il}), but the thickness of d_{il} is selected by the required withstand voltage and cannot be tempered. Thus, the capacitance value of structure can be considerably increased by using a high-dielectric interfacial layer and it can be used in a wide range of charges/energy capture and storage applications. Demirezen et al.[17] obtained the value of ε' for PrBaCoO nanofibers at 1 kHz, which is 276 times more than the dielectric constant value of conventional SiO_2, and 21 times greater than TiO_2. The high dielectric interfacial layer prevents the inter-diffusion between metal and semiconductor and also alleviates the electric field reduction issue in these structures.

The frequency dependent capacitance–voltage (C–V) and conductance-voltage (G/ω–V) measurements yield accurate and reliable information about the doping of organic material and the existence of localized trap states and the trapping process in these devices. Depending on the frequency, interface states could follow the ac signal, thus yield an excess capacitance. However, at sufficiently high frequency (≥1 MHz), they are independent of frequency as each defect in the structure is frozen. On the other hand, it is important to investigate the dielectric relaxation behavior in conjugated-polymer based devices. Admittance measurements can be used as a powerful analysis tool to evaluate dielectric relaxation, interfacial polarization and the electrical conductivity of these devices. A method of predicting the relaxation behavior of composites, the electric modulus spectra, is used to investigate conductivity as well as its associated relaxation in conjugated polymers.[18]

In this work, we reported the fabrication and characterization of Au/P3HT:PCBM:F4-TCNQ/n-Si Schottky barrier diode (SBD). For a better understanding of the impact of frequency on the interface states and dielectric properties of the prepared diode, the C–V and G/ω–V measurements were made in the wide range of frequency and voltage. Various parameters such as density of interface states (N_{ss}), series resistance, dielectric constant (ε') and dielectric loss (ε''), loss tangent ($\tan\delta$), ac electrical conductivity (σ_{ac}), and electric modulus (M' and M'') were calculated by using C–V and G/ω–V measurements.

EXPERIMENTAL DETAILS

For the preparation of blend solution, P3HT, PCBM and F4-TCNQ organic compounds were supplied from Sigma-Aldrich Ltd. and used without further purification. The mixtures of P3HT:F4-TCNQ were prepared by dissolving in 1-2 dichlorobenzene with a concentration of 25 g/L while F4-TCNQ was dissolved in 1,2-dichlorobenzene at a concentration of 0.01 mg/mL. Then the dissolved materials were stirred at 60°C for 3 h in a dry nitrogen environment.

The stirring process was followed by the preparation of P3HT:PCBM:F4-TCNQ organic blend. For this purpose, various amounts of F4-TCNQ were added to P3HT:PCBM blend solution with a weight ratio of 1:1 (10 mg/mL:10 mg/mL) to separate P3HT:PCBM solutions with the F4-TCNQ concentration of 1%. Subsequently, the blend solution was stirred overnight prior to the spin casting for complete mixing.

For the fabrication of the Au/P3HT:PCBM:F4-TCNQ/n-Si SBDs, phosphorus doped n-type single crystalline silicon (sc-Si) wafer (with <100> orientation, 350 ± 25 μm thick, 4.8 Ω cm resistivity) was used as a substrate. Immediately, surface cleaning of sc-Si wafer by RCA procedure and evaporation of silver (Ag) metal with a thickness of ~2500 Å, which was used as the low-resistivity ohmic back contact, onto the whole back side of Si substrate by thermal evaporation system were performed. Then, Ag-evaporated Si substrates were annealed by the thermal annealing at 450°C for 30 min under N_2 flow in order to achieve a good ohmic contact. Immediately, the P3HT:PCBM (1:1) solutions with F4-TCNQ concentration of 1% (F4-TCNQ to polymer ratio) were spin-coated onto the front surface of the sc-Si wafer at 1500 rpm/s for 30 s to form a continuous P3HT:PCBM:F4-TCNQ films with ~100 nm thickness. Subsequently, the samples were thermally annealed on the hot plate at 150°C for 15 min to evaporate the solvents and simultaneously to dry the samples. After the spin coating of organic layer, circular-shaped gold (Au) rectifying contacts with a 99.999% purity in a diameter of 1 mm were evaporated on the P3HT:PCBM:F4-TCNQ organic layer (on the front side of the Si wafer) through a metal shadow mask by a thermal evaporator vacuum system with the pressure of $\sim 1 \times 10^{-6}$ mbar. The thickness of the circular-shaped Au contacts and the deposition rate of the Au evaporation were ~2500 Å and ~3 Å/s, respectively, and both were monitored by the digital quartz crystal thickness monitor.[8]

Quanta FEG scanning electron microscope (SEM) was used for the investigation of the P3HT:PCBM:F4-TCNQ surface morphology. The

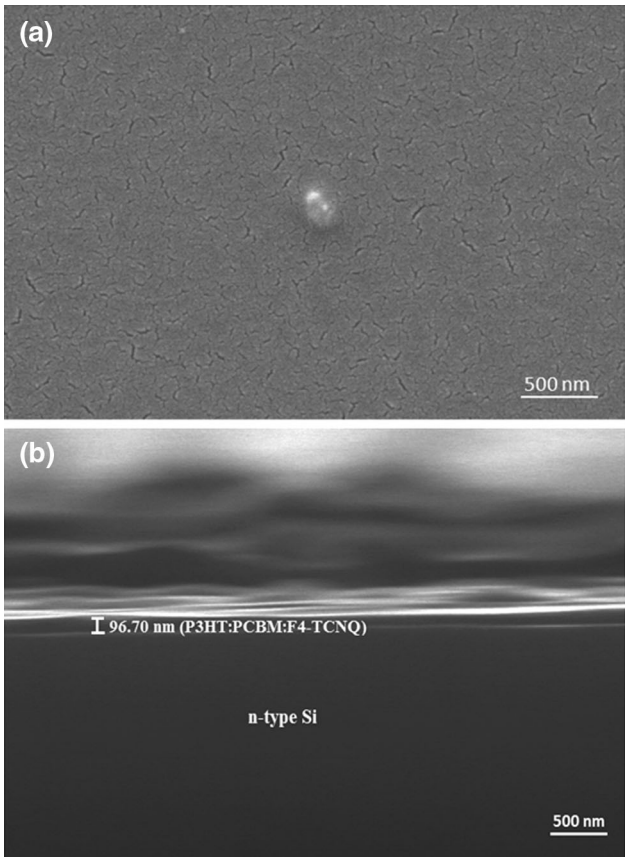

Fig. 1. (a) Top-view and (b) cross-sectional SEM images of P3HT:PCBM:F4-TCNQ layer.

operating voltage and working distance were 5 kV and 4.8 mm, respectively. Prior to loading the sample in the SEM chamber, P3HT:PCBM:F4-TCNQ surface was coated with a layer of gold to increase the conductivity of film for SEM view. Figure 1a shows 5 kV acceleration voltage SEM image of P3HT:PCBM:F4-TCNQ surface with the scale of 500 nm. In this figure, the grey area is the P3HT:PCBM polymer layer[19] while the bright portion is the F4-TCNQ dopant about 200 nm in diameter.[20] As shown in Fig. 1a, only one F4-TCNQ portion was detected by SEM for the 500 nm scale. This can be due to the very small amount of F4-TCNQ dopant concentration (1%) in the P3HT:PCBM:F4-TCNQ organic blend, which is compatible with literature.[20] Additionally, the cross-sectional SEM image of P3HT:PCBM:F4-TCNQ/n-Si structure was monitored to measure the thickness of P3HT:PCBM:F4-TCNQ polymer layer as shown in Fig. 1b. As a result, the thickness of polymer layer was found to be approximately 100 nm.

The frequency dependent capacitance–voltage (C–V) and conductance-voltage (G/ω–V) measurement processes of the Au/P3HT:PCBM:F4-TCNQ/n-Si SBDs were carried out as a function of frequency (10 kHz–2 MHz) using an HP 4192A LF impedance analyzer (5 Hz–13 MHz). All measurements were performed at room temperature by means of a microcomputer through an IEEE-488 AC/DC converter card.

RESULTS AND DISCUSSION

Frequency Dependent Capacitance–Voltage (C–V) and Conductance–Voltage (G/ω–V) Characteristics

Figure 2 shows the C–V and G/ω–V plots of Au/P3HT:PCBM:F4-TCNQ/n-Si SBD carried out at the frequency range of 10 kHz–2 MHz at room temperature. The capacitance and conductance decrease with increasing frequency as the traps start to respond to ac signal. The frequency dispersion of the C and G/ω in the depletion region possibly stems from the interface states at the polymer/Si interface and bulk charges. These charges may be due to the presence of unwanted impurities, network vacancies, interstitial anomalies and interface related phenomena.[21] The interfacial insulator or polymer materials can be easily polarized under an external electric field that displaces the charges from their equilibrium position or traps. In this case, the charges or dipoles can be restructured and reordered under an electric field depending on their relaxation times. There are many types of surface states or traps with different lifetimes and at low frequencies these states affected by the applied signal are able to give up and accept charges in response to this signal. The value of C for 10 kHz at 10 V is about 16 nF and the value of G/ω is about 32 nF, but their shapes are similar. For the MIS or MPS type SBDs with a high enough interfacial layer thickness, the changes in the real and imaginary parts of admittance ($Y = 1/Z = G + j\omega C$) are almost the same especially due to series resistance, and in this case, both C–V and G/ω–V plots have similar shapes. When these corrections are made by considering the effect of series resistance, the capacitance in the accumulation region is estimated to increase with the increasing voltage, whereas conductance decreases and the peaks in the G/ω–V plots become more distinctive.[9]

Series resistance (R_s) is one of the important sources of small energy loss in SBDs. R_s may originate from various sources such as the back ohmic contact to the semiconductor, the contact made by the probe wire to the gate or rectifier contact, the bulk resistance of the semiconductor, a dirty film or particulate matter at the back contact/pedestal interface and extremely non-uniformly doped atoms in the semiconductor. It can cause a serious error in the extraction of interface properties and doping profiles from conductance measurements.[22] In order to avoid this error and the senility limitation, R_s can be minimized by making measurements at sufficiently low frequencies, where the effect of N_{ss} is dominant, or applying a correction on the measured admittance. The relationship between

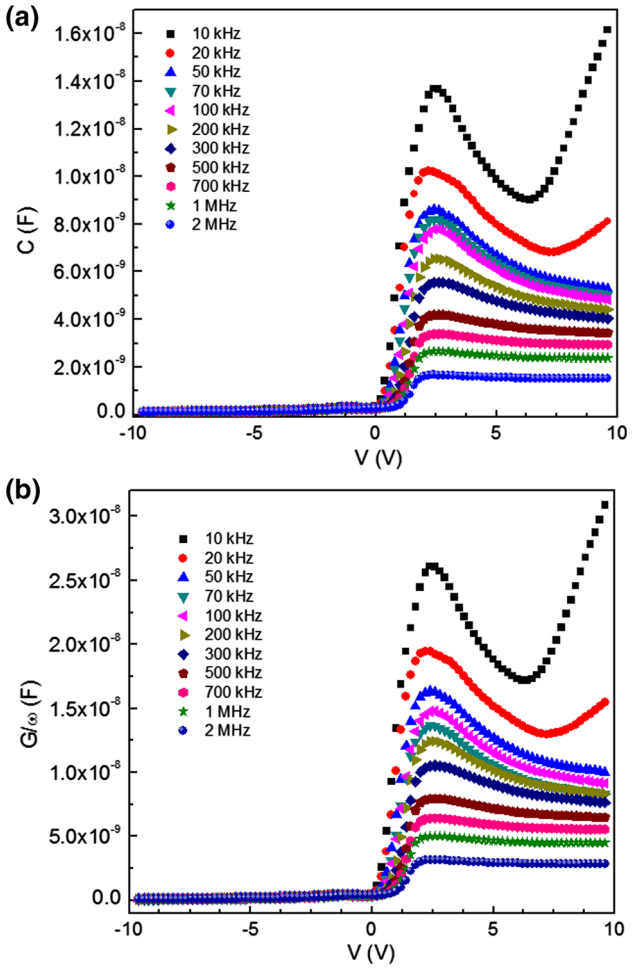

Fig. 2. Forward and reverse bias (a) *C–V–f* and (b) *G/ω–V–f* characteristics of Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

the interface states, R_s, charging process and admittance (*C–V* and *G–V*) of the MIS or MPS types of SBDs measured in the external circuit has been described and analyzed by Nicollian and Brews in detail.[23] The method developed by them is thought to be generally more accurate than the other reported methods that use *I–V* data and it ensures the determination of R_i over whole measurement range. According to this method, the real value of R_i at sufficiently high frequencies ($f \geq 500$ kHz) corresponds to the real value of series resistance (R_s) for MIS or MOS structures and can be subtracted from the measured C and G values in the strong accumulation region as follows[23,24]:

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \quad (1)$$

where ω (=$2\pi f$) is the angular frequency, C_m and G_m/ω are the measured capacitance and conductance values in the strong accumulation region.

The voltage and frequency dependence of the resistance was obtained from the measurements of

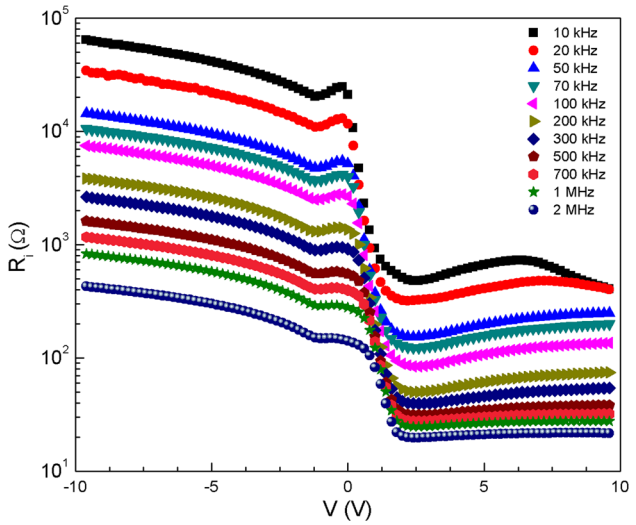

Fig. 3. The frequency dependent R_i–*V* characteristics of Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

C–V–f and *G/ω–V–f* curves by using Eq. 1. It is clearly seen in Fig. 3 that R_i is strongly dependent on voltage and frequency and the series resistance value at each frequency is large enough to affect the capacitance. Thus, special attention should be paid to the effects of series resistance in the application of admittance-based measurement methods.

The application of a single-frequency approximation method[25] enables the quantitative determination of the density of interface states (N_{ss}) from *C–V* and *G/ω–V* measurements. The frequency distribution of N_{ss} can be derived from Hill Coleman method by using the following equation:

$$N_{ss} = \frac{2}{qA}\left(\frac{G_{max}}{\omega}\right)\left[\left(\frac{G_{max}}{\omega C_i}\right)^2 + \left(1 - \frac{C_{max}}{C_i}\right)^2\right]^{-1} \quad (2)$$

where A is the rectifier contact area, ω is the angular frequency (=2πf), C_i is capacitance of interfacial layer, G_{max} corresponds to the maximum value in *G–V* curve and C_{max} is the capacitance value corresponding to G_m. According to Nicollian and Brews,[20] the value of interfacial layer capacitance can be extracted from the high frequency ($f \geq 500$ kHz) C and G values at the strong accumulation region as:

$$C_i = C_m\left[1 + \left(\frac{G_m}{\omega C_m}\right)^2\right] \quad (3)$$

The density distribution profile of N_{ss} for Au/P3HT:PCBM:F4-TCNQ/n-Si SBD was obtained by using Eq. 2 and given in Fig. 4. The values of N_{ss} were not high enough to pin the Fermi level of the Si substrate. This is verified by the behavior of *C–V* and *G/ω–V* plots which has three distinct regimes of accumulation–depletion–inversion regions.

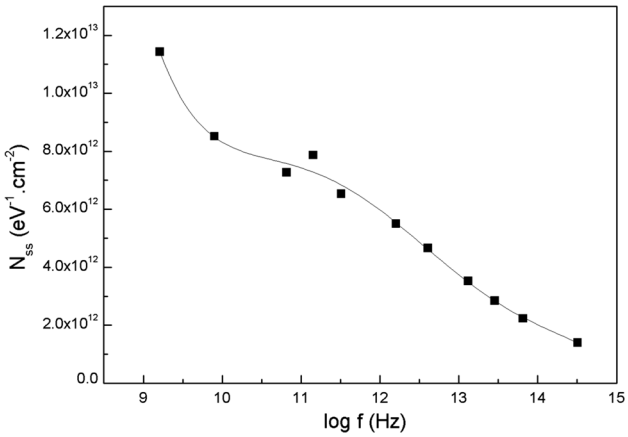

Fig. 4. The N_{ss}–f plot of Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

Frequency Dependent Dielectric Properties

Dielectric analysis measures the capacitive and conductive nature of materials. The dielectric behavior of the structure has been studied over a wide range of frequency (10 kHz–2 MHz). The complex permittivity (ε^*) formalism has been used to obtain significant data about the chemical and physical behavior of the electrical and dielectric properties. The frequency dependent value of $\varepsilon^*(\omega)$ includes the real (ε') and imaginary (ε'') parts, which correspond to the dielectric constant and dielectric loss of the material and they refer to the storage and loss of energy in each cycle of the applied electric field, respectively. It is expressed as[26–28]:

$$\varepsilon^*(\omega) = \varepsilon' - j\varepsilon'' \tag{4}$$

The values of the real dielectric constant ε' in the frequency range of 10 kHz–2 MHz are calculated by using the measured capacitance values according to the following relation[29,30]

$$\varepsilon' = \frac{C_m}{C_o} = \frac{C_m d_{il}}{\varepsilon_0 A} \tag{5}$$

where C_o ($=\varepsilon_o A/d_{il}$) is the capacitance of an empty capacitor, A is the rectifier contact area in cm^{-2}, d_{il} is the thickness of interfacial organic layer ($\approx$100 nm) and ε_o is the permittivity of free space charge ($\varepsilon_o = 8.85 \times 10^{-14}$ F/cm). In the strong accumulation region, the maximal capacitance of the SBD corresponds to the interfacial organic layer capacitance. In addition, the values of ε'' are calculated by using the measured conductance values from the relation

$$\varepsilon'' = \frac{G_m}{\omega C_0} = \frac{G_m d_{il}}{\varepsilon_0 A} \tag{6}$$

The tangent ($\tan\delta$) is the ratio of energy dissipated per radian in the dielectric material (ε'') to the energy stored at the peak of polarization (ε'). Therefore, the investigation of $\tan\delta$ as a function of frequency and voltage is considered an important subject. The values of loss tangent provide data about the conduction mechanism and dielectric relaxation, and it can be calculated by using the obtained ε' and ε'' values as seen in the following relation[30]:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{7}$$

Figure 5 shows the variation of dielectric constant ε' and dielectric loss ε'' with frequency and voltage. In order to get high/ultra-capacitor, high-dielectric interfacial layer is desirable so that it can be used in a wide range of charges/energy capture and storage applications. Figure 5a demonstrates that the value of ε' of P3HT:PCBM:F4-TCNQ at 10 V was found to be about 250 for 10 kHz, and this value is almost 83 times greater than the dielectric constant value of conventional SiO_2[31] and six times greater than TiO_2 interfacial layer[32] at the same frequency. The values of ε' and ε'' decrease with increasing frequency, whereas the value of tan δ observed in Fig. 6 remains almost unchanged. This frequency dispersion of ε' and ε'' may be explained by supposing that the mechanism of the polarization process is similar to that of the conduction process. As explained by Maxwell–Wagner,[33] the inhomogeneities can lead to a frequency dependence of the conductivity because charge carriers accumulate at the boundaries of less conductive regions, hence creating interfacial polarization. Higher conducting phase (grains) in the insulating grain boundaries of a dielectric material gives rise to the localized accumulation of charges under the influence of electric field. In the case of the absence of an external electric field, the charge carriers trapped in different localized states show different dipole orientations. An electron can hop between a pair of these centers under the applied AC field, in turn leading to the reorientation of an electric dipole.[34,35] The interface polarization decreases with increasing frequency and approaches a constant value. This is related to the fact that beyond a certain frequency of the external field, electron hopping cannot follow the alternative field.[34,36]

The dispersion of $\sigma_{ac}(\omega)$ with frequency is a common characteristic in nanostructures of disordered heterogeneous materials.[37,38] The AC electrical conductivity (σ_{ac}) is calculated using the following relation:

$$\sigma_{ac} = \omega C \tan\delta\left(\frac{d}{A}\right) = \omega\varepsilon_0\varepsilon'' \tag{8}$$

It is clearly seen in Fig. 7 that the electrical conductivity generally increases with increasing frequency because the polarization decreases with increasing frequency. It is acceptable that the ε' value decreases with decreasing polarization and more carriers are introduced in the structure. An increase in the eddy current caused by the additional charge carriers may be responsible for the

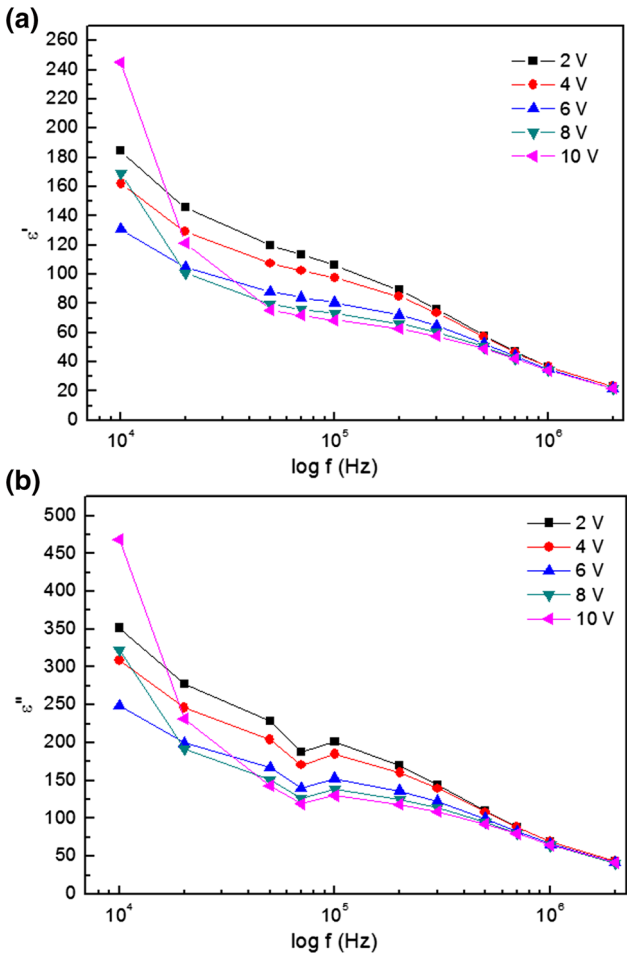

Fig. 5. The frequency and voltage dependent (a) ε' and (b) ε'' for Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

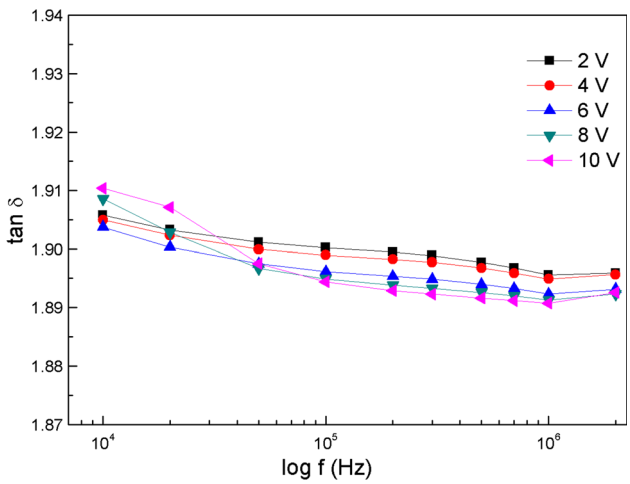

Fig. 6. The curves of tan δ for Au/P3HT:PCBM:F4-TCNQ/n-Si SBD as a function of frequency and voltage.

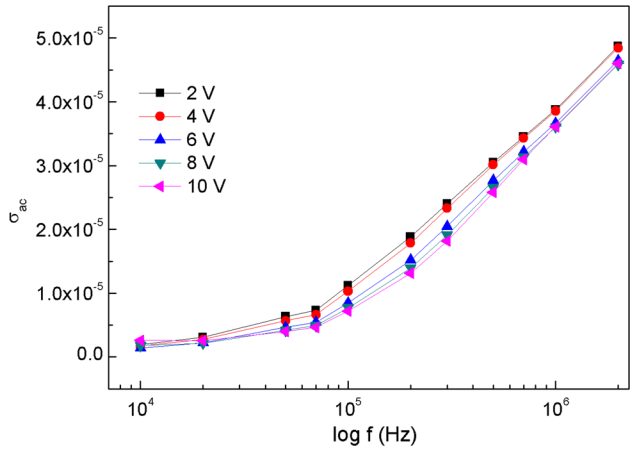

Fig. 7. The frequency and voltage dependent σ_{ac} characteristic of Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

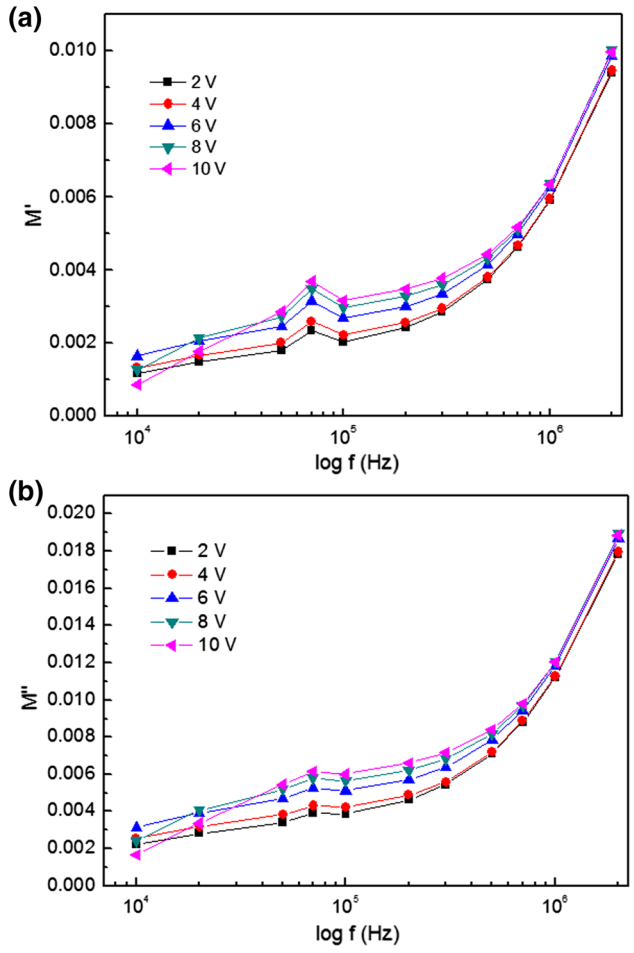

Fig. 8. The frequency and voltage dependent (a) M' and (b) M'' characteristics for Au/P3HT:PCBM:F4-TCNQ/n-Si SBD.

increasing σ_{ac} values with increasing frequency due to the origin of the structure of organic film at M/S interface.

The complex electrical modulus formalism is an alternative approach to analyze the electrical transport process parameters in the structure. It is particularly suitable to extract the phenomena such

as electrode polarization and conductivity relaxation times.[27,39] Complex electric modulus plots attribute more importance to the elements with the smallest capacitance which occur in the dielectric system. A theory for the conductivity relaxation in ion conductors in terms of a dimensionless quantity was introduced by Macedo and co-workers.[40] The complex permittivity ($\varepsilon^* = 1/M^*$) data were transformed into the M^* formalism using the following relation[17,26,29]:

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2} \quad (9)$$

The real (M') and imaginary (M'') components of the electric modulus as a function of frequency at different voltages are shown in Fig. 8. The decrease in ε' and ε'' with increasing frequency causes an increase in M' and M''. Moreover, the dielectric constant going to infinity brings M' closer to zero at low frequencies, suggesting the suppression of the electrode polarization. On the other hand, at high frequencies, M' and M'' display a maximum value corresponding to $M_\infty = 1/\varepsilon_\infty$ due to the relaxation process. This is because the period (T) is much lower than the lifetime (τ) of interface states at high frequencies and N_{ss} cannot follow the ac signal.

CONCLUSION

The present study reports the experimental results on the electrical and dielectric properties of Au/P3HT:PCBM:F4-TCNQ/n-Si SBDs in the frequency range 10 kHz–2 MHz. The values of C and G/ω decrease in the depletion and accumulation region with increasing frequency. The excess capacitance is responsible for the high capacitance values due to the ability of N_{ss} to follow ac signal. It is observed that the interface states are strongly dependent on the frequency and decrease exponentially with increasing frequency. In that case, at sufficiently high frequency limit ($f \geq 500$ kHz), the N_{ss} can hardly follow the ac signal and the contribution of N_{ss} to the total capacitance may be neglected. Also, R_s causes a serious error in the extraction of electrical and dielectric parameters of SBDs from C–V and G/ω–V measurements. Dielectric measurements reveal that the dielectric constant ε' and dielectric loss ε'' decrease with increasing frequency, while the loss tangent $\tan\delta$ remains virtually unchanged. The increase of capacitance and conductance with decreasing frequencies can be understood in respect of the charge storage at traps so that they lead to the decrease of ε' and ε''. At low frequencies all the four types of polarization processes, i.e. the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the values of ε' and ε''. On the other hand, the increase in σ_{ac} with increasing frequency can be explained by the relaxation phenomenon occurring due to mobile charge carriers. The experimental dielectric data were also analyzed by taking electric modulus formalism into account. The value of M' is closer to zero at low frequencies, which is possibly related to a long range mobility of charge carriers. In conclusion, the presence of high-dielectric interfacial organic layer inserted between metal and semiconductor is important as it can be used in a wide range of charges/energy capture and storage applications.

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