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# Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile

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This paper proposes a new model for the subthreshold current and swing of the short-channel symmetric underlap ultrathin double gate metal oxide field effect transistors with a source/drain lateral Gaussian doping profile. The channel potential model already reported earlier has been utilized to formulate the closed form expression for the subthreshold current and swing of the device. The effects of the lateral straggle and geometrical parameters such as the channel length, channel thickness, and oxide thickness on the off current and subthreshold slope have been demonstrated. The devices with source/drain lateral Gaussian doping profiles in the underlap structure are observed to be highly resistant to short channel effects while improving the current drive. The proposed model is validated by comparing the results with the numerical simulation data obtained by using the commercially available ATLAS™, a two-dimensional (2-D) device simulator from SILVACO.

**Key words:** Ultra-shallow junction (USJ), straggle parameter, subthreshold current, subthreshold swing, short-channel effects (SCEs), gate underlap, DG MOSFETs

## INTRODUCTION

Double-gate (DG) metal oxide semiconductor (MOS) structures are the potential candidates for low-power and high speed VLSI applications due to their better immunity to the short-channel effects (SCEs), higher drivability, and better scalability features over the conventional single-gate MOSFETs.[1–5] Further, the use of gate underlap structure in place of the conventional gate overlap region in different MOS structures is reported to provide significant improvement in the circuit level performance due to the reduction in the gate edge direct tunneling leakage[6] and gate sidewall fringe capacitance.[7,8] Moreover, MOSFETs with a lateral Gaussian-doping profile in the source/drain region are reported to provide better flexibility in controlling the on-state drive current of the device.[9] In view of the above, we have recently reported an analytical model for studying the channel potential and threshold voltage characteristics of an ultra-shallow junction (USJ) DG MOSFET structure combined with both the gate underlap and drain/source lateral Gaussian doping features.[12] In this paper, an effort has been made for the first time to analytically model the subthreshold current and subthreshold swing characteristics of the gate Underlap DG MOSFETs with a source/drain lateral Gaussian doping profile as an extension to our work was reported in Ref. 12. The model results have been validated by comparing them with the 2-D numerical simulation data obtained from ATLAS™, a -2D device simulator from Silvaco.[10]

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## THEORETICAL MODELING

### Subthreshold Current Model

The schematic diagram of the Underlap USJ DG MOSFET with a source/drain lateral Gaussian-doping profile used for modeling and simulation of subthreshold current and swing is shown in Fig. 1a.

The $x$ and $y$ axes of the 2-D structure are taken along the front surface and source-channel interface of the channel, respectively. Both the gates are connected together with a common gate-to-source voltage ($V_{GS}$). A Lateral Gaussian-shaped doping profile, say $N_{sd}(x)$, has been used for the ultra-shallow junction (USJ) regions in the channel in the similar manner as in Ref. 9

$$N_{sd}(x) = N_{sdp} e^{\left(\frac{x^2}{2\sigma_L^2}\right)}, \quad (1)$$

where $N_{sdp}$ is the peak Gaussian doping. Figure 1b shows the S/D Gaussian profiles for different values of lateral straggle $\sigma_L$ in the channel. The degenerated doping value has been set at $2.7 \times 10^{19}$ cm$^{-3}$.[9] Since the present work is in continuation to our earlier work reported in Ref. 12, we will use all the device parameters with same nomenclature as in Ref. 12 in the present model. Further, some of the results of Ref. 12 will be directly used for developing the subthreshold swing model of the device as follows. Since the diffusion can be assumed to be the dominant phenomena for the subthreshold current flow mechanism in the MOS device, the subthreshold current of the DG MOSFETs under study can be given as in Ref. 11

$$I_S = \int_0^{tsi} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy, \quad (2)$$

where $D_n$ is the diffusion constant, $L_{eff}$ the effective channel length, $V_{DS}$ the drain to source voltage, $V_T$ the thermal voltage and

$$n_{min}(y) = \frac{n_i^2}{N_a} \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) \quad (3)$$

$$\psi_{VC}(y) = \psi_{s2}(x_{min})\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} y - \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}} y^2\right] + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} (V_{GS} - V_{fb})\left[-y + \frac{y^2}{t_{si}}\right] \quad (4)$$

$n_{min}(y)$ is the carrier concentration at the virtual cathode potential, and $\psi_{VC}(y)$ is the potential at the virtual cathode of the device.[11] By solving $\left.\frac{\partial \psi_{c2}(x)}{\partial x}\right|_{x=x_{min}} = 0$, $x = x_{min}$ (at which $\psi_{c2}(x)$ has the minimum value)[12] is given as $x_{min} = L_{ul} + (\lambda/2) \ln((D/C)_{max})$, where $\psi_{VC}(y_{min}) = \psi_{VC}(y)|_{y=y_{min}}$ is the minimum potential at the virtual cathode; $y_{min}$ is the division point (i.e,. the point at which electric field amends its direction) which can be obtained by solving the following equation:

$$\left.\frac{\partial \psi_{VC}(y)}{\partial x}\right|_{y=y_{min}} = 0 \quad (5)$$

Let us assume that the total channel region $0 \le y \le t_{si}$ in the vertical direction is divided into two regions, namely, the front and back regions corresponding to $0 \le y \le y_{min}$ and $y_{min} \le y \le t_{si}$, respectively. If the subthreshold currents contributed by the front and back regions are denoted by $I_{Sf}$ and $I_{Sb}$, respectively, then the total subthreshold current described by Eq. 2 can be expressed as

$$I_S = I_{Sf} + I_{Sb}, \quad (6)$$

where

$$I_{Sf} = \int_0^{y_{min}} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy \quad (7)$$

and

$$I_{Sb} = \int_{y_{min}}^{t_{si}} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy. \quad (8)$$

Note that the subthreshold currents $I_{Sf}$ and $I_{Sb}$, contributed by the upper and lower channel regions, are controlled by the front gate and back gate of the device, respectively. Following the methodology described in Ref. 11, Eqs. 7 and 8 can be written as

$$I_{Sf} = K\left(\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(0)}{V_T}\right)\right) \quad (9)$$

and

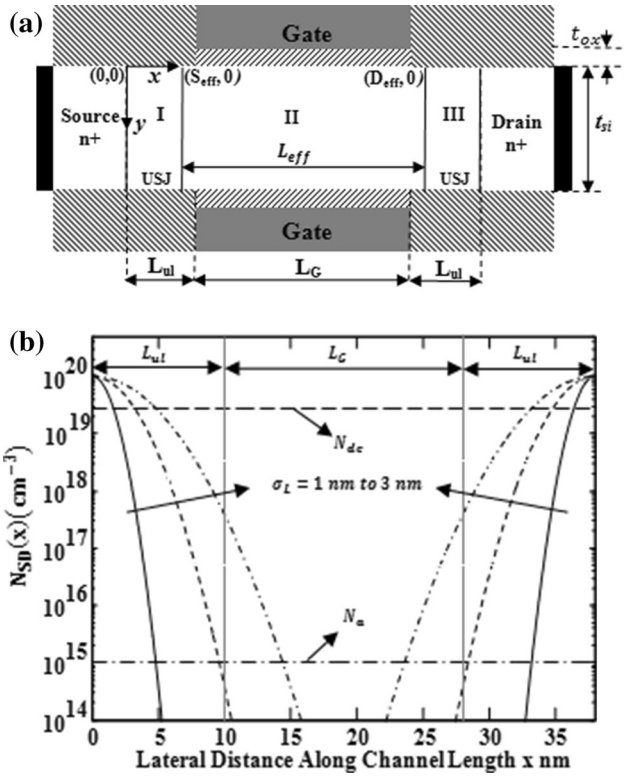


Fig. 1. (a) Schematic view of Underlap DG MOSFET. (b) Lateral doping profile in the source/drain extension region for different values of straggle parameter.

$$I_{Sb} = K\left(\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)\right), \quad (10)$$

where

$$K_f = \frac{qD_n n_i^2 V_T}{E_f N_a L_{eff}}\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

$$K_b = \frac{qD_n n_i^2 V_T}{E_b N_a L_{eff}}\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

$$E_f = \frac{\psi_{VC}(y_{min}) - \psi_{min}(0)}{y_{min} - 0}$$

$$E_b = \frac{\psi_{VC}(y_{min}) - \psi_{min}(t_{si})}{y_{min} - t_{si}}.$$

Note that $E_f$ and $E_b$ are the electric fields associated with the front and back surfaces of the Underlap USJ DG MOSFET structure under consideration. Assuming that $d_{eff,A}$ and $d_{eff,B}$ are the effective conduction path parameters[11] of the front and back regions of the channel, we write

$$d_{eff,A} = \frac{\int_0^{y_{min}} y \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy}{\int_0^{y_{min}} \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy} = \frac{\left(y_{min} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \left(0 - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(0)}{V_T}\right)}{\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(0)}{V_T}\right)} \quad (11)$$

$$d_{eff,B} = \frac{\int_{y_{min}}^{t_{si}} y \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy}{\int_{x_{min}}^{t_{si}} \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy} = \frac{\left(t_{si} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \left(y_{min} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)}{\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)} \quad (12)$$

Now, the effective conduction effect path parameter, $d_{eff}$, can be expressed as in Ref. 11

$$d_{eff} = \frac{I_{Sf}|d_{eff,A}| + I_{Sb}|d_{eff,B}|}{I_S}. \quad (13)$$

## Modeling of Subthreshold Swing

The subthreshold swing (S) can be defined as in Ref. 11

$$S = \left(\frac{\partial \log I_S}{\partial V_{GS}}\right)^{-1}, \quad (14)$$

where $I_S$ is the subthreshold current of the Underlap USJ DG MOSFET under study. In principle, $I_S$ from Eq. 6 can be substituted in Eq. 14 to determine S. Since the subthreshold current $I_S$ is mainly due to the diffusion phenomenon, it can be assumed to be proportional to the carrier concentration $n_{min}(x)$ at the virtual cathode, and; hence, $I_S$ can be expressed as in Ref. 11

$$I_S \propto n_{min}(y) \propto \exp\left(\frac{\psi_{VC}(y)}{V_T}\right). \quad (15)$$

Using Eq. 15 in Eq. 14, we can express S as

$$S = V_T(\ln 10) \times \left(\frac{\partial \psi_{VC}(y)}{\partial V_{GS}}\right)^{-1}. \quad (16)$$

The virtual cathode can be considered as a hypothetical electrode placed at $y = y_{min}$ along the vertical direction of the channel, which has a potential distribution of $\psi_{VC}(y)$ and a carrier distribution of $n_{min}(y)$. Thus, the subthreshold swing becomes a function of $y$, which is undesirable since S is a position-independent device parameter. To make S independent of $y$, we can use the concept of the effective conduction path effect parameter ($d_{eff}$)[11] to obtain the expression of the subthreshold swing as

$$S = \frac{V_T \ln 10}{\left(\left(\frac{c_1(e_1+f_1)}{d_1}\right)+1\right)b_1 + a_1} \quad (17)$$

where,

$$a_1 = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left[-d_{eff} + \frac{d_{eff}^2}{t_{si}}\right]$$

$$b_1 = \left\{1 - \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}\left[-d_{eff} + \frac{d_{eff}^2}{t_{si}}\right]\right\}$$

$$c_1 = \frac{1}{\sqrt{C_{min} D_{min}}}$$

$$d_1 = \frac{4 t_{ox} g h}{\eta\lambda}\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox} h}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)$$

$$e_1 = D_{min}\left(g\left(e^{-L_G/\lambda} - 1\right) - \frac{t_{ox} h}{\eta\lambda}\left(e^{-L_G/\lambda} + 1\right)\right)$$

$$f_1 = C_{min}\left(g\left(1 - e^{L_G/\lambda}\right) - \frac{t_{ox} h}{\eta\lambda}\left(e^{L_G/\lambda} + 1\right)\right).$$

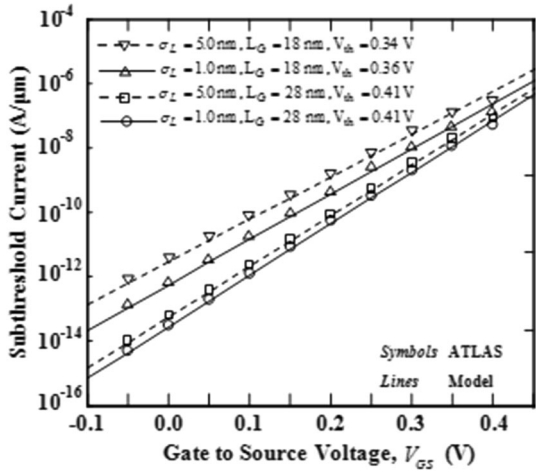


Fig. 2. Subthreshold current versus gate to source voltage. Parameters used: $V_{DS} = 0.05$ V, $L_{ul} = 10$ nm, $t_{si} = 7$ nm, $t_{ox} = 1$ nm.

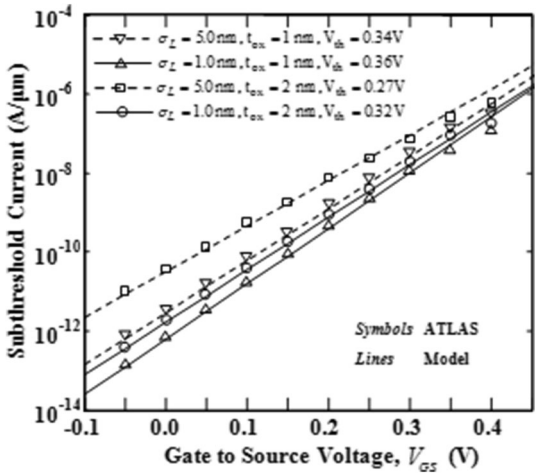


Fig. 3. Subthreshold current versus gate to source voltage. Parameters used: $V_{DS} = 0.05$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $t_{si} = 7$ nm.

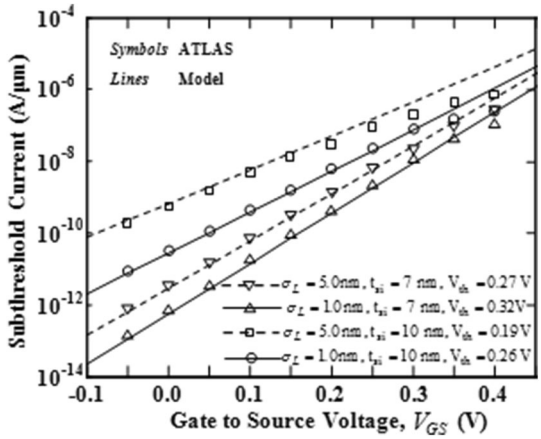


Fig. 4. Subthreshold current versus gate to source voltage. Parameters used: $V_{DS} = 0.05$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $t_{ox} = 1$ nm.

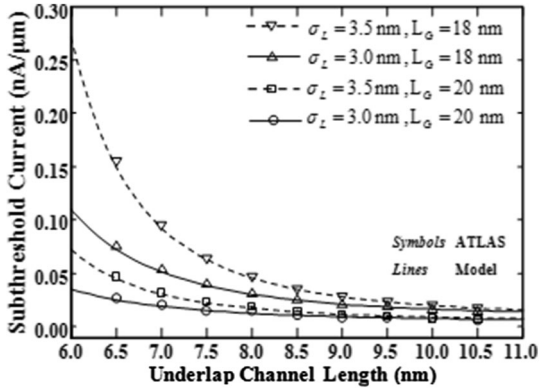


Fig. 5. Subthreshold current versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $t_{si} = 7$ nm, $t_{ox} = 1$ nm.

## RESULTS AND DISCUSSION

In this section, the analytical results of the subthreshold current, ($I_S$) and swing (S) of Underlap DG MOSFETs with a lateral Gaussian doped source/drain calculated from our model have been compared with the numerical simulation results obtained by the 2-D device simulation software ATLAS™. The drift–diffusion (DD) model and Fermi–Dirac statistics have been used for the carrier transport and carrier distribution in the ATLAS simulation. The results have been presented for identical front and back gate structures with the same gate-oxide thicknesses and tungsten (work function $\varphi_M$ = 4.7 eV) as the gate material for both of the gates of the device. Since the present work is in continuation to our previous work reported in Ref. 12, the expression for the threshold voltage derived in Ref. 12 is directly applicable in the present study. Note that the threshold voltage in Ref. 12 has been defined as the gate voltage for which the channel electron density at the minimum surface potential point equals the doping concentration of the channel.

First of all, the variations of the subthreshold current as a function of gate to source voltage for four different combinations of $\sigma_L$ and $L_G$; $\sigma_L$ and $t_{ox}$ and $\sigma_L$ and $t_{si}$ (while keeping the underlap length ($L_{ul}$) and other parameters constant)are shown in Figs. 2–4, respectively. It is observed that the subthreshold current is increased with $\sigma_L$ when other parameters remain unchanged. The increased $\sigma_L$ reduces the effective channel length of the device which, in turn, increases the subthreshold current. Further, for a fixed value of $\sigma_L$, the subthreshold current is increased with the decreased channel length, increased oxide thickness, and increased channel thickness due to increased SCEs as observed in Figs. 2–4, respectively. It is

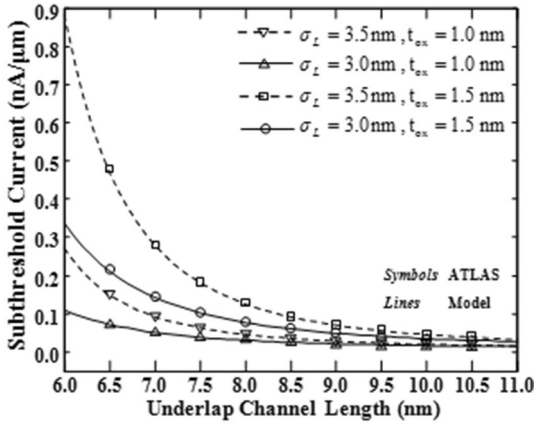


Fig. 6. Subthreshold current versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $t_{si} = 7$ nm, $L_G = 18$ nm.

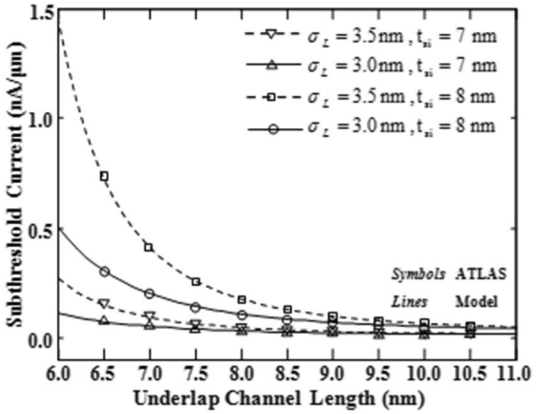


Fig. 7. Subthreshold current versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $L_G = 18$ nm, $t_{ox} = 1$ nm.

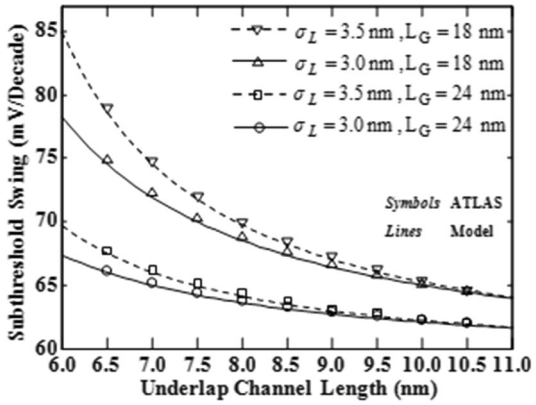


Fig. 8. Subthreshold swing versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $t_{si} = 7$ nm, $t_{ox} = 1$ nm, $V_{GS} = 0.1$ V.

demonstrated in our previous work that[12] the threshold voltage of the device in decreased with the decrease in channel length, increase in channel thickness, and increase in oxide thickness due to

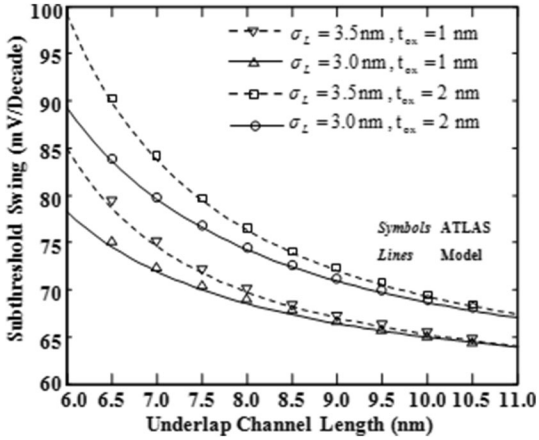


Fig. 9. Subthreshold swing versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $t_{si} = 7$ nm, $V_{GS} = 0.1$ V, $L_G = 18$ nm.

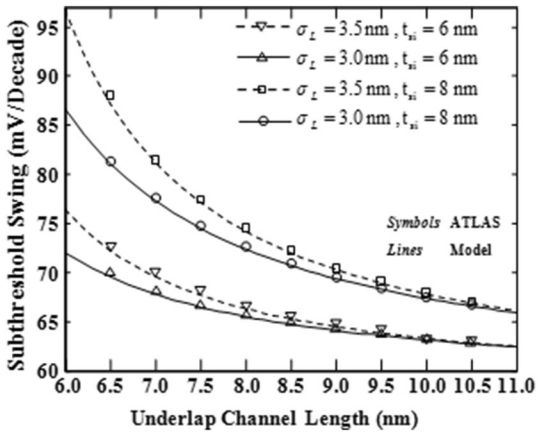


Fig. 10. Subthreshold swing versus underlap channel length. Parameters used: $V_{DS} = 0.05$ V, $t_{ox} = 1$ nm, $V_{GS} = 0.1$ V, $L_G = 18$ nm.

SCEs which, in turn, increases the subthreshold current of the device. From the results of Figs. 2–4, it is observed that the straggle parameter $\sigma_L$ can provide us an additional flexibility of controlling the subthreshold current of the device. The variations of subthreshold current as a function of the gate underlap channel length ($L_{ul}$) for four different combinations of $\sigma_L$ and $L_G$; $\sigma_L$ and $t_{ox}$ and $\sigma_L$ and $t_{si}$ (while keeping other parameters constant) are shown in Figs. 5–7, respectively. The subthreshold leakage current is observed to be decreased with the increase in the gate underlap region due to reduction in the SCEs. However, for fixed values of $L_{ul}$ and $\sigma_L$, the subthreshold current is increased with decreased channel length, increased oxide thickness, and increased channel thickness as demonstrated in Figs. 5–7, respectively. Similarly, it is increased with $\sigma_L$ for a fixed $L_{ul}$ and other device parameters as discussed earlier. It may be mentioned that the reduction in subthreshold current at

the cost of increased $L_{ul}$ must increase the overall size of the transistor under consideration.

Finally, the variations of subthreshold swing as a function of the gate underlap length ($L_{ul}$) for four different combinations of $\sigma_L$ and $L_G$; $\sigma_L$ and $t_{ox}$ and $\sigma_L$ and $t_{si}$ (while keeping other parameters constant) are shown in Figs. 8–10, respectively. It is observed from all the above mentioned figures that the subthreshold swing is increased with $\sigma_L$ similar to the subthreshold current. For fixed values of $\sigma_L$ and $L_{ul}$, the swing also increases with the decrease in the channel length, increase in oxide thickness, and increase in channel thickness due to increased SCEs as observed from Figs. 8–10, respectively.

All the model results have been compared with the ATLAS simulation data presented in Figs. 2–10. The reasonable good matching shows the validity of the proposed model in this paper. The results clearly show that two parameters, namely, $\sigma_L$ and $L_{ul}$ can be used along with other device parameters for optimizing the subthreshold performance characteristics of the device in terms of subthreshold current and subthreshold swing.

## CONCLUSION

In this paper, subthreshold current and swing of the short-channel symmetric underlap ultrathin DG MOSFETs with a lateral source/drain Gaussian doping profile have been proposed. The analytical results have been compared with ATLAS simulation data to validate the proposed model. It is observed that both the subthreshold current and subthreshold swing can be optimized by optimizing the values of gate underlap length ($L_{ul}$) and straggle parameter ($\sigma_L$) of the source/drain Gaussian profile. The general trend of increased subthreshold current and subthreshold swing can be compensated by reducing $\sigma_L$ and/or increasing $L_{ul}$. Thus, the device structure under consideration provides better flexibility for optimization of the subthreshold current and swing characteristics due to two additional parameters $L_{ul}$ and $\sigma_L$ over and above the conventional device parameters of the gate overlap uniformly doped source/drain DG MOSFETs.

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