Journal of ELECTRONIC MATERIALS, Vol. 46, No. 1, 2017
DOI: 10.1007/s11664-016-4841-6
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Effect of Remote Oxygen Scavenging on Electrical Properties of Ge-Based Metal–Oxide–Semiconductor Capacitors

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Remote oxygen scavenging has been studied in a metal/high-*k* dielectric/GeO_2/Ge stack, where a thin Ti layer inserted into the metal/high-*k* dielectric interface serves as the scavenger. First, we established that remote oxygen scavenging indeed occurs specifically in the studied HfO_2/Al_2O_3/GeO_2/Ge stack. It was also established that the source for oxygen is decomposition of the GeO_2 layer. Then, the effect of remote oxygen scavenging of the GeO_2 layer on the electrical characteristics of the metal/oxide/Ge capacitors was investigated. The electrical properties were studied in comparison with identical gate stacks with a Pt electrode, before and after annealing. Although a decrease in effective oxide thickness was demonstrated as a result of this process, clear degradation of the interface electrical quality was observed after scavenging. Initiation of the scavenging process was witnessed upon deposition of Ti at room temperature, emphasizing that this process could not be controlled.

Key words: Ge, high-*k* dielectric, metal–oxide–semiconductor, scavenging

INTRODUCTION

Ongoing dimensional scaling of electronic devices has placed high-mobility substrate metal–oxide–semiconductor (MOS) capacitors at the center of attention in numerous research papers over the last decade. Ge is a leading candidate high-mobility channel material due to its high bulk hole mobility compared with Si and all alternative III–V semiconductors.[1] The first obstacle to overcome in Ge MOS research was passivation of the Ge/high-*k* dielectric interface, since it became clear that direct deposition of high-*k* dielectric onto Ge results in severe electrical degradation attributed to formation of a defective interfacial layer.[2] Numerous methods have been proposed to achieve excellent passivation of the Ge/high-*k* interface.[3–8] It was found that a thin thermally grown GeO_2 layer dramatically decreased the interface trap density, therefore serving as very good passivation for *p*-type Ge.[9,10] Selection of a proper high-*k* dielectric for Ge MOS capacitors was the obvious next challenge. The need for bi- or multilayered dielectric stacks was established[11,12] to obtain both good thermal stability on top of the GeO_2 passivation layer as well as high effective dielectric constant. In our previous paper[13] we showed that, in such complex stacks, even though the high-*k* dielectric is not in direct contact with the Ge surface, it has a significant effect on the density of traps at the interface (D_{it}) and on the density of border traps (D_{bt}), namely traps close to the interface from the high-*k* dielectric side.

In Si/high-*k* MOS capacitors with complex multilayer stacks, one approach to decrease the effective oxide thickness (EOT) is by scavenging of the interface layer (IL) formed between the Si substrate and high-*k* dielectric using a variety of reactive metals.[14–16] In some cases of scavenging,[17,18] it was also reported that removing oxygen from the Si interface can result in mobility degradation and deterioration of the electrical properties of the interface. In our recent work,[19] we studied the reactivity of Ti on top of a Ge-based MOS stack

(Received March 11, 2016; accepted July 29, 2016; published online August 19, 2016)

using synchrotron x-ray photoelectron spectroscopy (XPS). It was found that Ti could serve as a scavenging element also in Ge MOS capacitors. In the studied cases, we saw evidence for complete removal of GeO_2 from the interface after annealing. However, this was studied on GeO_2/Ge and Al_2O_3/GeO_2/Ge stacks, where the insulators have relatively low dielectric constant compared with other high-k dielectrics such as HfO_2 and ZrO_2. More importantly, the effect of the scavenging process on the electrical properties was not addressed. In the current study, we investigate the HfO_2/Al_2O_3/GeO_2/Ge stack structure, which provides effective passivation of the Ge surface, good thermal stability on top of GeO_2 (achieved by using Al_2O_3 as the bottom high-k dielectric), and high effective dielectric constant (achieved by using HfO_2 as the top high-k dielectric). It is important to note that we use a relatively large thickness of the dielectric stack (~8 nm) since the goal is to track and understand changes and processes in the stack rather than achieve state-of-the-art devices in terms of EOT.

In this work, we compare the effect of a thin Ti layer inserted into a Pt electrode on a high-k/GeO_2/Ge stack before and after a forming gas (FG) anneal, to investigate the feasibility of Ti scavenging through this stack. In particular, our goal is to study whether complete or partial removal of GeO_2 is possible with minimal disruption of the passivation of the Ge surface, and to study the effect of scavenging on the electrical properties of the Ge MOS capacitor.

EXPERIMENTAL PROCEDURES

To remove most of the native oxide, 300-mm p-type Ge-on-Si wafers were cleaned for 30 s in dilute (2 wt.%) HF solution. After the HF dip, the Ge surface was reoxidized in a controlled manner to obtain GeO_2 layers ~2 nm thick, as measured by spectroscopic ellipsometry (SE). The oxidation was performed with a direct O_2 plasma at 300°C in an ASM EmerALD 3000 reactor, attached to a Polygon 8300 platform. On top of the GeO_2, ~2-nm Al_2O_3 and ~4-nm HfO_2 layers were deposited by atomic layer deposition (ALD) of trimethylaluminum (TMA)/H_2O and $HfCl_4$/H_2O, respectively. The depositions of the dielectrics were carried out at 300°C in a hot-wall cross-flow ASM Pulsar 3000 reactor, attached to the same Polygon 8300 platform, which made *in situ* transfer feasible. The metals (Ti and Pt) were deposited using e-gun evaporation through a shadow mask to fabricate the gate electrode. The Ti evaporation conditions were carefully chosen to prevent oxidation during the evaporation process. Pt (~40 nm) was deposited immediately after Ti (~3 nm) to protect the Ti from environmental exposure and oxidation. For comparison, Pt (40 nm) only was deposited on another sample. Both samples underwent a forming gas (FG, 90% N_2 + 10% H_2) anneal at 400°C for 30 min.

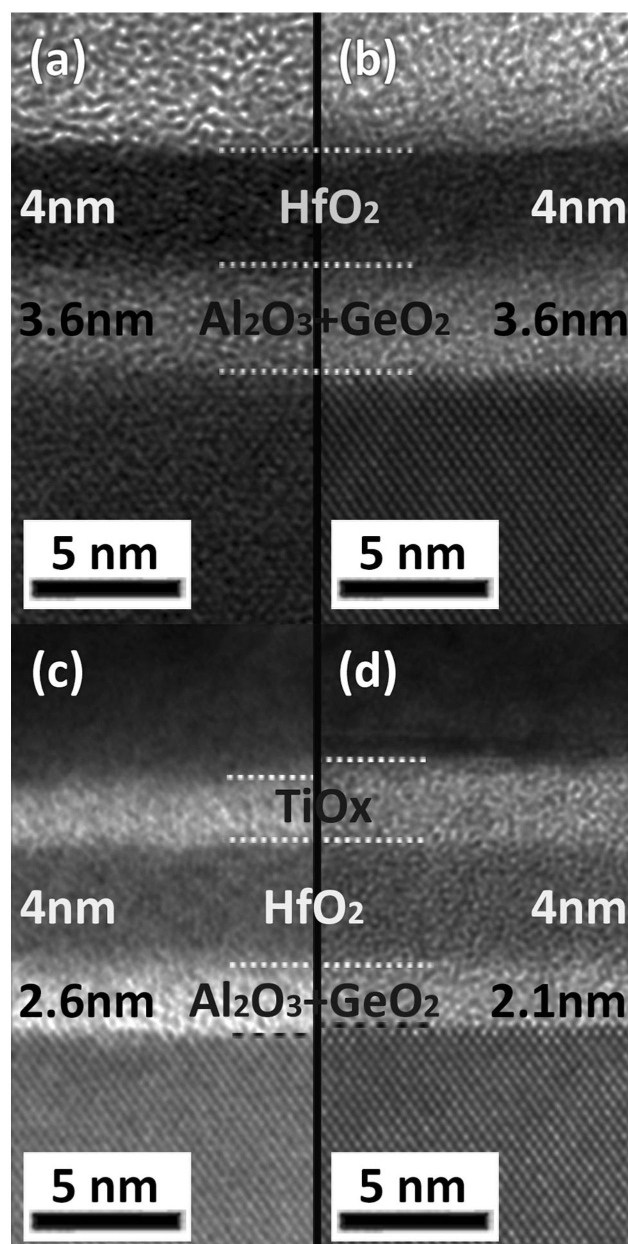

Fig. 1. HRTEM micrographs of the dielectric stack (a) as grown, and (b) after FG anneal, and with Ti/Pt metallization (c) as deposited and (d) after FG anneal. The thicknesses of the dielectric layers are marked for each sample.

All characterizations were done before and after the FG anneal. Electrical measurements were performed at room temperature using a probe station sealed from light. Steady-state capacitance–voltage (C–V) measurements were conducted using an HP4284 LCR meter at various frequencies (10 kHz to 500 kHz). Current–voltage (I–V) measurements were conducted using an Agilent 4155C parametric analyzer. Cross-sectional transmission electron microscopy (TEM) samples were prepared by conventional polishing and examined in a 200-keV FEI Tecnai G2 T20 Twin TEM.

RESULTS AND DISCUSSION

To verify that scavenging occurred in the studied Ti/Pt metallization, the samples were studied by high-resolution transmission electron microscopy (HRTEM) imaging (Fig. 1). First, we compared the dielectric stack before any metal deposition. The stacks were examined before and after FG anneal (Fig. 1a and b, respectively). As discussed in Ref. 13, due to the only slight differences in density and average molecular weight, there is almost no difference in contrast between Al_2O_3 and GeO_2. As can be seen, no change is seen after annealing. The thickness of the dielectric layers remained as before annealing: 4.0 nm for the HfO_2 layer and 3.6 nm for the light-contrast layer (Al_2O_3 + GeO_2). However, the micrographs with Ti/Pt metallization showed several differences (Fig. 1c and d). First, the thickness of the $Al_2O_3 + GeO_2$ reduced from 3.6 nm before metal deposition to 2.6 nm after metal deposition but before annealing (Fig. 1a and c, respectively). After FG anneal, a further reduction in the thickness of this layer (Al_2O_3 + GeO_2) to 2.1 nm was observed (Fig. 1d). In contrast to the reduction in the thickness of the Al_2O_3 + GeO_2 layer, the thickness of the HfO_2 layer remained constant throughout the process. An additional bright-contrast layer was observed on top of the HfO_2 layer after deposition of the Ti/Pt electrode (Fig. 1c), and its thickness increased after FG anneal (Fig. 1d). This increase along with the decrease in the thickness of Al_2O_3 + GeO_2 suggests that scavenging of GeO_2 occurred in our studied stack, and that the additional light-contrast layer on top of HfO_2 is Ti undergoing oxidation. Another important observation from the TEM micrographs is that HfO_2 is not the source for oxygen in this redox reaction, since its thickness remained constant. Rangan et al.[20] also demonstrated scavenging of GeO_2 through HfO_2, but in that case Al served as the reactive metal, and no TEM results supported this assumption.

Due to the similar bright contrast of Al_2O_3 and GeO_2, one may wonder if indeed the GeO_2 decomposes or perhaps the oxygen involved in the Ti oxidation originates from the Al_2O_3 layer. In Ref. 19, we reported a similar process on an Al_2O_3/GeO_2/Ge stack, with no change in the Al_2O_3 layer observed by TEM or chemical bonding (XPS) analyses. Table I presents the possible chemical reactions for oxidization of Ti at the expense of any oxide in our studied system, and the change in the Gibbs free energy for each reaction at room temperature and at 400°C.[21] The chemical reactions present the formation of TiO_2 or Ti_2O_3, based on our previous findings on Ti scavenging in Al_2O_3/GeO_2/Ge stacks,[19] where we observed formation of these oxides under similar conditions. No thermodynamic driving force exists for decomposition of Al_2O_3 or HfO_2 to form TiO_2 or Ti_2O_3 at the studied temperatures. However decomposition of GeO_2 to form any of the Ti oxides is thermodynamically favorable, even at room temperature.

High-frequency (500 kHz) *C–V* curves of the samples before and after FG anneal are shown in Fig. 2. In this figure, the capacitance is normalized to the capacitor area, after verifying that the capacitance showed no dependence on area. The *C–V* curve for the Pt sample (empty symbols) after FG anneal shows a steeper depletion slope in comparison with the as-deposited Pt sample, due to elimination of interface traps, as expected. A small shift in the flat-band voltage (V_{fb}) of 0.2 V towards lower gate bias is also expected, since radiation damage caused by the e-gun deposition is repaired during annealing.[22] The fact that the accumulation capacitance of the Pt sample did not change after annealing indicates no change in the thicknesses of the dielectric films during annealing. Several differences are revealed when the *C–V* curves of the Pt sample are compared with those of the Ti/Pt sample (full symbols). Already upon metal deposition, the accumulation capacitance is significantly higher for the Ti/Pt sample, even though the Ti/Pt was deposited on the same dielectric stack as the Pt. After FG annealing, the accumulation capacitance is further increased. These increases may be a result of a reduction in the thickness of one or more of the dielectric layers, which might be accompanied by addition of a higher-*k* dielectric to the as-deposited stack. Considering the low value of the dielectric constant of GeO_2[1] and the high dielectric constant value of Ti oxides,[23] scavenging of GeO_2 and addition of TiO_2 to the dielectric stack can explain the change in the accumulation capacitance. EOT values were

Table I. Change in Gibbs free energy for possible oxidation reactions of Ti[21]

Reaction	ΔG (kJ/mol) at 298 K	ΔG (kJ/mol) at 673 K
$Ti + GeO_2 \rightarrow TiO_2 + Ge$	−367	−372
$Ti + \frac{3}{4}GeO_2 \rightarrow \frac{1}{2}Ti_2O_3 + \frac{3}{4}Ge$	−280	−224
$Ti + \frac{1}{2}Al_2O_3 \rightarrow Ti_2O_3 + Al$	166	157
$Ti + \frac{2}{3}Al_2O_3 \rightarrow TiO_2 + \frac{4}{3}Al$	120	173
$Ti + HfO_2 \rightarrow TiO_2 + Hf$	198	194
$Ti + \frac{3}{4}HfO_2 \rightarrow \frac{1}{2}Ti_2O_3 + \frac{3}{4}Hf$	97	96

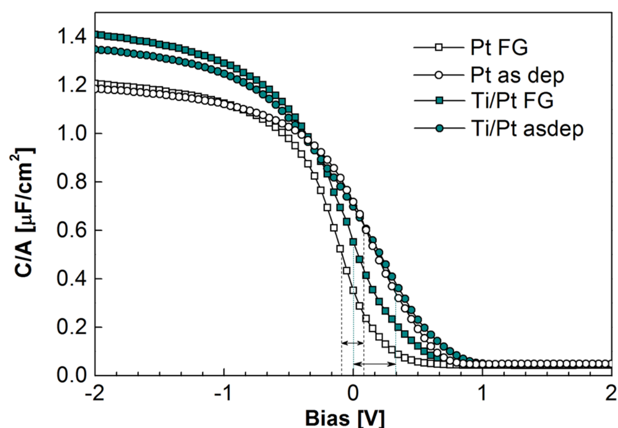

Fig. 2. *C–V* curves at 500 kHz for the Pt sample (empty symbols) and Ti/Pt sample (full symbols) before and after FG anneal. Vertical dashed lines mark V_{fb} for each curve.

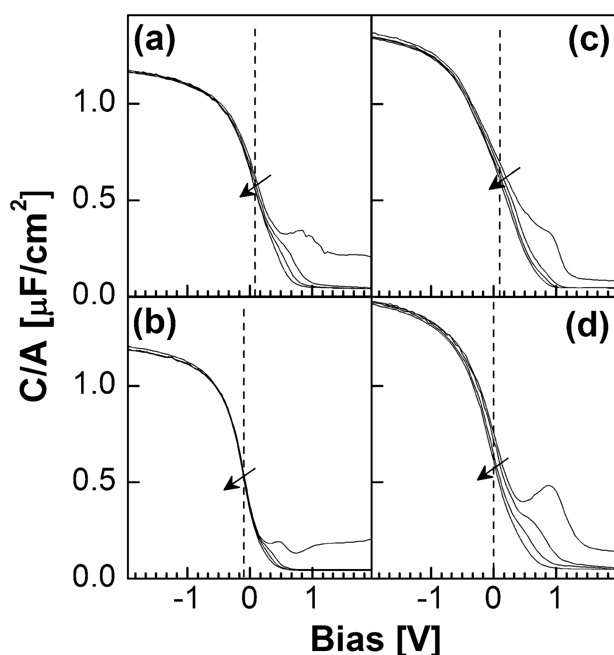

Fig. 3. *C–V–F* results for the samples: (a) as-deposited Pt, (b) FG-annealed Pt, (c) as-deposited Ti/Pt, and (d) FG-annealed Ti/Pt. Dashed lines mark V_{fb} for each sample. Black arrows indicate increasing measurement frequency from 20 kHz to 500 kHz.

calculated from the high-frequency *C–V* results. The initial EOT of 2.9 nm calculated for the Pt sample was reduced for the Ti/Pt sample upon deposition to 2.6 nm. A further reduction to 2.4 nm was observed after annealing of the Ti/Pt sample. As mentioned previously, the absolute values of the EOT do not reflect those needed for realization of state-of-the-art devices, but the significant reduction of EOT can be utilized for such devices.

To study the effect of scavenging on the interface trap density, *C–V* curves were measured at various frequencies (*C–V–F*) for all samples in the range from 20 kHz to 500 kHz (Fig. 3). The dispersions in the accumulation capacitance (C_{acc}) and in the depletion capacitance at $V = V_{fb}$ (marked C_{fb}) are directly connected to the border and interface trap densities, respectively.[24–26] The calculated dispersion values are summarized in Table II. All samples show quite low values of dispersion in C_{acc} (1% to 3%), indicating low density of border traps and consequently high quality of the dielectric films. Before annealing, both samples showed roughly the same values of dispersion in C_{fb}. For the Pt sample, the dispersion in C_{fb} was significantly improved after FG anneal, due to passivation of interface traps, as expected.[27] However, this was not the case

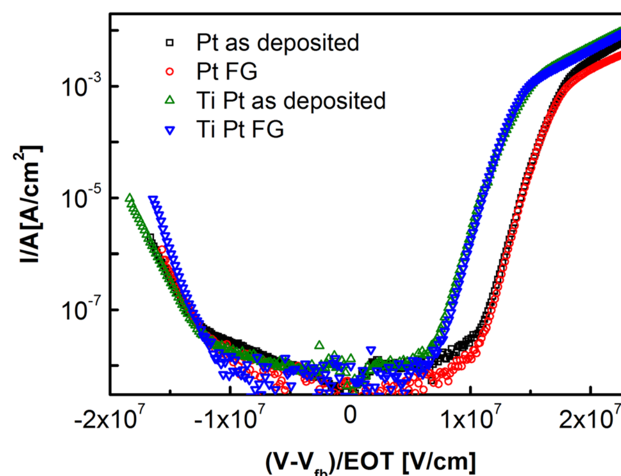

Fig. 4. *I–V* curves as a function of gate bias relative to V_{fb} for all samples, presented in both positive bias (inversion) and negative bias (accumulation).

Table II. Dispersion of capacitance in accumulation and flat-band voltage for all samples before and after FG anneal

Sample	Dispersion in C_{acc} (%)	Dispersion in C_{fb} (%)
Pt as deposited	0.6	11.7
Pt FG	1.3	4.5
Ti/Pt as deposited	1.0	13.0
Ti/Pt FG	1.5	24.0

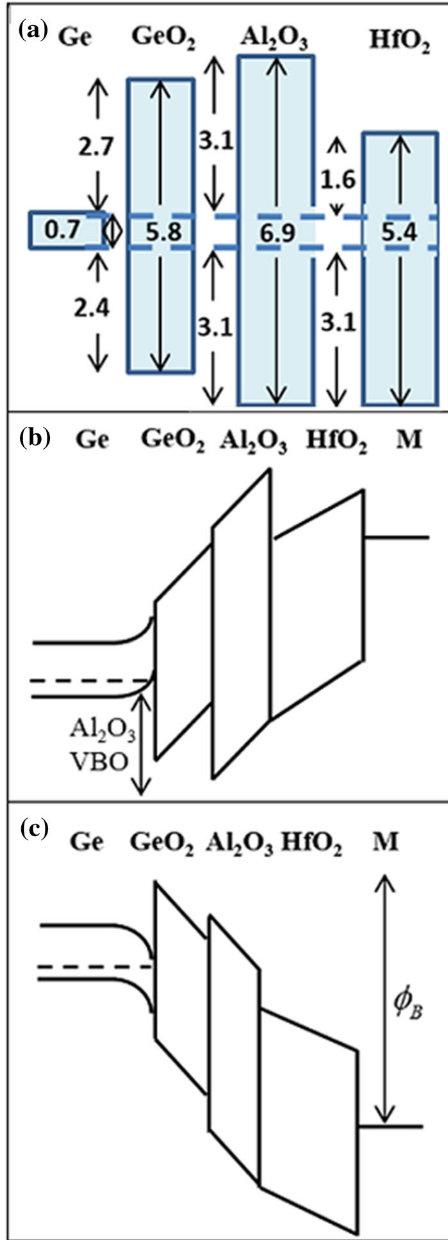

Fig. 5. Schematic band diagram of the studied system: (a) at flat band with the measured values of band alignment, (b) under negative bias (accumulation), and (c) under positive bias (inversion).

for the Ti/Pt sample: the C_{fb} dispersion increased substantially after FG anneal, which is an indication of deterioration of the Ge interface and an increase of D_{it}. A similar result was obtained when the hump at the weak inversion regime was analyzed[28] (C–V at the low frequency, 20 kHz). It is clear that, while for the Pt sample the hump area decreased after the FG anneal due to a lower D_{it}, an increase in the hump area was observed after annealing the Ti/Pt sample.

To further confirm this analysis of the C–V–F results, D_{it} was calculated using a simulation.[29,30] The D_{it} value around the Ge Fermi level (which in our case is located 0.18 eV above the valence-band edge) is $2 \times 10^{12}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$ for the as-deposited samples. In the case of the Pt sample, this value drops after FG annealing to $9 \times 10^{11}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$, and rises to $2.5 \times 10^{12}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$ in the case of the Ti/Pt sample post FG annealing. This result is in agreement with previous works. In his work, Ando[18] presented reliability and mobility degradation as a result of interface roughening after scavenging, which was probably accompanied by an increase in D_{it}. In our case, the increase in D_{it} is probably a result of new dangling bonds of Ge formed when oxygen is depleted from the interface.

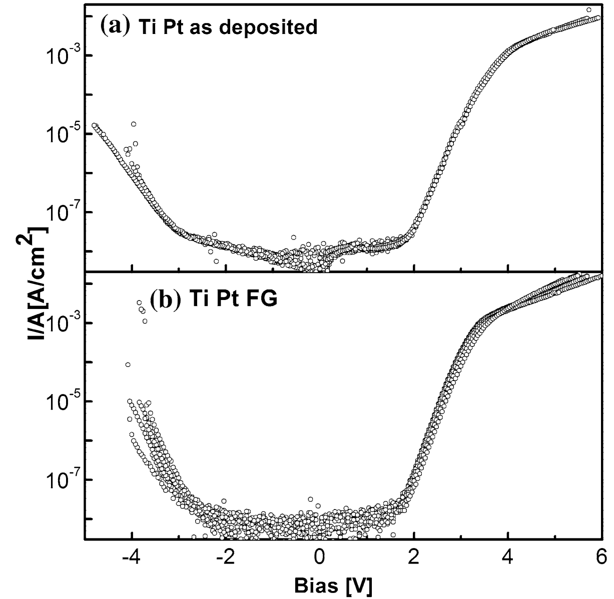

Fig. 6. I–V curves for the Ti/Pt sample (a) as deposited and (b) after FG anneal. For both samples, multiple capacitors were measured, showing repeatability in the measurement for the as-deposited sample but variance between capacitors for the annealed sample.

Typical I–V curves for the samples before and after FG anneal are shown in Fig. 4. To correctly analyze the I–V measurements, we used the band alignment of the as-deposited studied system[13,31] and the band diagram under each polarity (Fig. 5). The gate bias is normalized in Fig. 4 to the EOT, meaning that the leakage current is presented as a function of the effective electric field. Under negative bias, a significant increase in leakage current is achieved, at roughly the same effective field for all samples. The level of the leakage current for high negative bias is similar for the as-deposited samples, but a small increase of the leakage current is shown for the Ti/Pt sample after annealing, with a slightly different slope. This change might indicate a change in the conduction mechanism after scavenging. Since we observed an increase in D_{it} after scavenging, the change in the current density–electric field (J–E) slope may be related to additional leakage through trap-assisted tunneling.

In his review of scaling through scavenging, Ando showed[16] that, when the leakage current is plotted

relative to EOT, the current density is lower after scavenging. However, this was reported for an Si substrate and an La capping layer. During that scavenging process, La diffused to the Si interface and formed a silicate, acting as an additional barrier to leakage. Taking into consideration that no decrease of the leakage current was observed after scavenging in our case, it can be inferred that the additional TiO_x layer on top of the HfO_2 in the Ti/Pt sample does not serve as a barrier to leakage current under negative bias.

Under positive bias, the Pt sample showed significant leakage current only for effective electric field higher than that of the Ti/Pt sample. No significant difference was visible for each of the metal electrodes before and after annealing. In this case, the capacitor is in inversion (Fig. 5c), and the current is mainly dominated by transport of electrons from the Ge to the metal electrode. Since the conduction-band offset of Al_2O_3 with respect to Ge defines the barrier to electron transport,[13] and under the assumption that no change occurs in the Al_2O_3 layer during the scavenging process, it is fair to assume that this barrier remains intact. Therefore, the difference in current (for positive bias) between the Pt sample and the Ti/Pt sample shown in Fig. 4 must be due to the change of the metal electrode. If we assume a Fowler–Nordheim tunneling mechanism, the current is also dependent on the band bending of the dielectric. Significant current is possible only for band bending larger than the barrier to electrons from the side of the metal (ϕ_B). Since ϕ_B is directly dependent on the metal work function, the shift shown in Fig. 4 may be evidence for a metal with a different work function in each sample's gate governing this barrier. The difference between the onset of the leakage current of the Pt sample and the Ti/Pt sample is in agreement with this hypothesis when the values of the vacuum work functions of Ti and Pt are considered (4.3 eV and 5.6 eV, respectively[32]). The fact that this difference remains constant also after annealing may indicate the presence of Ti in metallic form at the interface with the dielectric stack, meaning that Ti is not completely oxidized even after the FG anneal. This is possible when the available oxygen in the system is deficient. Deficiency of oxygen was also observed in our previous paper,[19] where due to this deficiency Ti formed both the thermodynamically stable TiO_2 and the metastable Ti_2O_3.

Another interesting phenomenon is observed for the Ti/Pt sample. When the *I–V* curves of several capacitors are plotted together (Fig. 6), a clear variation is shown between the measurements of the various capacitors after the FG anneal (Fig. 6b). This variation highlights a loss of uniformity between capacitors and may be related to trapping and detrapping of carriers during the measurement.[33,34] Since this variation does not occur for the as-deposited sample (Fig. 6a), it is fair to assume that it is also a result of additional traps at the interface after annealing, due to the scavenging effect. Another possible explanation is that scavenging is not uniform, and in some of the capacitors there is still a GeO_2 layer. It should be noted that this phenomenon is not observed for the annealed Pt sample (not shown).

CONCLUSIONS

The electrical properties of a Pt/high-k/GeO_2/Ge MOS stack were studied after a scavenging process initiated by addition of a thin Ti layer at the dielectric–metal interface. We show in this paper that scavenging of the GeO_2 passivation layer starts already at room temperature and continues after FG annealing. It was found that, although Ti oxidation along with removal of the low-k GeO_2 causes an increase in the capacitance and can be utilized to scale down Ge MOS devices, the effect on the electrical properties is destructive. We observed an increase in D_{it} as well as degradation in the leakage current after the scavenging process. It was also found that this reaction cannot be controlled or avoided, since it starts at room temperature and continues after annealing. This is in contrary to scavenging in Si-based MOS stacks, where there is no thermodynamic driving force for decomposition of SiO_2 at room temperature, hence the scavenging process can be controlled.

ACKNOWLEDGEMENTS

This work was supported by the Russell Berrie Nanotechnology Institute at the Technion. The authors thank Mr. A. Shay for his assistance and expertise with e-gun deposition and Dr. F. Palumbo for his help with analysis of *I–V* measurements.

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