Journal of ELECTRONIC MATERIALS, Vol. 45, No. 11, 2016
DOI: 10.1007/s11664-016-4760-6
© 2016 The Minerals, Metals & Materials Society

CrossMark

# Investigation of Leakage Current Mechanisms in $La_2O_3/SiO_2$/4H-SiC MOS Capacitors with Varied $SiO_2$ Thickness

YUCHENG WANG,[1] RENXU JIA,[1,3] YANLI ZHAO,[2] CHENGZHAN LI,[2] and YUMING ZHANG[1]

1.—School of Microelectronics, Xidian University, Xi'an 710071, China. 2.—Zhuzhou CSR Times Electric Co., Ltd., Zhuzhou, China. 3.—e-mail: rxjia@mail.xidian.edu.cn

In this study, the material and electrical properties of $La_2O_3/SiO_2$/4H-SiC metal–oxide–semiconductor (MOS) capacitors are systematically characterized. Thermal oxidization $SiO_2$ with varying thickness (0 nm, 3.36 nm, 5 nm, 8 nm, and 30 nm) were coated with $La_2O_3$ using atomic layer deposition on $n$-type 4H-SiC. The stacking oxides were measured using atomic force microscopy, transmission electron microscopy, and x-ray photoelectron spectroscopy, and the MOS capacitors were measured by capacitance–voltage and current–voltage measurements. The results demonstrate that the main gate current leakage mechanisms are dependent on the thickness of the $SiO_2$ oxide under the applied electric field. The primary mechanism for current leakage from the $La_2O_3$/4H-SiC MOS capacitor follows the Schottky emission mechanism due to its low conduction band offset. In contrast, the current leakage mechanism for the capacitor with a 3.36 nm $SiO_2$ layer follows the Poole–Frenkel emission mechanism on account of its high trap charge density in the gate dielectric and at the interface. When the thickness of the $SiO_2$ layer increases to 8 nm, lower leakage current is observed by reason of the low trap charge density and high conduction band offset when $E \leq 5$ MV/cm. As the electric field strength increases to 5 MV/cm and 5.88 MV/cm (30 nm $SiO_2$: 4.8 MV/cm), the main current leakage mechanism changes to the Fowler–Nordheim tunneling mechanism, which indicates that the $La_2O_3/SiO_2$ stacking structure can improve the properties of MOS capacitors.

**Key words:** $La_2O_3$, 4H-SiC, x-ray photoelectron spectroscopy, current leakage mechanism

## INTRODUCTION

Silicon carbide (SiC) has been the focus of a wide range of studies over the past several years due to its superior electrical properties (wide band gap, high thermal conductivity, high critical breakdown field, and high saturated electron velocity).[1–4] The quality and reliability of the gate insulators generally determine the overall efficiency of SiC metal–oxide–semiconductor field-effect transistor (MOSFET) devices.[5–7] According to Gauss's law, the most frequently used dielectric, $SiO_2$ ($e$ = 3.9), is subjected to electric fields higher than 5 MV/cm in the SiC MOS devices at higher applied voltages.

In order to reduce the electric field for the gate oxide, various high-$\kappa$ materials with large band gaps, large conduction, valence band offsets, good thermodynamic stabilities, and high crystallization temperatures have been used as potential gate dielectric materials. Recently, high-$\kappa$ dielectric materials such as $Al_2O_3$[8,9] $HfO_2$[10,11] $TiO_2$[12] $Y_2O_3$[13] and $La_2O_3$[14] have attracted a considerable amount of interest in this field. In particular, $La_2O_3$ has proved to be a promising high-$\boldsymbol{\kappa}$ gate insulator with a large $\kappa$-value of approximately 30 and a high crystallization temperature of 1100°C.[15,16] Depositing $Al_2O_3$ as the capping layer on the $La_2O_3$ films[17,18] and introducing an

(Received December 20, 2015; accepted June 17, 2016; published online July 11, 2016)

ultrathin $SiO_2$ interfacial layer between 4H-SiC and the high-$\kappa$ gate dielectrics can effectively reduce moisture absorption and help overcome the problem of low conduction band offsets for the high-$\kappa$/4H-SiC structure. Although there are many previous works about the material and electrical properties of the stacking oxide on 4H-SiC, such as $Al_2O_3/SiO_2$/4H-SiC,[8] $La_2O_3/SiO_2$/4H-SiC[16] C. M. Hsu had made a deep analysis for the gate leakage current mechanisms of the $HfO_2/SiO_2$/4H-SiC structure 11, but fewer studies have clearly analyzed the mechanisms of gate current leakage of the $La_2O_3/SiO_2$/4H-SiC structure, which are particularly important for the MOS capacitor based on $La_2O_3/SiO_2$ stacking structure. In this study, the gate current leakage mechanisms of $La_2O_3/SiO_2$/4H-SiC MOS capacitors are systematically studied.

## EXPERIMENTAL DETAILS

*N-type*, *Si-faced*, 4° off (0001) oriented, 4H-SiC substrates with a 10 $\mu$m thick epilayer (doping level of $8 \times 10^{15}$ cm$^{-3}$) were purchased from CREE, Inc. (USA) and used to fabricate the Ni/$La_2O_3/SiO_2$/4H-SiC MOS capacitors. Prior to dielectric deposition, a conventional Radio Corporation of America (RCA) clean was performed. Oxide layers with varying thicknesses were grown on the 4H-SiC wafers by adjusting the thermal oxidation time at pure oxide ambient. Using La(iPrCp)$_3$ (ris Lanthanum) and TMA (trimethylaluminium) as the La and Al precursor while $O_{3T}$ was used as the oxidant, $La_2O_3$ and $Al_2O_3$ were deposited by atomic layer deposition (ALD) at 300°C for most MOS capacitors (except the thickest $SiO_2$ one). The thickness of the $SiO_2$ layer for each capacitor measured by spectroscopic ellipsometry was found to be 0 nm (#1), 3.3 nm (#2), 5 nm (#3), 8 nm (#4), and 30 nm (#5), respectively, while the thickness of $La_2O_3$ was 16 nm. The $Al_2O_3$ capping layer was deposited on the $La_2O_3$ film to suppress any effects from moisture absorption. Nickel was employed as the gate electrode and the back contact at 100 W direct current (DC) power and $6.6 \times 10^{-4}$ kPa Ar ambient by magnetron sputtering.

The surface quality of each sample was characterized by Keysight 5500 atomic force microscopy (AFM), while the interface quality was determined with transmission electron microscopy (TEM) from Evan Analytical Group Company. The bonding structures and band offsets of $La_2O_3/SiO_2$/4H-SiC

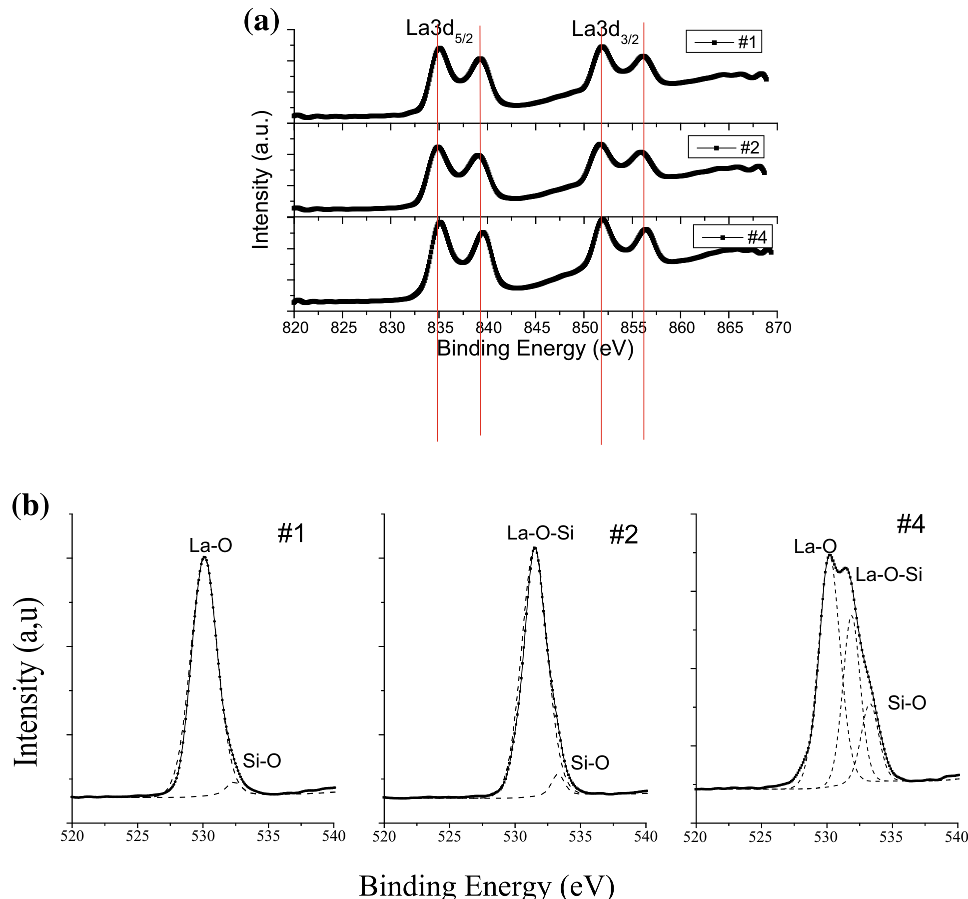


Fig. 1. Photoelectron spectra of (a) La3d in the $La_2O_3$ films and (b) O1 s in the $La_2O_3$/4H-SiC (#1) and $La_2O_3/SiO_2$ (#2 and #4) interfacial layer.

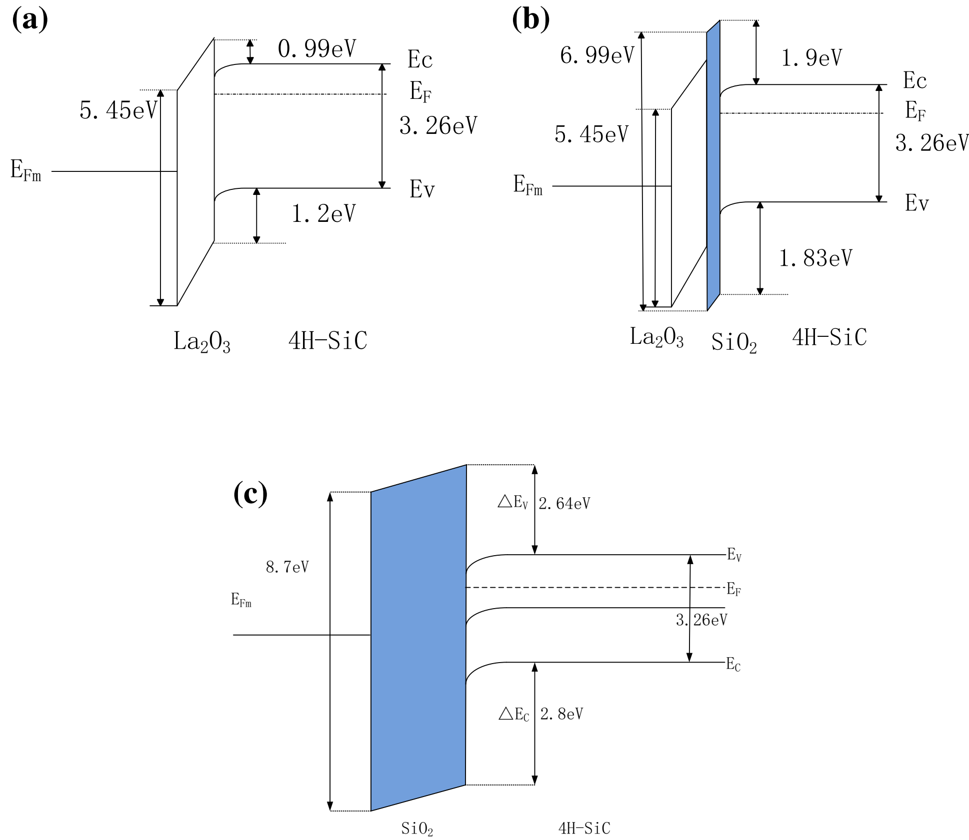


Fig. 2. The schematic band alignments for the (a) $La_2O_3$/4H-SiC (b) $La_2O_3$/$SiO_2$ (8 nm)/4H-SiC and (c) $SiO_2$/4H-SiC systems with positive voltage polarity on the Ni electrode.

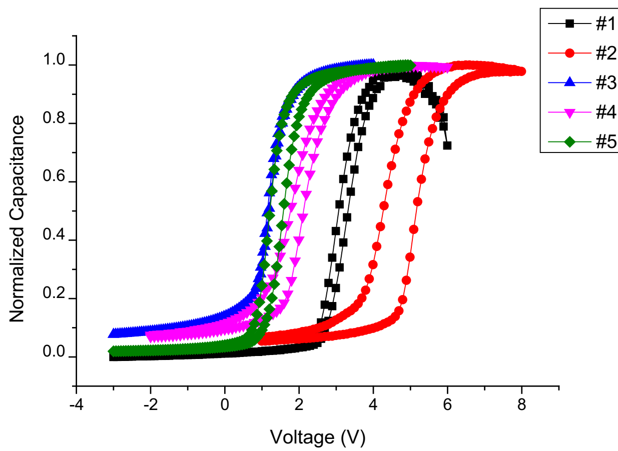


Fig. 3. Capacitance–voltage (C–V) characteristics of MOS capacitors with samples #1–#5.

were characterized using K-α x-ray photoelectron spectroscopy (XPS) from Thermo Electron Corporation. Performed with Al Kα emission at 1486.6 eV, XPS spectra were observed at the constant pass energy of C1 s 284.6 eV on the surface and C1 s 282.8 eV in the 4H-SiC layer. The films were etched 3 nm every time until the 4H-SiC substrate was reached. Electrical analysis of the dielectrics was performed by 100 kHz capacitance–voltage (C–V) measurements with a computer-controlled Keithley 590 C–V analyzer. After the nickel electrode was deposited, current–voltage (I–V) measurements of the MOS capacitors were conducted using HP4156B Semiconductor Parameter Analyzer.

## RESULTS AND DISCUSSION

Figure S1 presents the AFM images for all samples with a scanning area of $5 \times 5\ \mu m^2$. It was found that the surface roughness (RMS) values of all the samples were relatively small, indicating the formation of a smooth surface film. The TEM image in Fig. S2 reveals the structure of $Al_2O_3$/$La_2O_3$/$SiO_2$/4H-SiC (sample #4) with a clear boundary.

The La3d and O1 s core-level spectra of the varied $SiO_2$ thicknesses in $Al_2O_3$/$La_2O_3$/$SiO_2$/4H-SiC structure are shown in Fig. 1. The La3d spectra with four peaks corresponding to binding energies of 834.88 eV, 839.08 eV, 851.78 eV, and 855.98 eV can be attributed to the spin-orbital splitting of oxidized La($3d_{3/2}$) and La($3d_{5/2}$) in Fig. 1a.[19] Figure 1b exhibits the O1 s peaks at the interfacial layers ($La_2O_3$/$SiO_2$ or $La_2O_3$/4H-SiC) for each sample, while the corresponding binding energies are 529.88 eV (La-O), 531.5 ± 1 eV (La-O-Si), and 532.98 ± 0.3 eV (Si-O).[20] No OH-La and La-Si bonds exist,

**Table I. The relevant parameters for all samples**

| Sample | #1 | #2 | #3 | #4 | #5 |
|---|---|---|---|---|---|
| $C_{ox}$ ($10^{-9}$ F) | 3.01 | 2.46 | 2.02 | 1.65 | 0.75 |
| EOT (nm) | 8.1 | 9.91 | 12.1 | 14.77 | 29.1 |
| $N_t$ ($10^{11}$ cm$^{-2}$) | 3.85 | 12 | 0.36 | 3.3 | 1.95 |
| $N_f$ ($10^{12}$ cm$^{-2}$) | 3.6 | 4.4 | 0.023 | 0.96 | 0.29 |

demonstrating that the samples are of good quality. It was found that the intensity of Si-O bond (sample #2 with 3.3 nm $SiO_2$) was quite small, indicating that a thin $SiO_2$ layer will be totally interacting with $La_2O_3$.

The valence and conduction band offsets for high-$\kappa$/4H-SiC structures can be determined using the following Eq. 1a and 1b.[15]

$$\Delta \mathrm{Ev} = E_{\mathrm{VBM}}^{\mathrm{Dielectric_layer}} - E_{\mathrm{VBM}}^{\mathrm{SiC}}, \quad (1a)$$

$$\Delta \mathrm{Ec} = E_g(\mathrm{Dielectric_layer}) - \Delta \mathrm{Ev} - E_g(\mathrm{4H\text{ - }SiC}), \quad (1b)$$

where ΔEv is the valence band offset, $E_{\mathrm{VBM}}^{\mathrm{Dielectric_layer}}$ is the valence band maximum (VBM) for the pure dielectric layer, $E_{\mathrm{VBM}}^{\mathrm{SiC}}$ is the VBM for bulk 4H-SiC, $E_g$(Dielectric_layer) is the band gap of the dielectric layer, and $E_g$(4H - SiC) is the band gap of 4H-SiC, which is assumed to be 3.26 eV. The O1 s core level energy loss spectra of $La_2O_3$ (#1) and $SiO_2$ (#4 and #5) are shown in Fig. S3a. The fitted values for $La_2O_3$ (5.45 eV) and $SiO_2$ (6.99 eV) are much smaller than the literature value due to the intermixing of $La_2O_3/SiO_2$/4H-SiC structures.[21] The valence band (VB) for 4H-SiC, the VBM for the bulk $La_2O_3$ of $La_2O_3$/4H-SiC, and bulk $SiO_2$ of $SiO_2$/4H-SiC are shown in Fig S3b, respectively.

The values of conduction band offset for $La_2O_3$/4H-SiC (#1) and $SiO_2$/4H-SiC (#5) are calculated to be 0.99 eV and 2.64 eV, while for $La_2O_3/SiO_2$/4H-SiC (#4), the values for $La_2O_3$/4H-SiC and $SiO_2$/4H-SiC are 0.62 eV and 1.5 eV, respectively. Based on the results, diagrams illustrating the energy band alignment for the $La_2O_3$/4H-SiC, $La_2O_3/SiO_2$ (8 nm)/4H-SiC, and $SiO_2$/4H-SiC systems with positive voltage polarity on Ni electrode are shown in Fig. 2. It is observed that a thin $SiO_2$ layer intermediate layer can effectively increase band barriers and promote resistance against electron climbing over the substance.

Figure 3 illustrates the normalized C–V curves for each sample. The density of trap charge ($N_t$) and fixed oxide charge ($N_f$) values are obtained by following Eq. 2a and 2b.

$$N_t = \frac{C_{\mathrm{ox}}(V_{\mathrm{FBback}} - V_{\mathrm{FBforward}})}{\mathrm{qA}}, \quad (2a)$$

$$N_f = \frac{C_{\mathrm{ox}}(V_{\mathrm{FBfoward}} - V_{\mathrm{FBideal}})}{\mathrm{qA}}, \quad (2b)$$

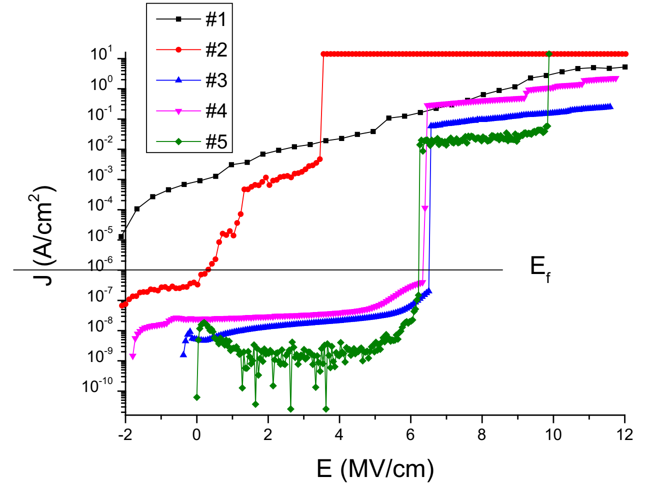


Fig. 4. Current density(J)-electric field(E) plots for samples #1–#5, $E_f$ is defined at the point when current reaches $10^{-6}$ A/cm$^2$.

where $C_{ox}$ is the accumulation capacitance. $V_{FBforward}$, $V_{FBback}$, and $V_{FBideal}$ are the flatband voltages of the forward scanning, back scanning, and ideal curves, respectively. Additionally, $q$ is the electronic charge and $A$ is the gate electrode area ($7.065 \times 10^{-3}$ cm$^2$). The relevant parameters for each sample are presented in Table I.

The values of $N_t$ ($1.2 \times 10^{12}$ cm$^{-2}$) and $N_f$ ($4.4 \times 10^{11}$ cm$^{-2}$) for sample #2 are the largest due to the La silicate material generated by the interaction between the $La_2O_3$ layer and the thin $SiO_2$ (3.3 nm). The values of $N_t$ ($3.85 \times 10^{11}$ cm$^{-2}$) and $N_f$ ($3.6 \times 10^{11}$ cm$^{-2}$) for sample #1 are also quite high owing to the possible reason being the high interface state density, while a rapid decrease in the capacitance is observed in the accumulation region because of the severe leakage current at higher positive voltages, which is attributed to the low band offsets for the $La_2O_3$/4H-SiC structure. Samples #3 are revealed to have low values of charge density, indicating that the stacking of $La_2O_3$ layers on thicker layers of $SiO_2$ (5 nm) can improve interfacial characteristics. With longer time of oxidation, the trap density is improved on account of the increase of the carbon cluster.[22]

The I–V of the MOS capacitors at room temperature can be transformed into the current density–electric field (J–E) using Equations Sa to c. The calculated equivalent oxide thickness (EOT) of all

Table II. Summary of the onset electric fields of conduction mechanisms for the investigated oxides

| $La_2O_3$ stacked with different oxide thicknesses (nm) | The initial electric field of the conduction mechanism | | | | | |
|---|---|---|---|---|---|---|
| | Breakdown electric field (MV/cm) | Fowler–Nordheim tunneling (MV/cm) | Schottky emission (MV/cm) | Poole–Frenkel emission (MV/cm) | Ohm's law (V) | Child's law (V) |
| 0 | – | 5 | 0.1 | 0.6 | – | – |
| 3.3 | 0.1 | 3.45 | 1.3 | 0.6 | 0.606 | 1.49 |
| 5 | 6.5 | 5.88 | – | – | 1.284 | – |
| 8 | 6.3 | 5 | – | – | – | – |
| 30 | 6.15 | 4.8 | – | – | 0.135 | – |

the samples are given in Table I. The J–E plots measured for samples #1–#5 are shown in Fig. 4; the breakdown electric field is defined at the point when current reaches $10^{-6}$ A/cm$^2$.[23] The leakage current density of sample #1 is $10^{-3}$ A/cm$^2$ when a low gate voltage is applied on account of its high charge density and low band offsets. The various charge conduction mechanisms, such as Fowler–Nordheim (F–N) tunneling, Schottky emission (SE), Poole–Frenkel (P–F) emission, and space charge limit (including Ohm's law, and Child's law) mechanisms are also considered here. J–E curves are done using a mathematical method for the linearity curves. The fitting relationships for the three types of charge conduction mechanisms are shown in Table SI. The conduction band offset can be calculated by determining the slope of the F–N tunneling fitting curves, which is defined using the Eq. 3.

$$S = -\frac{4\sqrt{2m^*}}{3\hbar q}\Phi_B^{\frac{3}{2}}, \quad (3)$$

where $m^*$ is the electron effective mass, $\Phi_B$ is the conduction band offset, $S$ is the slope of the F–N tunneling fitting curves, and $\hbar$ is the reduced Planck constant. For sample #1 ($La_2O_3$/4H-SiC), the $m^*$ of $La_2O_3$ is 0.26 $m_0$, the value of the slope is 29.1, and the conduction band offset is 0.89 eV. This value is similar to the value obtained by XPS measurements (0.99 eV).

The leakage current mechanisms' fitting curves of all samples are given in Fig. S4a–f. The data reveal that SE and PF mechanisms at low electric field, and FN mechanisms at high electric field, match the previous paper.[24,25] Table II exhibits the summary of the onset electric fields or voltage of conduction mechanisms for the investigated MOS capacitors. The SE mechanism is the main leakage current mechanism for sample #1, when the electric field starts at 0.1 MV/cm due to its low conduction band offset, which is reported by a previous study,[24] while P–F emission is the main leakage current mechanisms for sample #2 at the electric field of 0.35 MV/cm by reason of its high trap charge density. As the thickness of $SiO_2$ increases, the electric field for samples #3 and #4, where F–N mechanism is predominant, is 5.88 and 4.5 MV/cm, which is higher than sample #5, proving the $La_2O_3$/$SiO_2$ stacking structure can improve the proprieties of MOS capacitors.

## CONCLUSION

In summary, the gate leakage mechanisms of $La_2O_3$/$SiO_2$/4H-SiC MOS capacitors have been systematically studied. $La_2O_3$ gate dielectrics and different thicknesses of $SiO_2$ (0-, 3.36 nm, 5 nm, 8 nm, and 30 nm) were stacked on $n$-type 4H-SiC by thermal oxidization and atomic layer deposition. The main mechanism for gate current leakage was studied for three kinds of samples. The main

current leakage mechanism of the $La_2O_3$/4H-SiC MOS is the Schottky emission (SE) due to its low conduction band offset. However, the current leakage mechanism for a sample with a $SiO_2$ layer thickness at 3.3 nm is the Poole–Frenkel (P–F) emission, resulting from high trap charge density in the gate dielectric and at the interface. As the thickness of the $SiO_2$ layer reaches 5 and 8 nm, lower leakage current is observed by reason of the low trap charge density and high conduction band offset when $E \leq 5$MV/cm. As the electric field strength increases to 5 MV/cm and 5.88 MV/cm (30 nm $SiO_2$: 4.8 MV/cm), the main current leakage mechanism is dominated by the F–N mechanism, proving the $La_2O_3/SiO_2$ stacking structure can improve the proprieties of MOS capacitors.

## ACKNOWLEDGEMENTS

Authors would like to acknowledge that this work is supported by the National Natural Science Foundation of China (Grant No. 51272202 and No. 51472196).

## ELECTRONIC SUPPLEMENTARY MATERIAL

The online version of this article (doi:10.1007/s11664-016-4760-6) contains supplementary material, which is available to authorized users.

## REFERENCES

1. R.H. Kikuchi and K. Kita, *Appl. Phys. Lett.* 105, 032106 (2014).
2. A.F. Basile, A.C. Ahyi, L.C. Feldman, J.R. Williams, and P.M. Mooney, *J. Appl. Phys.* 115, 034502 (2014).
3. P. Fiorenza, F. Giannazzo, A. Frazzetto, and F. Roccaforte, *J. Appl. Phys.* 112, 084501 (2012).
4. Q.W. Song, Y.M. Zhang, Y.M. Zhang, Q. Zhang, and H.L. Lü, *Chin. Phys. B* 19, 087202 (2010).
5. X. Shen, S. Dhar, and S.T. Pantelides, *Appl. Phys. Lett.* 106, 143504 (2015).
6. A. Chanthaphan, T. Hosoi, Y. Nakano, T. Nakamura, T. Shimura, and H. Watanabe, *Appl. Phys. Lett.* 104, 122105 (2014).
7. X.Y. Yang, B.M. Lee, and V. Misra, *IEEE Electron. Dev. Lett.* 36, 312 (2015).
8. X.Y. Tang, Q.W. Song, Y.M. Zhang, Y.M. Zhang, R.X. Jia, H.L. Lv, and Y.H. Wang, *Chin. Phys. B* 21, 087701 (2012).
9. S.S. Suvanam, K. Gulbinas, M. Usman, M.K. Linnarson, D.M. Martin, J. Linnros, V. Grivickas, and A. Hallén, *J. Appl. Phys.* 117, 105309 (2015).
10. A. Tselev, V.K. Sangwan, D. Jariwala, T.J. Marks, L.J. Lauhon, M.C. Hersam, and S.V. Kalinin, *Appl. Phys. Lett.* 103, 243105 (2013).
11. C.M. Hsu and J.G. Hwu, *Appl. Phys. Lett.* 101, 253517 (2012).
12. S. Alialy, Ş. Altındal, E.E. Tanrıkulu, and D.E. Yıldız, *J. Appl. Phys.* 116, 083709 (2014).
13. H.J. Quah, W.F. Lim, S.C. Wimbush, Z. Lockman, and K.Y. Cheong, *Electrochem. Solid-State Lett.* 13, 396 (2010).
14. Y.C. Wang, R.X. Jia, C.Z. Li, and Y.M. Zhang, *AIP Adv.* 5, 087166 (2015).
15. X.Y. Yang, B.M. Lee, and V. Misra, *Mater. Sci. Forum* 778, 557 (2014).
16. J.H. Moon, K.Y. Cheong, D.I. Eom, H.K. Song, J.H. Yim, J.H. Lee, H.J. Na, W. Bahng, N.K. Kim, and H.J. Kim, *Mater. Sci. Forum* 556, 643 (2007).
17. Y. Zhao, K. Kita, and A. Toriumi, *Appl. Phys. Lett.* 96, 242901 (2010).
18. Y. Kim, S. Woo, H. Kim, J. Lee, H. Lee, and H. Jeon, *J. Mater. Res.* 25, 1898 (2010).
19. H. Wong, H. Iwai, K. Kakushima, B.L. Yang, and P.K. Chu, *J. Electrochem. Soc.* 157, G49 (2010).
20. Y. Yang, C.G. Jin, L.J. Zhuge, H.Y. Zhang, Z.F. Wu, and X.M. Wu, *J. Phys. D* 46, 505312 (2013).
21. R. Mahapatra, A.K. Chakraborty, A.B. Horsfall, N.G. Wright, G. Beamson, and K.S. Coleman, *Appl. Phys. Lett.* 92, 042904 (2008).
22. Y.C. Wang, Y.M. Zhang, and R.X. Jia, *Mater. Sci. Forum* 858, 689 (2016).
23. K.Y. Cheong, J.H. Moon, T.J. Park, J.H. Kim, C.S. Hwang, and H.J. Kim, *IEEE. Trans. Electron. Dev.* 54, 3409 (2007).
24. K.Y. Cheong, J.H. Moon, H.J. Kim, W. Bahng, and N.K. Kim, *J. Appl. Phys.* 103, 084113 (2008).
25. I.Y.K. Chang and J.Y.M. Lee, *Appl. Phys. Lett.* 93, 223503 (2008).