Journal of ELECTRONIC MATERIALS, Vol. 45, No. 7, 2016
DOI: 10.1007/s11664-016-4490-9

Effects of Annealing on Electrical Characteristics and Current Transport Mechanisms of the Y/*p*-GaN Schottky Diode

V. RAJAGOPAL REDDY,[1,3] B. ASHA,[1] and CHEL-JONG CHOI[2]

1.—Department of Physics, Sri Venkateswara University, Tirupati 517 502, India. 2.—School of Semiconductor and Chemical Engineering, Semiconductor Physics Research Center (SPRC), Chonbuk National University, Jeonju 561-756, Republic of Korea. 3.—e-mail: reddy_vrg@rediffmail.com

This study investigates the effects of annealing on the electrical properties and current transport mechanism of Y/*p*-GaN Schottky barrier diodes (SBDs). We found no significant change in the surface morphology of the Y Schottky contacts during the annealing process. The Schottky barrier height (SBH) of the as-deposited Y/*p*-GaN SBD was estimated to be 0.95 eV (*I*–*V*)/1.19 eV (*C*–*V*). The SBH increased upon annealing at 400°C and 500°C, and then decreased slightly with annealing at 600°C. Thus the maximum SBH of the Y/*p*-GaN SBD was achieved at 500°C, with values of 1.01 eV (*I*–*V*)/1.29 eV (*C*–*V*). In addition, the SBH values were estimated by Cheung's, Norde, and Ψ_s-*V* plots and were found to be in good agreement with one another. Series resistance (R_S) values were also calculated by *I*–*V*, Cheung's, and Norde functions at different annealing temperatures. Results showing a decrease in the interface state density of the SBD with annealing at 500°C, followed by a slight increase upon annealing at 600°C. The forward-bias current transport mechanism of SBD was investigated by the log*I*–log*V* plot at different annealing temperatures. Our investigations revealed that the Poole–Frenkel emission mechanism dominated the reverse leakage current in Y/*p*-GaN SBD at all annealing temperatures.

Key words: Yttrium Schottky contacts, *p*-GaN, electrical properties, annealing, interface state density, current transport mechanisms

INTRODUCTION

Group III–V nitride semiconductor materials have garnered significant interest among researchers for the development of various high-performance devices. Gallium nitride (GaN), in particular, has shown considerable potential for optoelectronic and high-power electronic device applications including blue light-emitting diodes, blue lasers, ultraviolet Schottky barrier photodetectors, solar-blend Schottky photodiodes, metal–semiconductor field-effect transistors (MSFETs), heterostructure field-effect transistors (HFETs), and high-electron-mobility transistors (HEMTs).[1–9] For the fabrication of such devices, reliable and well-controlled contacts are essential. Metal–semiconductor (MS) rectifying contacts, which are used extensively in electronic devices, thus require low leakage current and high barrier height for the successful production of GaN-based devices. Considerable effort has been focused on the analysis of the electrical properties of different metals/*p*-GaN Schottky diodes[10,11] to improve device performance. Studies have shown that Mg-doped GaN layers grown on a sapphire substrate contain high densities of deep-level defects, originating from the low activation efficiency of Mg–H complexes.[12] Thus the development of stable Schottky contacts on *p*-GaN with low leakage current and high barrier height is essential for achieving high-performance *p*-GaN-based devices.

(Received May 23, 2015; accepted March 22, 2016; published online April 12, 2016)

A few studies have explored different metal schemes for the fabrication of Schottky contacts on *p*-type GaN.[13–22] Kim et al.[18], for example, investigated the electrical properties of a Ti/Al/*p*-GaN Schottky barrier diode (SBD), and reported barrier heights of 1.43 eV at 300 K and 1.41 eV at 500 K using capacitance–voltage (*C*–*V*) measurements at 1.5 kHz. Fukushima et al.[19] constructed rare-earth metal (Dy, Er, Gd) Schottky contacts to *p*-GaN and studied their electrical properties with the use of current–voltage (*I*–*V*) and *C*–*V* measurement techniques. They reported SBH of 1.91 eV, 2.38 eV, and 2.16 eV from *I*–*V* and 1.79 eV, 1.78 eV, and 2.16 eV from *C*–*V* for Dy, Er, and Gd contacts, respectively. Greco et al.[20] studied the electrical and structural properties of the Au/Ni/*p*-GaN SBD upon thermal treatment, and electrical results were correlated with the interfacial microstructure of the annealed contacts for different models. Jang et al.[21] constructed a non-alloyed Ti/*p*-GaN SBD and studied its electrical properties over a temperature range of 293–443 K. They analyzed the *I*–*V* characteristics of the Ti/*p*-GaN SBD in terms of thermionic field emission (TFE) theory, which were confirmed by the thermally increased ideality factor and high tunneling parameter. Choi et al.[22] recently fabricated Ti, Cu, Ni, and Pt Schottky diodes on surface states at semipolar *p*-GaN, and reported an S-parameter of semipolar *p*-GaN of close to zero, indicating that the surface Fermi level was almost perfectly pinned due to the presence of a high density of deep-level defects.

In this work, our primary objective was to fabricate and investigate the electrical properties and current transport mechanism of yttrium Schottky contacts on *p*-type GaN as a function of annealing temperature. Previous studies of such characteristics in *p*-GaN Schottky diodes are limited. Yttrium (Y) was selected because of its low work function (3.1 eV) and unlikeliness of band lineup, i.e., a negative barrier for *n*-type or a barrier over E_g for *p*-type contacts. To the best of our knowledge, no studies to date have explored a Y metal scheme for Schottky contacts on *p*-GaN, and there are no reports on the electrical properties and current transport mechanism of Y/*p*-GaN SBDs at different annealing temperatures. In this work, therefore, using current–voltage (*I*–*V*), capacitance–voltage (*C*–*V*), and Cheung's and Norde functions, we calculate the barrier height (Φ_b), ideality factor (n), interface state density (N_{SS}), and series resistance (R_S) at different annealing temperatures, and compare these values with one another. We also describe and discuss the feasible forward and reverse current transport mechanisms of the Y/*p*-GaN SBD at the various annealing temperatures.

EXPERIMENTAL DETAILS

Mg-doped 1.5-μm-thick *p*-GaN films were grown on c-plane sapphire substrate (0001) by metal-organic chemical vapor deposition (MOCVD). The carrier concentration was estimated at 1.13×10^{17} cm^{-3} by means of Hall measurements. First, the *p*-GaN films were ultrasonically degreased with warm organic solvents including acetone, methanol, and ethanol for 5 min in each step. The GaN films were then dipped in a buffered oxide etch (BOE) solution for 10 min to remove the surface oxide, and were rinsed in deionized (DI) water. Standard photolithography and lift-off techniques were used to define contact electrodes. For ohmic contact, Ni (50 nm)/Au (100 nm) metal films were deposited on the cleaned GaN surface, followed by annealing at 750°C in a nitrogen atmosphere for 1 min. To form a Schottky contact, 50-nm-thick Y film was deposited by electron beam evaporation under a vacuum of 7×10^6 Torr. The area of the Y/*p*-GaN Schottky diode was 3.14×10^{-4} cm^{-2}. To study thermal stability, the diodes were sequentially annealed at 400°C, 500°C, and 600°C for 1 min in a nitrogen atmosphere. Current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) characteristics of the Y/*p*-GaN Schottky diodes were measured using a precision semiconductor parameter analyzer and a precision inductance (L), capacitance (C), and resistance (R) (LCR) meter (model nos. 4156C and 4284A; Agilent Technologies, Santa Clara, CA, USA), respectively, at room temperature. In addition, atomic force microscopy (AFM) (model no: MOD-1M plus, make: Nano focus; operating mode: non-contact, tip size <10 nm) was performed to characterize the surface morphology of the Y/*p*-GaN SBD at different annealing temperatures.

RESULTS AND DISCUSSION

The surface condition of the metal films on the semiconductor plays a significant role in determining the electrical properties of the device. The surface roughness of the Y Schottky contacts was measured by AFM, and the AFM images at different annealing temperatures are shown in Fig. 1. For the as-deposited Y Schottky contact, the surface morphology was fairly smooth, with root-mean-square (RMS) roughness of 2.030 nm, as shown Fig. 1a. However, with annealing at 400°C, RMS roughness increased to 4.112 nm (Fig. 1b). For the contacts annealed at 500°C and 600°C (Fig. 1c and d), the surface morphology was further degraded, with RMS roughness of 4.923 nm and 5.565 nm, respectively. Results indicated no significant change in surface morphology of the Y Schottky contacts during the thermal annealing process.

The semi-logarithmic forward and reverse current–voltage (*I*–*V*) characteristics of the Y/*p*-GaN SBDs at different annealing temperatures are shown in Fig. 2 (the schematic diagram of the Schottky diode including Schottky and ohmic patterns is shown in the inset). The leakage current of the as-deposited Y/*p*-GaN SBD was 2.4528×10^{-12} A at 1 V. For the contacts annealed at 400°C, the leakage current decreased slightly, to 1.7548×10^{-12}

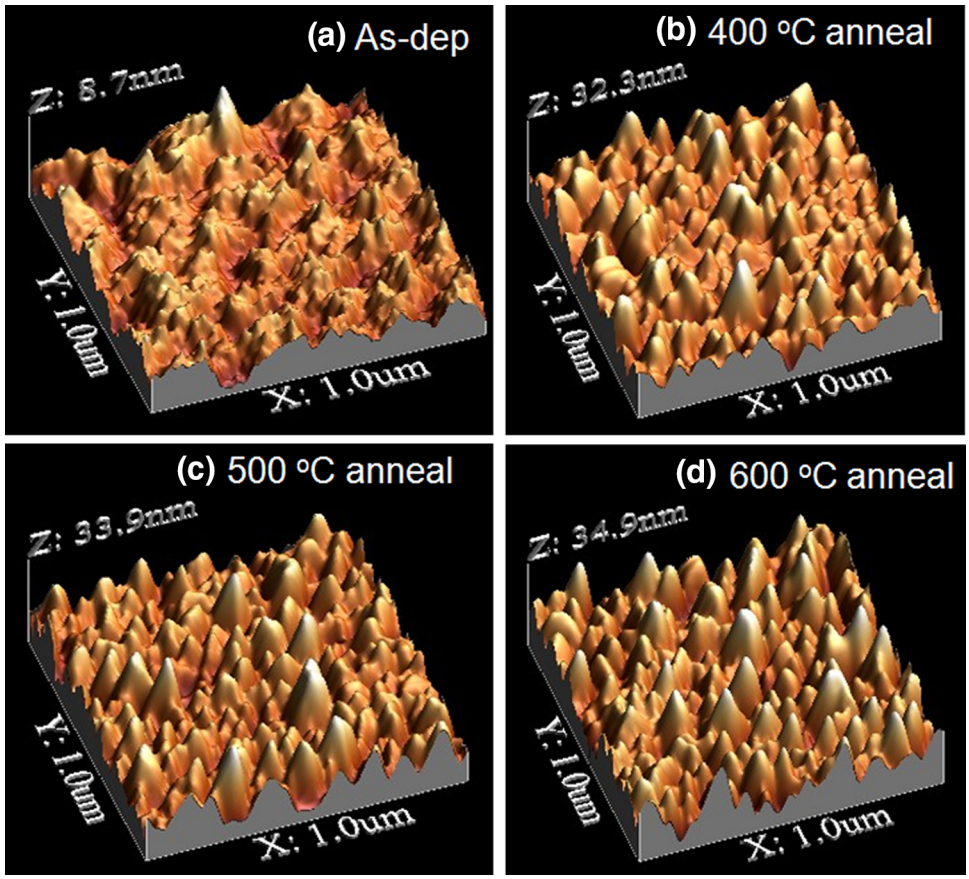

Fig. 1. AFM images of the Y/*p*-GaN SBD at various annealing temperatures.

A. The measured leakage current was further decreased to 1.1245×10^{-12} A at 1 V after annealing at 500°C. However, increasing the annealing temperature to 600°C resulted in a slight increase in leakage current, to 4.1410×10^{-12} A, at 1 V. The electrical properties of the Y/*p*-GaN SBD were improved with annealing at 500°C. The current through an SBD with series resistance (R_S) at a forward bias ($V \geq 3kT/q$) based on the thermionic emission (TE) theory can be expressed as[23]

$$I = I_0 \exp\left[\frac{q(V - IR_S)}{nkT}\right]\left\{1 - \exp\left[\frac{-q(V - IR_S)}{kT}\right]\right\} \quad (1)$$

Here,

$$I_0 = AA^*T^2 \exp\left[\frac{-q\Phi_b}{kT}\right] \quad (2)$$

where I is the current, V is the biased voltage, q is the elementary charge, n is the ideality factor, k is the Boltzmann constant, R_S is the series resistance of the diode, T is the absolute temperature of the diode, Φ_b is the zero-bias barrier height, A^* is the effective Richardson constant (~96 A cm^{-2} K^{-2} for $m_e^* = 0.8\, m_0$), and A is the diode area. The saturation current I_0 values were obtained by extrapolation of the linear region of the semi-logarithmic forward I–V curves to zero applied voltage, and were used to calculate the Schottky barrier height (SBH). The ideality factor n was estimated from the slope of the linear region of the forward-bias ln$I$–V curve, where

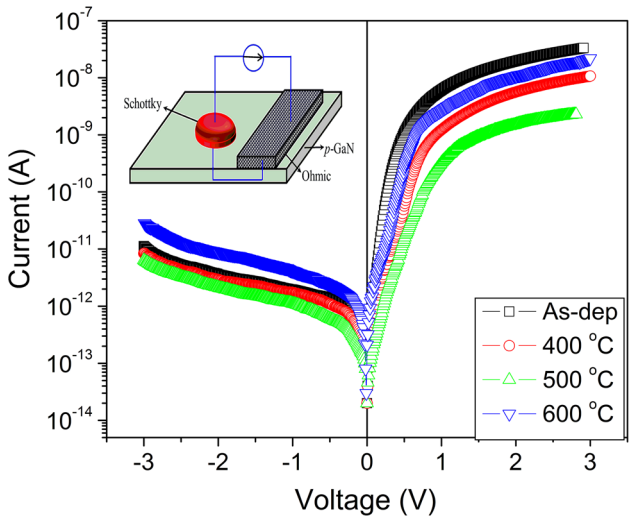

Fig. 2. Current–voltage (*I*–*V*) characteristics of the Y/*p*-GaN SBD at various annealing temperatures. The inset shows a cross-sectional view of the V/*p*-GaN SBD.

the series resistance is small. The SBH values of the SBDs as-deposited and annealed at 400°C were 0.95 eV and 0.98 eV, respectively. With annealing at 500°C, the estimated SBH of the Y/*p*-GaN SBD was 1.01 eV, and this value decreased slightly, to 0.96 eV, after annealing at 600°C. These experimental results show that maximum SBH was achieved with annealing at 500°C, with a slight decrease after annealing at 600°C. Thus the optimal annealing temperature for the Y/*p*-GaN SBD was 500°C. The ideality factors of the as-deposited Y/*p*-GaN SBD and with annealing at 400°C were 1.64 and 1.33, respectively. However, the ideality factor improved to 1.21 when the Y/*p*-GaN SBD was annealed at 500°C. Annealing at 600°C led to a slight increase in the ideality factor, to 1.53. The experimental results thus showed an ideality factor of greater than 1.0 for the Y/*p*-GaN SBD for all contacts. This may be largely ascribed to the particular distribution of interface states.[24] Other possible mechanisms include image force effect, recombination generation, and tunneling. The presence of a wide distribution of low SBH patches caused by laterally inhomogeneous BH at the interface may also explain this phenomenon.[25] Another possibility may be secondary mechanisms such as interface dipoles caused by the formation of an interface state as well as fabrication-induced defects at the interface. Higher ideality factor values ($n > 1$) may also be due to the presence of a thick interfacial insulator layer between the metal and semiconductor.[26]

The values of the series resistance (R_S) and shunt resistance (R_{Sh}) of the Y/*p*-GaN SBD were estimated from the junction resistance obtained by $R_j = \partial V/\partial I$ from the *I*–*V* characteristics. Figure 3 presents a plot of the junction resistance R_j versus the bias voltage of the Y/*p*-GaN SBD at various annealing temperatures, from which the R_S and R_{Sh} values of the as-deposited and annealed Y/*p*-GaN SBDs are estimated. The values of the R_S and R_{Sh} were 95 MΩ and 2.5×10^{12} Ω for as-deposited, 285 MΩ and 3.9×10^{12} Ω for 400°C, 1321 MΩ and 4.3×10^{12} Ω for 500°C, and 139 MΩ and 3.3×10^{12} Ω for 600°C, respectively. These results reveal that the R_S and R_{Sh} increased with annealing at 500°C, and then decreased slightly after annealing at 600°C.

The Cheung and Cheung[27] technique was used to determine the series resistance (R_S), barrier height (Φ_b), and ideality factor (n) of the Y/*p*-GaN SBD in the non-linear forward-bias region of the ln*I*–*V* curve. According to Cheung's functions, the values of the R_S can be estimated from the following equations.[27]

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_S \tag{3}$$

$$H(I) = V - \left(\frac{nkT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) \tag{4}$$

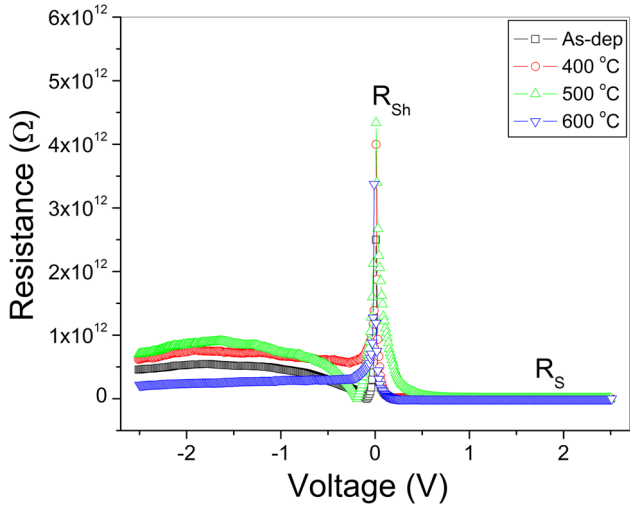

Fig. 3. Plot of the junction resistance between Y and *p*-GaN at various annealing temperatures.

where $H(I)$ can be written as

$$H(I) = IR_S + n\Phi_b \tag{5}$$

According to Eqs. 3 and 5, the forward-bias d*V*/d(ln*I*) versus *I* and H(*I*) versus *I* gives linear behavior for the as-deposited and annealed Y/*p*-GaN SBD, as presented in Fig. 4. The slope and y-axis intercept of d*V*/d(ln*I*) versus *I* plots (Fig. 4a) will give R_S and nkT/q, respectively. Conversely, the second estimation of R_S is calculated from the slope of H(*I*) versus *I* plots. Using the ideality factor value calculated from Eq. 3, the values of SBH are obtained from the y-axis intercept of H(*I*) versus *I* plots (Fig. 4b). The values of R_S, n, and Φ_b calculated from the analysis of d*V*/d(ln*I*) versus *I* and H(*I*) versus *I* plots for the Y/*p*-GaN SBD at different annealing temperatures are given in Table I. Here we can see that the values of R_S are closely matched between the two plots, implying their consistency and validity. However, the ideality factors estimated from the d*V*/d(ln*I*)–*I* plot and the forward-bias ln(*I*)–*V* plot are different, possibly due to the existence of series resistance and interface states and to the voltage drop across the interface layer. The R_S values obtained from the d*V*/d(ln*I*) versus *I* and H(*I*) versus *I* plots are in reasonably good agreement with those obtained from the *I*–*V* characteristics for the as-deposited and annealed contacts.

In addition, the modified Norde function[28] was employed to determine the barrier height (Φ_b) and series resistance (R_S) of the Y/*p*-GaN SBD. A plot of the Norde function $F(V)$ versus V for the Y/*p*-GaN SBD as a function of annealing temperature is presented in Fig. 5. The modified Norde function can be expressed as

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{6}$$

where γ is a dimensionless integer having a value greater than the ideality factor, and $I(V)$ is the

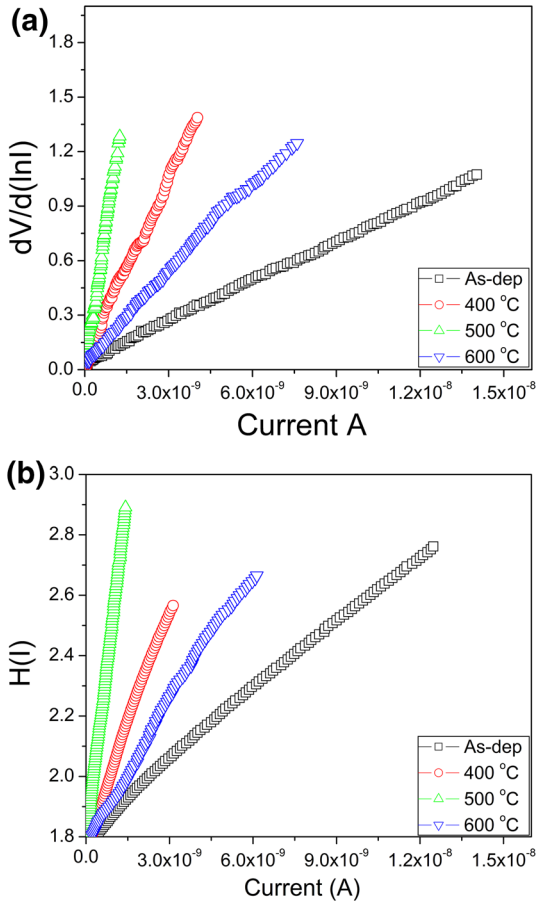

Fig. 4. Plots of (a) d*V*/d (ln*I*) versus *I* and (b) H(*I*) versus *I* for the Y/*p*-GaN SBD at various annealing temperatures.

current obtained from the *I*–*V* curve. The barrier height is expressed as

$$\Phi_b = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{kT}{q} \quad (7)$$

where $F(V_{min})$ is the minimum point of $F(V)$, and V_{min} is the corresponding voltage. The R_S is calculated using the following relation

$$R_s = \frac{kT(\gamma - n)}{qI} \quad (8)$$

where I is the current in the device corresponding to voltage V_0 (at which $F(V)$ becomes minimum). The values of Φ_b and R_S calculated for the Y/*p*-GaN SBD at different annealing temperatures are presented in Table I. Here, the Φ_b values calculated from the Cheung and Norde functions are in good agreement with those calculated from the forward-bias ln*I*–*V* characteristics. However, the values of R_S calculated from Cheung's function are lower than those calculated from the modified Norde function, since Cheung's function is applied only to the non-linear (high-voltage) region of the forward-bias *I*–*V* characteristics, while the Norde function is applied to the entire forward-bias *I*–*V* characteristics of the diodes.[29,30]

There is generally a native insulating oxide layer in an MS, usually 1–2 nm thick, on the surface of the semiconductor. The current through such a diode can be given as[23]

$$I = AA^*T^2 \exp\left(-\frac{q\psi_s}{kT}\right)\left[\exp\left(-\frac{qV_p}{nkT}\right)\right] \quad (9)$$

Table I. Barrier height, ideality factor, series resistance, and interface state density of the Y/*p*-GaN SBD calculated by *I*–*V* and *C*–*V* methods at various annealing temperatures

Parameter	As-deposited	400°C	500°C	600°C
I–*V* characteristics				
Barrier height, Φ_b (eV)	0.95	0.98	1.01	0.96
Ideality factor, n	1.64	1.33	1.21	1.53
Shunt resistance R_{Sh} (Ω)	2.5×10^{12}	3.9×10^{12}	4.3×10^{12}	3.3×10^{12}
Series resistance, R_S (MΩ)	95	285	1321	131
Cheung's method				
dV/d(ln I) versus I				
Series resistance, R_S (MΩ)	73	338	1001	164
Ideality factor, n	1.81	1.46	1.32	1.63
H(I) versus I				
Series resistance, R_S (MΩ)	77	268	781	152
Barrier height, Φ_b (eV)	1.00	1.21	1.35	1.09
Norde's method				
Barrier height, Φ_b (eV)	0.98	1.01	1.02	0.97
Series resistance, R_S ($\times 10^9\Omega$)	33	45	199	10
C–*V* characteristics				
Barrier height, Φ_b (eV)	1.19	1.26	1.29	1.22
Built-in potential (V)	0.92	1.00	1.02	0.96
Interface state density (N_{SS}) ($\times 10^{13}$ cm^{-2} eV^{-1})	4.71	2.41	1.52	3.90

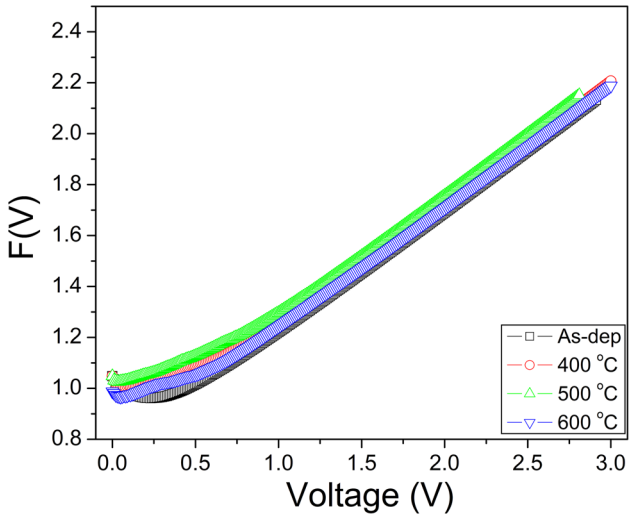

Fig. 5. Modified Norde plot of the Y/*p*-GaN SBD at various annealing temperatures.

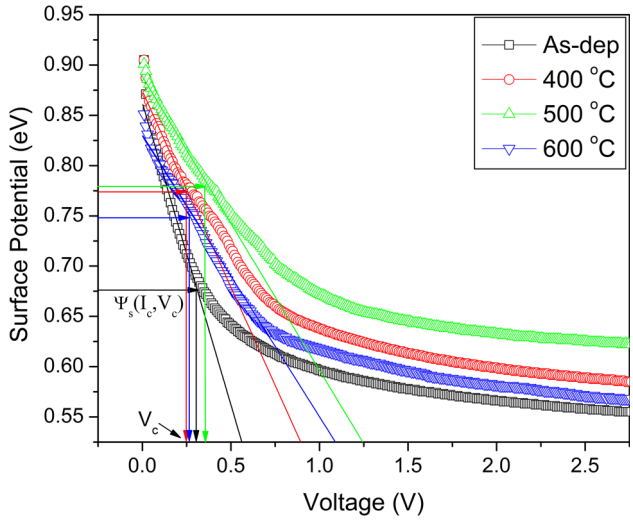

Fig. 6. Surface potential versus forward voltage curves of the Y/*p*-GaN SBD at various annealing temperatures.

The effective barrier heights are also estimated based on the method proposed by Chattopadhyay[31] if the values of the critical surface potential, $\Psi_s(I_c,V_c)$, the critical voltage, V_c, and $n = 1/\alpha$ are known experimentally. The surface potential, Ψ_s, is expressed as

$$\psi_s = \frac{kT}{q}\ln\left[\frac{AA^*T^2}{I}\right] - V_p \tag{10}$$

where V_p is the potential difference between the Fermi level and the top of the valance band in the neutral region of *p*-GaN, and $V_p = (kT/q)\ln(N_V/N_a)$, where N_V is the effective density of the valance band. The potential difference, Ψ_s, is estimated using the value of V_p for the as-deposited and annealed Y/*p*-GaN SBD. The estimated Ψ_s values against the forward-bias voltage at different annealing temperatures are shown in Fig. 6. From this plot, the barrier height and ideality factor can be estimated. Also, the barrier height, Φ_b, can be described as

$$\Phi_b = \psi_s(I_c,V_c) + \alpha V_c + V_p \tag{11}$$

In addition, the inverse of ideality factor α is given by

$$\alpha = 1/n = -\left(\frac{d\psi_s}{dV}\right)_{I_c,V_c} \tag{12}$$

As can be observed in the Ψ_s-V plot (Fig. 6), the value of Ψ_s decreases linearly until V reaches the critical value V_c. The values of the critical V_c and $\Psi_s(I_c,V_c)$ of the Y/*p*-GaN SBD are estimated from Fig. 6 at different annealing temperatures. The barrier heights and ideality factors of Y/*p*-GaN SBD are then determined using Eqs. 11 and 12, which yield values of 0.93 eV and 1.81 for as-deposited, 0.95 eV and 2.63 for 400°C, 0.98 eV and 3.44 for 500°C, and 0.91 eV and 3.57 for 600°C, respectively. The barrier heights calculated from the Ψ_s-V plot are in good agreement with those calculated from the forward-bias ln$I$–V characteristics and the Cheung and Norde functions.

The capacitance–voltage characteristics (C–V) of the Y/*p*-GaN SBD are measured at a frequency of 1 MHz. A plot of $1/C^2$ versus voltage for the as-deposited and annealed Y/*p*-GaN SBDs is shown in Fig. 7, from which the built-in potential and barrier heights are estimated. In Schottky diodes, the depletion layer capacitance C can be given by[25]

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - \frac{kT}{q} - V\right)}{A^2 q N_a \varepsilon_s} \tag{13}$$

where A is the diode area, N_a is the carrier concentration of the GaN substrate, V_{bi} is the built-in potential, ε_s is the dielectric constant of the semiconductor, and k, T, and q have their usual definitions. The x-intercept (V_0) of the $1/C^2$ versus V plot is related to the built-in potential (V_{bi}), and the relation is $V_{bi} = V_0 + kT/q$. The barrier height Φ_b is given by the equation $\Phi_b = V_{bi} + V_p$, where V_p is the potential difference between the Fermi level and the top of the valance band in the neutral region of *p*-GaN, and $V_p = (kT/q)\ln(N_V/N_a)$, where N_V is the effective density of the valance band, and its value is $1.79 \times 10^{19}\,\mathrm{cm}^{-3}$. The barrier heights of the as-deposited Y/*p*-GaN SBD and with annealing at 400°C are 1.19 eV and 1.26 eV, respectively. The SBH values for the diodes annealed at 500°C and 600°C are 1.29 eV and 1.22 eV, respectively. The built-in potential of the as-deposited Y/*p*-GaN SBD is 0.92 V. The estimated values of the built-in potential are 1.00 V, 1.02 V, and 0.96 V for Y/*p*-GaN SBDs annealed at 400°C, 500°C, and 600°C,

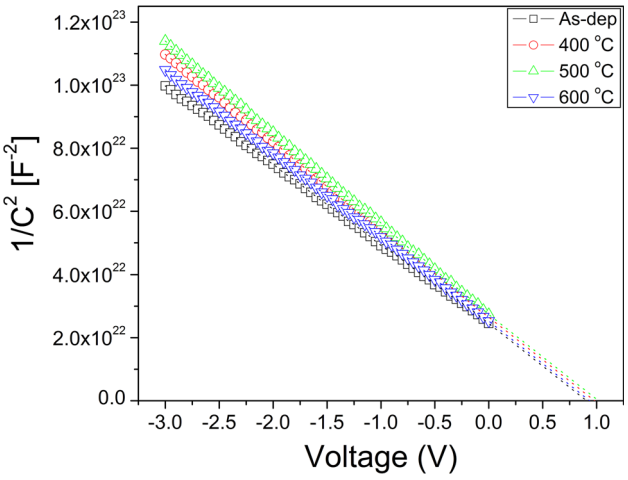

Fig. 7. Plot of $1/C^2$–V characteristics of the Y/p-GaN SBD at various annealing temperatures.

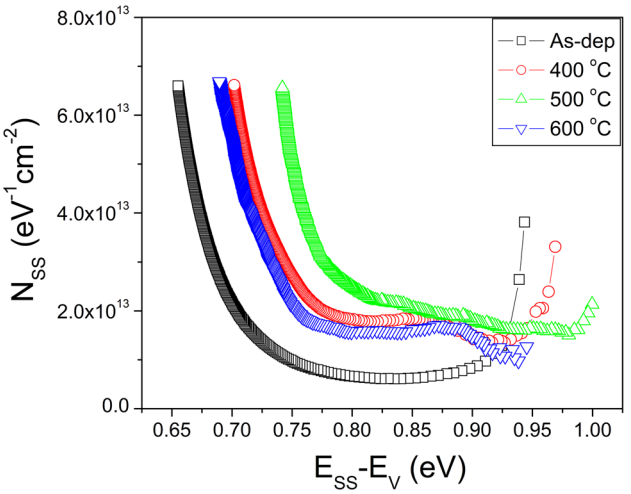

Fig. 8. The interface state energy distribution curves of the Y/p-GaN SBD at various annealing temperatures.

respectively. The calculated values of the built-in potential and SBH of the Y/p-GaN SBD at different annealing temperatures are given in Table I, which shows that the barrier height values achieved using the I–V technique are smaller than those determined using the C–V technique, possibly due to the existence of lateral inhomogeneity in the SBH at the MS interface.[32–36] The I–V analysis may include image-force and dipole lowering effects and may be reduced by the tunneling and leakage currents,[25,33] which would cause the I–V and C–V methods to yield different SBH values. Differences in structural defects, grain boundaries, dislocations, and stacking faults at the GaN layer[37] may also contribute to SBH inhomogeneity. Geng et al.[38] demonstrated that pinholes arise from the extended core-less dislocations, which originate in the GaN buffer layer, resulting in a high leakage current and low SBH. Conversely, much fewer dislocations or pinholes appear on the surface of the sample, resulting in low leakage current and high effective SBH. The dislocations or pinholes are normally less affected by C–V measurements, and hence the determined SBH is considered more reliable, though the depletion width can be altered by the interface defects if they are deeper into the space charge region.

The value of the ideality factor becomes greater than unity because of the effects of the interface states (N_{SS}) in equilibrium with the semiconductor. The density distribution of the N_{SS} can be estimated from the forward-bias I–V data by taking into account the voltage-dependent ideality factor $n(V)$ and effective barrier height (Φ_e). Card and Rhoderick[39] proposed that the ideality factor n of a diode becomes greater than unity, and the interface state density N_{SS} can be expressed as

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \tag{14}$$

where W_D is the space charge width, N_{SS} is the density of interface states, and ε_s and ε_i are the permittivity of the semiconductor and interfacial layer and δ its thickness, respectively. The value of W_D ($W_D = \sqrt{2\varepsilon_s V_{bi}/qN_a}$) is determined from reverse-bias $1/C^2$ versus V plot for each annealing temperature. The voltage-dependent ideality factor $n(V)$ can be expressed as $n(V) = V/(kT/q)\ln(I/I_s)$.[40] The interface state density can be expressed as

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_d}\right] \tag{15}$$

In p-type semiconductors, the energy of the interface states E_{SS} with respect to the top of the valance band at the surface of the semiconductor is given by

$$E_{SS} - E_V = q(\Phi_e - V) \tag{16}$$

The energy distribution curves of N_{SS} were determined from the experimental data of forward I–V characteristics. The N_{SS} versus E_{SS}-E_V was obtained by substituting the $n(V)$ and other parameters in Eq. 15, and these were plotted at different annealing temperatures and are presented in Fig. 8. Here we can clearly see that the N_{SS} increases with bias from mid-gap towards the top of the valance band. The extracted interface state density of the Y/p-GaN SBD was 4.71×10^{13} cm^{-2} eV^{-1} for as-deposited contacts, and 2.41×10^{13} cm^{-2} eV^{-1} with annealing at 400°C, 1.52×10^{13} cm^{-2} eV^{-1} at 500°C, and 3.90×10^{13} cm^{-2} eV^{-1} at 500°C. The interface state density was found to decrease with an increase in annealing temperature up to 500°C, and then to increases slightly after annealing at 500°C. These results reveal that the interface states and series resistance affect the electrical properties of the Y/p-GaN SBD.

Next, to investigate the dominant current conduction mechanism in the entire forward-bias

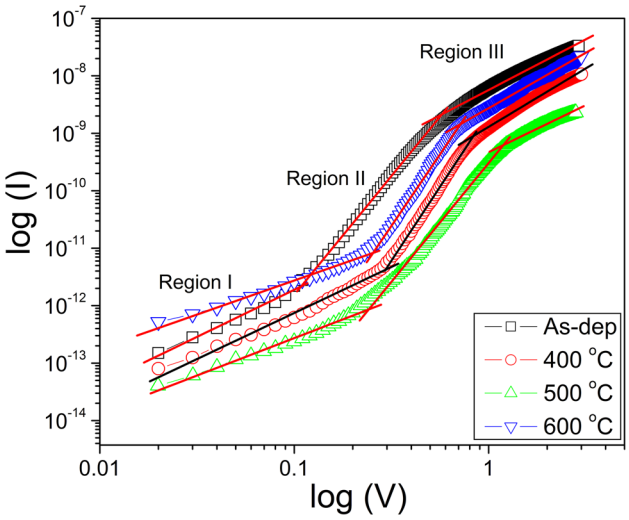

Fig. 9. Plot of forward-bias log (*I*) versus log (*V*) for the Y/*p*-GaN SBD at various annealing temperatures.

region for the Y/*p*-GaN SBD, *I*–*V* characteristics were also drawn in logarithmic scale for as-deposited contacts and with annealing at 400°C, 500°C, and 600°C, and are presented in Fig. 9. Here we can see that the log*I*–log*V* plots have three distinct linear regions (region I, region II, and region III) with different slopes for the as-deposited and annealed contacts that obey $I \propto V^m$ change (here, m is the slope of the log*I*–log*V* plot), i.e., the current is directly proportional to the applied bias voltage.[41] These three linear regions indicate the existence of different conduction mechanisms. From Fig. 9 we can see that in region I, the slope values are 1.64 for as-deposited, 1.60 for 400°C, 1.30 for 500°C, and 1.18 for 600°C. These values are close to unity, which indicates an ohmic behavior at low voltages. This behavior can be attributed to the existing background doping or thermally generated carriers.[41,42] In region II, the slope values for as-deposited contacts and with annealing at 400°C, 500°C, and 600°C are 4.13, 5.14, 4.13, and 4.97, respectively. These slope values are greater than 2.0, indicating that the charge transport is governed by space-charge limited-current (SCLC) with discrete trapping levels. At higher voltages, i.e., in region III, the slopes of the as-deposited and annealed contacts (1.76 for as-deposited, 2.03 for 400°C, 1.63 for 500°C, and 1.92 for 600°C) tend to decrease, since the device approaches the "trap-filling" limit when injection level is high, whose dependence is the same as in the trap-free SCLC.[43,44]

Furthermore, we can observe from Fig. 2 that the as-deposited and annealed Y/*p*-GaN SBD exhibit exponential dependence of reverse current (I_R) on applied voltage (V_R), which strongly suggests that Poole–Frenkel or Schottky barrier lowering was operative in the Schottky junction. Figure 10a and b shows the plots of I_R/E versus $E^{1/2}$ and I_R/T^2 versus $E^{1/2}$ for the as-deposited and annealed Y/*p*-GaN

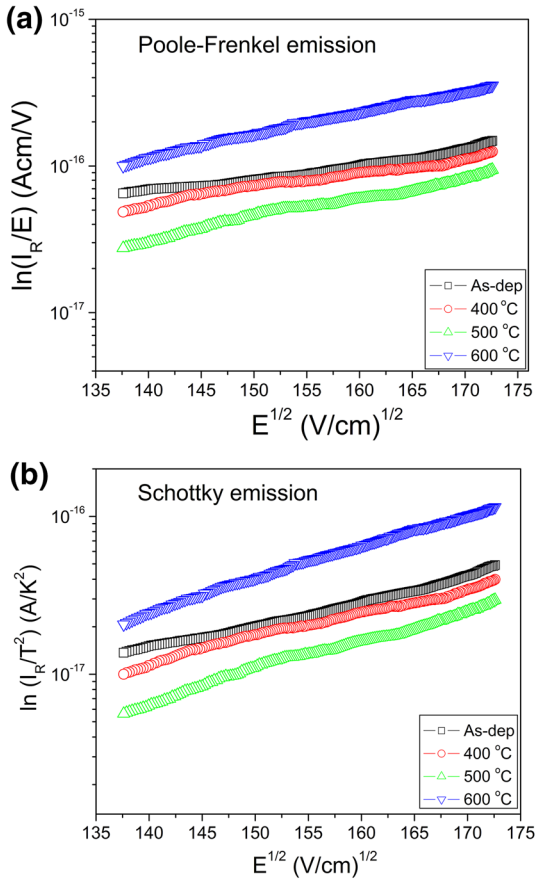

Fig. 10. Plots of (a) I_R/E versus $E^{1/2}$, and (b) I_R/T^2 versus $E^{1/2}$ for the Y/*p*-GaN SBD at various annealing temperatures.

SBDs. The plots exhibit a linear variation irrespective of annealing temperatures, indicating possible dominance of Poole–Frenkel and Schottky emission on the reverse current. The reverse current through the Schottky diode when dominated by Poole–Frenkel emission is described as[45,46]

$$I_R \propto E \exp\left[\frac{1}{kT}\sqrt{\frac{qE}{\pi\varepsilon}}\right] \tag{17}$$

and the contribution to reverse current when dominated by Schottky emission mechanism is described as

$$I_R \propto T^2 \exp\left[\frac{1}{2kT}\sqrt{\frac{qE}{\pi\varepsilon}}\right] \tag{18}$$

where E is the maximum electric field in the junction. The plots of I_R/E versus $E^{1/2}$ and I_R/T^2 versus $E^{1/2}$ present linear curves for the Poole–Frenkel and Schottky emissions, and the slope can be expressed as[47]

$$S = \frac{q}{nkT}\sqrt{\frac{q}{\pi\varepsilon}} \tag{19}$$

Here, n = 1 for Poole–Frenkel and n = 2 for Schottky emission. Generally, the Poole–Frenkel and

Table II. The theoretical and experimental slope values of Poole–Frenkel and Schottky emissions for the Y/*p*-type GaN SBD at various annealing temperatures

	Poole–Frenkel emission		Schottky emission	
Sample	**Theoretical**	**Experimental**	**Theoretical**	**Experimental**
As-deposited		0.00971		0.01530
400°C	0.00951	0.00984	0.00475	0.01523
500°C		0.01360		0.01892
600°C		0.01487		0.02040

Schottky effects can be distinguished by the estimated values of the field-lowering coefficients. According to Eq. 19, the Poole–Frenkel field-lowering (β_{PF}) coefficient is twice the Schottky field-lowering coefficient (β_S). The theoretical and experimental slope values obtained from the fit to the data of β_{PF} and β_S for the as-deposited and annealed Y/*p*-GaN SBDs are given in Table II. Here we can see that the experimental slopes determined are close to the theoretical values of the Poole–Frenkel field-lowering coefficient. Hence, the reverse current of Y/*p*-GaN SBD is dominated by the Poole–Frenkel field-lowering mechanism irrespective of annealing temperature. This suggests that the conduction mechanism of the Y/*p*-GaN SBD is related to the presence of a high density of structural defects or trap levels in the diode, which may be responsible for trapping/detrapping of charge carriers.[48,49]

CONCLUSIONS

The electrical properties and the forward and reverse current transport mechanisms of Y/*p*-GaN SBD were investigated by *I–V* and *C–V* measurements before and after annealing at 600°C. The SBH of the as-deposited and with annealing at 400°C contacts were 0.95 eV (*I–V*)/1.19 eV (*C–V*) and 0.98 eV (*I–V*)/1.26 eV (*C–V*), respectively. However, the SBH of Y/*p*-GaN SBD increased to 1.01 eV (*I–V*)/1.29 eV (*C–V*) after annealing at 500°C for 1 min in a nitrogen atmosphere. Upon annealing at 600°C, the SBH decreased slightly, to 0.96 eV (*I–V*)/1.12 eV (*C–V*). Cheung's, Norde, and Ψ_s-*V* plots were employed to determine the SBH at different annealing temperatures. The values of SBH obtained from the *I–V* method were comparable to those obtained from the Cheung, Norde, and Ψ_s-*V* plots. Series resistance values for Y/*p*-GaN SBD were also extracted from the *I–V*, Cheung's, and Norde functions at different annealing temperatures, and the values were in good agreement with one another. Experimental results showed a decrease in the interface state density of the Y/*p*-GaN SBD when the diode was annealed at 500°C, and then a slight increase after annealing at 600°C. In addition, the conduction mechanism of the Y/*p*-GaN SBD under forward-bias *I–V* characteristics was found to be ohmic in low-voltage regions, whereas a space-charge limited conduction (SCLC) mechanism was found in higher-voltage regions at all annealing temperatures. The electric field dependence of the reverse current showed that the Poole–Frenkel emission dominated the reverse current in the Y/*p*-GaN SBD irrespective of annealing temperature.

ACKNOWLEDGEMENTS

This research was supported by a grant from the R&D Program for Industrial Core Technology (Grant No.: 10045216) and by the Transfer machine specialized lighting core technology development professional manpower training project (Project No.: N0001363) funded by the Ministry of Trade, Industry and Energy (MOTIE), Republic of Korea.

REFERENCES

1. L.H. Huang, S.H. Yeh, C.T. Lee, H. Tang, J. Bardwell, and J.B. Webb, *IEEE Electron Devices Lett.* 29, 284 (2008).
2. T. Miyajima, H. Watanabe, M. Ikeda, and H. Yokoyama, *Appl. Phys. Lett.* 94, 161103 (2009).
3. B.J. Kim, Y.R. Ryu, T.S. Lee, and H.W. White, *Appl. Phys. Lett.* 94, 103506 (2009).
4. T.K. Kim, S.H. Kim, S.S. Yang, J.K. Son, K.H. Lee, Y.G. Hong, K.H. Shim, J.W. Yang, K.Y. Lim, S.J. Bae, and G.M. Yang, *Appl. Phys. Lett.* 94, 161107 (2009).
5. W.D. Hu, X.S. Chen, F. Yin, J.B. Zhang, and W. Lu, *J. Appl. Phys.* 105, 084502 (2009).
6. K. Takahashi, J.P. Ao, Y. Ikawa, C.Y. Hu, H. Kawai, N. Shinohara, N. Niwa, and Y. Ohno, *Jpn. J. Appl. Phys.* 48, 04C095 (2009).
7. Z. Chen, Y. Pei, S. Newman, R. Chu, D. Brown, R. Chung, S. Keller, S.P. Denbaars, S. Nakamura, and U.K. Mishra, *Appl. Phys. Lett.* 94, 112108 (2009).
8. K.P. Korona, A. Drabinska, P. Caban, and W. Strupinski, *J. Appl. Phys.* 105, 083712 (2009).
9. J.C. Lin, Y.K. Su, S.J. Chang, W.H. Lan, K.C. Huang, W.R. Chen, C.Y. Huang, W.C. Lai, W.J. Lin, and Y.C. Cheng, *Appl. Phys. Lett.* 91, 173502 (2007).
10. A.C. Schmitz, A.T. Ping, M.A. Khan, Q. Chen, J.W. Yang, and I. Adesida, *Semicond. Sci. Technol.* 11, 1464 (1996).
11. Q.Z. Liu and S.S. Lau, *Solid State Electron.* 42, 677 (1998).
12. J. Wu, *J. Appl. Phys.* 106, 011101 (2009).
13. K. Shiojimaa, *Appl. Phys. Lett.* 77, 2625 (2000).
14. L.S. Yu, D. Qiao, L. Jia, and S.S. Lau, *Appl. Phys. Lett.* 79, 2731 (2001).
15. Y.J. Lin, *Appl. Phys. Lett.* 86, 122109 (2005).
16. C.K. Tan, A.A. Aziz, and F.K. Yam, *Appl. Surf. Sci.* 252, 5930 (2006).
17. C.K. Tan, A.A. Aziz, Z. Hassan, F.K. Yam, and A.Y. Hudeish, *Phys. Stat. Solid C* 3, 1762 (2006).
18. J.W. Kim and J.W. Lee, *Appl. Surf. Sci.* 250, 247 (2005).

19. Y. Fukushima, K. Ogisu, M. Kuzuhara, and K. Shiojima, *Phys. Stat. Solid C* 6, S856 2009).
20. G. Greco, P. Prystawko, M. Leszczynski, R.L. Nigro, V. Raineri, and F. Roccaforte, *J. Appl. Phys.* 110, 123703 (2011).
21. S.-H. Jang and J.-S. Jang, *Electron. Mater. Lett.* 9, 245 (2013).
22. Y.-Y. Choi, S. Kim, M. Oh, H. Kim, and T.-Y. Seong, *Superlattices Microstruct.* 77, 76 (2015).
23. E.H. Rhoderick and R.H. Williams, *Metal-Semiconductor Contacts* (Clarendon: Oxford, 1988), p. 121.
24. S. Altindal, S. Karadeniz, N. Tugluoglu, and A. Tataroglu, *Solid State Electron.* 47, 1847 (2003).
25. R.T. Tung, *Phys. Rev. B* 45, 13502 (1992).
26. S.M. Sze, *Physics of Semiconductor Devices* (Willey: New York, 1981), p. 279.
27. S.K. Cheung and N.W. Cheung, *Appl. Phys. Lett.* 49, 85 (1986).
28. H. Norde, *J. Appl. Phys.* 50, 5052 (1979).
29. X. Zhang, F. Hai, T. Zhang, C. Jia, X. Sun, L. Ding, and W. Zhang, *Microelectron. Eng.* 93, 5 (2012).
30. S. Sonmezoglu, S. Senkul, R. Tas, G. Cankaya, and M. Can, *Solid Stat. Sci.* 12, 706 (2010).
31. P. Chattopadhyay, *Solid State Electron.* 38, 739 (1995).
32. G.D. Mohan, *J. Appl. Phys.* 55, 980 (1984).
33. Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, and F. Cardon, *Solid State Electron.* 29, 633 (1986).
34. J.H. Werner and H.H. Guttler, *J. Appl. Phys.* 69, 1522 (1991).
35. B. Boyarbay, H. Cetin, M. Kaya, and E. Ayyildiz, *Microelectron. Eng.* 85, 721 (2008).
36. G. Nagaraju, L.D. Rao, and V.R. Reddy, *Appl. Phys.* A121, 131 (2015).
37. R. Padma, G. Nagaraju, V.R. Reddy, and C.J. Choi, *Thin Solid Films* 598, 236 (2016).
38. L. Geng, F.A. Ponce, S. Tanaka, H. Omiya, and Y. Nakagawa, *Phys. Stat. Solid A* 188, 803 (2001).
39. H.C. Card and E.H. Rhoderick, J. Phys. D. *Appl. Phys.* 4, 1589 (1971).
40. O. Gullu and A. Turut, *J. Appl. Phys* 106, 103717 (2009).
41. S. Wagle and V. Shirodkar, *Braz. J. Phys.* 30, 380 (2000).
42. S. Aydogan, U. Incekara, A.R. Deniz, and A. Turut, *Microelectron. Eng.* 87, 2525 (2010).
43. V.R. Reddy, V. Janardhanam, J.-W. Ju, H.-J. Yun, and C.-J. Choi, *Solid State Commun.* 179, 34 (2014).
44. S.M. El-Sayed, H.M.A. Hamid, and R.M. Radwan, *Radiat. Phys. Chem.* 69, 339 (2004).
45. T.T. BenJomaa, L. Beji, A. Ltaeif, and A. Bouazizi, *Mater. Sci. Eng. C* 26, 530 (2006).
46. H.D. Lee and I.E.E.E. Trans, *Electron. Dev.* 47, 762 (2000).
47. V. Janardhanam, H.K. Lee, K.H. Shim, H.B. Hong, S.H. Lee, K.S. Ahn, and C.J. Choi, *J. Alloys Compd.* 504, 146 (2010).
48. A.A. Kumar, V.R. Reddy, V. Janardhanam, H.-D. Yang, H.-J. Yun, and C.-J. Choi, *J. Alloys Compd.* 549, 18 (2013).
49. V.R. Reddy, V. Janardhanam, J.-W. Ju, H. Hong, and C.-J. Choi, *Semicond. Sci. Technol.* 29, 075001 (2014).