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Analytical Modeling of Potential Distribution and Threshold Voltage of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile

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This paper reports a new two-dimensional (2D) analytical model for the potential distribution and threshold voltage of the short-channel symmetric gate underlap ultrathin DG MOSFETs with a lateral Gaussian doping profile in the source (S)/drain (D) region. The parabolic approximation and conformal mapping techniques have been explored for solving the 2D Poisson's equation to obtain the channel potential function of the device. The effects of straggle parameter (of the lateral Gaussian doping profile in the S/D region), underlap length, gate length, channel thickness and oxide thickness on the surface potential and threshold voltage have been investigated. The loss of switching speed due to the drain-induced barrier lowering (DIBL) has also been reported. The proposed model results have been validated by comparing them with their corresponding TCAD simulation data obtained by using the commercially available 2D ATLAS™ simulation software.

Key words: DG MOSFETs, ultra-shallow junction (USJ), straggle parameter, drain-induced barrier lowering (DIBL), short-channel effects (SCEs), gate underlap, loss of switching speed

INTRODUCTION

With the significant progress in the fabrication of FinFETs[1–3] or vertical DG MOSFETs,[4,5] the ultrathin body (UTB) double-gate (DG) MOS structures have been of great interest for researchers into sub-50 nm CMOS technology due to their excellent immunity to short-channel effects (SCEs) and ultimate scalability features.[6–9] However, the relentless scaling of the channel thickness of the DG MOSFETs may lead to the undesired increase in the source (S)/drain (D) resistance and junction capacitance which, in turn, may decrease the drive current.[10] A number of works reported in the literature show that the introduction of a gate underlapped channel region between the gate end and the beginning of the S/D region in the undoped DG MOS structures improves the device performance by reducing the SCEs,[11–13] gate edge direct tunneling leakage[14] and gate sidewall fringe capacitance.[15,16] Trivedi et al.[17] reported a simulation study of ultra-shallow junction (USJ) gate underlap DG MOSFETs to demonstrate the achievement of the combined benefits of improved immunity to SCEs due to the gate underlap region and enhanced on-state drive current due to the introduction of a lateral Gaussian doping profile in the S/D region. Bansal et al.[18] reported for the first time an analytical model for the potential distribution and subthreshold characteristics of gate underlap DG MOSFETs with uniformly doped S and D regions in a conventional manner. They observed significant improvements in the drain-induced barrier lowering (DIBL) and subthreshold swing with the increase in the underlap length of the DG MOS device. Vaddi

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et al.[19,20] reported an analytical model for the potential distributions and subthreshold characteristics of both the gate underlap and overlap DG MOSFETs with conventional uniform doping profile in the S/D region. Recently, Nandi et al.[21] has reported an analytical model to show the improvement of the on-current at the cost of degraded immunity to SCEs by controlling the lateral straggle parameter of a lateral Gaussian doping profile introduced in the S/D region of the DG MOSFETs without any gate underlap region. However, to the best of our knowledge, no analytical model has yet been reported to study the combined effects of lateral Gaussian doping in the S/D region and the gate underlap region on the potential distribution and subthreshold characteristics of the underlap DG MOSFETs. In view of the above, an attempt has been made in the present paper to report an analytical two-dimensional (2D) model of the gate underlap USJ DG MOSFETs with a lateral Gaussian profile in the S/D region to achieve the combined benefits of improved SCEs and enhanced drive current as discussed above. For the validity of the proposed model, the model results have been compared with the simulation data obtained by using the commercially available 2D ATLAS™ device simulator of the Silvaco International.[22]

THEORETICAL MODELING

Formulation of Potential Distribution

Figure 1a shows the schematic diagram of the gate underlap DG MOSFET structure under consideration with lateral Gaussian doping in the S/D region. The symbols L_G, L_{ul}, t_{si} and t_{ox} represent the gate length, underlap channel length, silicon film thickness and gate oxide thickness of the device, respectively. The front and back gates are assumed to be tied together with a single gate-to-source voltage (V_{GS}). The doping profile, i.e. $N_{sd}(x)$, in the USJ regions in the channel is assumed to be of a lateral Gaussian function expressed as[21]

$$N_{sd}(x) = N_{sdp}e^{\left(\frac{-x^2}{2\sigma_L^2}\right)} \quad (1)$$

where, N_{sdp} is the peak Gaussian doping. Figure 1b shows various lateral Gaussian profiles in the S/D region for different values of lateral straggle σ_L in the channel. The degenerated doping value N_{de} has been assumed as 2.7×10^{19} cm^{-3} for the present study.[21]

Let the 2D potential functions in the regions I, II and III shown in Fig. 1a be denoted by $\psi_1(x,y)$, $\psi_2(x,y)$ and $\psi_3(x,y)$ respectively. Now, the generalized potential function $\psi_i(x,y)$ for $i = 1,\ 2$ and 3 can be determined by solving the following 2D Poisson equation:

$$\frac{d^2\psi_i(x,y)}{dx^2} + \frac{d^2\psi_i(x,y)}{dy^2} = \frac{q}{\varepsilon_{si}}\left(N_a^- - N_{sd}^+(x)\right) \quad (2)$$

where, N_a^- is the ionized acceptor concentration and $N_{sd}^+(x)$ is the ionized donor concentration represented by[21]

$$N_{sd}^+(x) = \left(\frac{N_{sdp}e^{\left(\frac{-x^2}{2\sigma_L^2}\right)} + N_{sdp}e^{\left(\frac{-(L_G+2L_{ul}-x)^2}{2\sigma_L^2}\right)}}{\left(1 + s_D e^{\left(\frac{(E_F-E_D)}{kT}\right)}\right)}\right) \quad (3)$$

where, s_D is the spin degeneracy factor, E_F and E_D are the Fermi level and donor level of the $N_{SD}(x)$ profile given by[21]

$$E_F = \left(\frac{E_g}{2}\right) + kT\ln\left(\frac{N_{sd}(x)}{n_{i,eff}}\right) \quad (4)$$

$$E_D = E_{g,eff} - E_I \quad (5)$$

where E_I and $E_{g,eff}$ are the ionization energy and effective band-gap of the Si considering many body effects, respectively. It is well known that the donor impurities form the energy level E_D below the conduction band E_C in a lightly doped n-type semiconductor and the impurity ionization energy $E_I = E_C - E_D$ represents the difference in energy between the conduction band energy and donor energy levels. When the doping concentration in the semiconductor is increased, the donor energy level is shifted upward (i.e., towards E_C) and finally merges with the conduction band edge for doping concentration beyond a certain level thereby resulting in $E_I = 0$. The ionization energy in the channel near the vicinity of the source (drain)/channel junction can be expressed as an empirical relationship given by[21]

$$E_I = E_{I_o}\left(1 - \sqrt[3]{N_{sd}(x)/N_{de}}\right) \quad (6)$$

where E_{I_o} is the ionization energy of lightly doped Si crystal, N_{de} is the critical doping concentration beyond which Si behaves as a degenerate semiconductor, $n_{i,eff}$ is the effective intrinsic concentration of the Si under many body effects and $E_{g,eff}$ is the effective band-gap of the Si defined as[21]

$$n_{i,eff} = \sqrt{n_i^2 e^{\frac{\Delta E_g}{kT}}} \quad (7)$$

$$E_{g,eff} = E_g - \Delta E_g \quad (8)$$

where, E_g, ΔE_g and n_i are the energy band-gap, band-gap narrowing and intrinsic carrier density of Si. Notations used for various device parameters have been listed in Table I.

By considering the parabolic approximation, the solution of Eq. 2, $\psi_i(x,y)$ can be expressed as[23]:

$$\psi_i(x,y) = C_{i1}(x) + C_{i2}(x)y + C_{i3}(x)y^2 \quad (9)$$

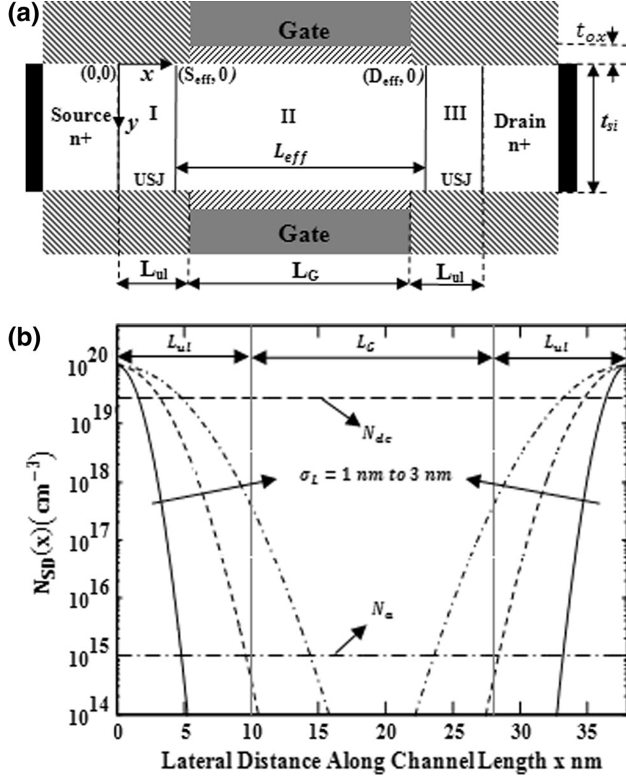

Fig. 1. (a) Schematic view of underlap DG MOSFET. (b) Lateral doping profile in the source/drain extension region for different values of straggle parameter.

where, $C_{i1}(x)$, $C_{i2}(x)$ and $C_{i3}(x)$ are arbitrary functions of x (for all $i = 1$, 2 and 3) which can be determined from the following boundary conditions:

$$\psi_i(x,0) = C_{i1}(x) \tag{10}$$

$$\psi_i(x,\ t_{si}) = C_{i1}(x) + C_{i2}(x)t_{si} + C_{i3}(x)t_{si}^2 \tag{11}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=0} = C_{i2}(x) \tag{12}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=t_{si}} = C_{i2}(x) + 2t_{si}C_{i3}(x) \tag{13}$$

Assuming $\psi_{si}(x) = \psi_i(x,y)|_{y=0}$ (for $i = 1$, 2 and 3) as the surface potential, the criteria of the continuity of electric field at gate oxide–channel interface gives[18]

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(x))}{t_{ox}} \tag{14}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(x))}{t_{ox}} \tag{15}$$

where, ε_{si} and ε_{ox}, V_{GS} are the permittivity of the silicon and SiO_2, gate to source voltage respectively, and V_{fb} is the flat band voltage given by[18]

$$V_{fb} = \phi_M - \left(\chi_s + \frac{E_g}{2q} + \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)\right) \tag{16}$$

where, ϕ_M,χ_s and E_g are the gate metal work function, electron affinity and band gap of the silicon, respectively.

By solving Eq. 11 with the help of boundary condition from Eqs. 12, 13, 14, and 15, we get

$$C_{i2}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{s2}(x))}{t_{ox}} \tag{17}$$

$$C_{i3}(x) = C_{i2}(x)/t_{si} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{(V_{GS} - V_{fb} - \psi_{s2}(x))}{t_{ox}} \tag{18}$$

By rearranging Eq. 2 for region II with the help of Eqs. 10, 17, and 18, we obtain

$$\frac{d^2\psi_{2s}(x)}{dx^2} - \frac{\psi_{2s}(x)}{\lambda^2} = \frac{q}{\varepsilon_{si}}\left(N_a - N_{sd}^+(x)\right) - \frac{(V_{GS} - V_{fb})}{\lambda^2} \tag{19}$$

where, $\lambda = \sqrt{\frac{\varepsilon_{si}t_{si}t_{ox}}{2\varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{ox}t_{ox}}\right)}$ is the characteristic length of the device under consideration. Solving

Table I. Notations of various device parameters

Parameters	Symbol	Values	Unit
Intrinsic doping	n_i	10^{10}	cm^{-3}
Channel doping	N_a	10^{15}	cm^{-3}
Source/drain doping	N_{sdp}	10^{20}	cm^{-3}
Degenerated doping	N_{de}	2.7×10^{19}	cm^{-3}
Silicon thickness	t_{si}	7	nm
Gate oxide thickness	t_{ox}	1	nm
Gate overlap length	L_G	18	nm
Ionization energy in lightly doped crystal	E_{I_o}	0.054 (arsenic)	eV
Spin degeneracy factor	s_D	2	–
Gate underlap length	L_{ul}	10	nm
Gate voltage	V_{GS}	–	V
Drain voltage	V_{DS}	–	V
Silicon energy band gap	E_g	1.12	eV

Eq. 19, the surface potential for the gate overlapped channel region II is given as:

$$\psi_{s2}(x) = Ce^{(x-L_{il})/\lambda} + De^{-(x-L_{ul})/\lambda} - \frac{q\lambda^2(N_a - N_{SD}^+(x))}{\varepsilon_{si}} + V_{GS} - V_{fb} \quad (20)$$

To model the fringing electric fields from gate to the gate underlapped spacer regions I and III, we have used the conformal mapping technique by converting (x, y) to (u, v) plane by using the following transfer function[18]

$$-y + j\eta(L_{ul} - x) = t_{ox}\sin(u + jv) \quad (21)$$

where,

$$\eta = \frac{t_{ox}}{L_{ul}}\sinh\left(\cosh^{-1}\left(\frac{t_{ox}+t_g}{t_{ox}}\right)\right) \quad (22)$$

Now, from the continuity of the electric fields in all three regions in the (u, v) plane, we can write

$$\left.\frac{d\psi_i(u,v)}{dy}\right|_{u=o;\, i=1,\,3} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(v))}{n\pi/2} \quad (23)$$

where, n is such that $|\sin(n\pi/2)| = 1$.

Following the methodology of Ref. 18 from the conformal mapping technique for obtaining the surface potential functions in regions I and III from Eqs. 2, 22, and 23, we can obtain

$$\psi_{s1}(x) = A\left[1 - \frac{\alpha}{2}r_1^2\right] + B\left[r_1 - \frac{\alpha}{6}r_1^3\right] + V_{GS} - V_{fb} \quad (24)$$

$$\psi_{s3}(x) = E\left[1 - \frac{\alpha}{2}r_2^2\right] + F\left[r_2 - \frac{\alpha}{6}r_2^3\right] + V_{GS} - V_{fb} \quad (25)$$

where,

$r_1 = \eta(L_{ul} - x)/t_{ox}$, $r_2 = \eta(x - L_G - L_{ul})/t_{ox}$ and $\alpha = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{2}{t_{ox}t_{si}(m\pi/2)}\left(\frac{t_{ox}}{\eta}\right)^2$

Constants A, B, C, D, E and F in Eqs. 24 and 25 can be determined by applying the following boundary conditions:

$$\psi_{s1}(S_{eff}) = V_{bi} \quad (26)$$

$$\psi_{s1}(L_{ul}) = \psi_{s2}(L_{ul}) \quad (27)$$

$$\psi_{s2}(L_{ul} + L_G) = \psi_{s3}(L_{ul} + L_G) \quad (28)$$

$$\psi_{s3}(D_{eff}) = V_{bi} + V_{DS} \quad (29)$$

$$\left.\frac{d\psi_{s1}(x)}{dx}\right|_{x=L_{ul}} = \left.\frac{d\psi_{s2}(x)}{dx}\right|_{x=L_{ul}} \quad (30)$$

$$\left.\frac{d\psi_{s2}(x)}{dx}\right|_{x=L_G+L_{ul}} = \left.\frac{d\psi_{s3}(x)}{dx}\right|_{x=L_G+L_{ul}} \quad (31)$$

where, $S_{eff} = \sqrt{\ln\left(\frac{N_{de}}{N_{sdp}}\right) \times (-\sigma_L^2)}$ defined as the distance at which the Gaussian doping profile in the source and drain region is effectively reduced to the critical degenerated doping value N_{de} in the channel[21] and $D_{eff} = L_G + 2L_{ul} - S_{eff}$.

Now, the effective channel length is calculated as

$$L_{eff} = L_G + 2L_{ul} - 2 \times S_{eff} \quad (32)$$

Therefore, we can write

$$A = C + D - \frac{q\lambda^2(N_a - N_{SD}^+(x))}{\varepsilon_{si}} \quad (33)$$

$$B = \frac{t_{ox}}{\eta\lambda}(D - C) \quad (34)$$

$$C = \left(\frac{g\left(V_{DS} + V_x\left(1 - e^{-L_G/\lambda}\right)\right) + \frac{t_{ox}H}{\eta\lambda}\left(V_{DS} + V_x\left(1 + e^{-L_G/\lambda}\right)\right)}{4\left(\frac{t_{ox}gH}{\eta\lambda}\right)\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox}H}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)}\right) \quad (35)$$

$$D = \left(\frac{g\left(V_x\left(e^{L_G/\lambda} - 1\right) - V_{DS}\right) + \frac{t_{ox}H}{\eta\lambda}\left(V_{DS} + V_x\left(1 + e^{L_G/\lambda}\right)\right)}{4\left(\frac{t_{ox}gH}{\eta\lambda}\right)\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox}H}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)}\right) \quad (36)$$

$$E = \mathrm{C}e^{L_{\mathrm{G}}/\lambda} + \mathrm{D}e^{-L_{\mathrm{G}}/\lambda} - \frac{q\lambda^2(N_{\mathrm{a}} - N_{\mathrm{SD}}^{+}(x))}{\varepsilon_{\mathrm{si}}} \quad (37)$$

$$F = \frac{t_{\mathrm{ox}}}{\eta\lambda}\left(\mathrm{C}e^{L_{\mathrm{G}}/\lambda} - \mathrm{D}e^{-L_{\mathrm{G}}/\lambda}\right) \quad (38)$$

where,

$$g = 1 - \frac{\alpha}{2}\left(\frac{\eta L_{\mathrm{ul}}}{t_{\mathrm{ox}}}\right)^2$$

$$H = \frac{\eta L_{\mathrm{ul}}}{t_{\mathrm{ox}}} - \frac{\alpha}{6}\left(\frac{\eta L_{\mathrm{ul}}}{t_{\mathrm{ox}}}\right)^3$$

$$V_{\mathrm{x}} = V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{fb}} + g\frac{q\lambda^2(N_{\mathrm{a}} - N_{\mathrm{SD}}^{+}(x))}{\varepsilon_{\mathrm{si}}}$$

$$V_{\mathrm{bi}} = V_{\mathrm{T}}\ln\left(\frac{N_{\mathrm{de}} \times N_{\mathrm{a}}}{n_i^2}\right)$$

Finally, using the values of $C_{i1}(x) = \psi_i(x,0) = \psi_{s1}(x)$, $C_{i2}(x)$ and $C_{i2}(x)$ from their respective Eqs. 10, 17, and 18 in Eq. 2, the 2D potential function in the three regions of the channel can be written as

$$\psi_i(x,y) = \psi_{\mathrm{si}}(x)\left[1 + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}t_{\mathrm{ox}}}y - \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}t_{\mathrm{ox}}t_{\mathrm{si}}}y^2\right] + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}t_{\mathrm{ox}}}(V_{\mathrm{GS}} - V_{\mathrm{fb}})\left[-y + \frac{y^2}{t_{\mathrm{si}}}\right]. \quad (39)$$

Formulation of Threshold Voltage, DIBL and Loss of Switching Speed

By putting $y = t_{\mathrm{si}}/2$ in Eq. 39, the central channel potential for gate overlap region $\psi_{\mathrm{c2}}(x) = \psi_2(x,y)|_{y=t_{\mathrm{Si}}/2}$ is given by

$$\psi_{\mathrm{c2}}(x) = \psi_{\mathrm{s2}}(x)\left[1 + \frac{\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}}{4\varepsilon_{\mathrm{si}}t_{\mathrm{ox}}}\right] - \frac{\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}}{4\varepsilon_{\mathrm{si}}t_{\mathrm{ox}}}(V_{\mathrm{GS}} - V_{\mathrm{fb}}) \quad (40)$$

It is important to mention that position (x_{min}) of the minimum channel central potential plays the role of a virtual cathode from which electron enters into the channel to contribute the drive current. By solving $\left.\frac{\partial\psi'_{\mathrm{c2}}(x)}{\partial x}\right|_{x=x_{\mathrm{min}}} = 0$, $x = x_{\mathrm{min}}$ [at which $\psi_{\mathrm{c2}}(x)$ has the minimum value] is given as

$$x_{\mathrm{min}} = L_{\mathrm{ul}} + (\lambda/2)\ln((D/C)_{\mathrm{max}})$$

Following the method described in Ref. 21 the threshold voltage can be defined as the gate voltage $V_{\mathrm{GS}} = V_{\mathrm{th}}$ at which the channel electron density at the minimum channel potential point reaches the channel doping density. Hence, we write

$$(n_i^2/N_{\mathrm{a}})e^{(\psi_{\mathrm{c2}}(x_{\mathrm{min}})/V_{\mathrm{T}})} = N_{\mathrm{a}} \quad (41)$$

where, V_{T} is the thermal voltage.

Now, solving Eq. 41 for $V_{\mathrm{GS}} = V_{\mathrm{th}}$, the final expression of the threshold voltage can be given by

$$V_{\mathrm{th}} = V_{\mathrm{fb}} + 2\phi - D_{\mathrm{max}}e^{\frac{-x_{\mathrm{min}}}{\lambda}} - C_{\mathrm{max}}e^{\frac{x_{\mathrm{min}}}{\lambda}} + \frac{\lambda^2 q(N_{\mathrm{a}} - N_{\mathrm{SD}}^{+}(x))}{\varepsilon_{\mathrm{si}}} - V(x_{\mathrm{min}}) \quad (42)$$

To include the quantum mechanical effects, we have added the quantum correction factor $\Delta V_{\mathrm{t}}^{\mathrm{QM}}$ to the value of V_{th} described by Eq. 42 to obtain the final expression for the threshold voltage as

$$V_{\mathrm{thf}} = V_{\mathrm{th}} + \Delta V_{\mathrm{t}}^{\mathrm{QM}}$$

where,

$$\Delta V_{\mathrm{t}}^{\mathrm{QM}} = \frac{h^2}{8qm_{\mathrm{eff}}t_{\mathrm{si}}^2} \quad (43)$$

where, h is Planck's constant, $m_{\mathrm{eff}} = 0.19m_{\mathrm{o}}$ is the effective mass of electron with m_{o} as the mass of the electron in vacuum.

Now, the DIBL of the USJ underlap short-channel symmetric DG MOSFETs can be expressed as[20]

$$\mathrm{DIBL} = \frac{V_{\mathrm{thf}}|_{V_{\mathrm{DS}}=0.1} - V_{\mathrm{thf}}|_{V_{\mathrm{DS}}=1.1}}{(V_{\mathrm{DS}} = 1.1) - (V_{\mathrm{DS}} = 0.1)} \quad (44)$$

It is important to mention that the DIBL severely affects the switching speed of the scaled CMOS devices. The loss of switching speed caused by the DIBL effect in the short-channel underlap DG MOSFETs under consideration can be expressed as[24]:

$$\left(\frac{\Delta f}{f}\right) = \frac{-2\,DIBL}{V_{DS} - V_{thf}} \quad (45)$$

where, Δf is the decrease in the maximum operating frequency f due to the DIBL described by Eq. 44.

RESULTS AND DISCUSSION

In this section, the analytical results of the channel central potential, $\psi_{\mathrm{ci}}(x)$, and threshold voltage (V_{th}) of Underlap DG MOSFETs with Gaussian-doped source/drain have been compared with the TCAD simulation results of obtained by using the ATLAS™ 2D device simulation software. A drift–diffusion (DD) model along with the classical Fermi–Dirac statistics has been used for simulating the device structure in the ATLAS™ software. The quantum model (quantum) has been used to include the quantum mechanical effects in the TCAD simulation results. This model is based on

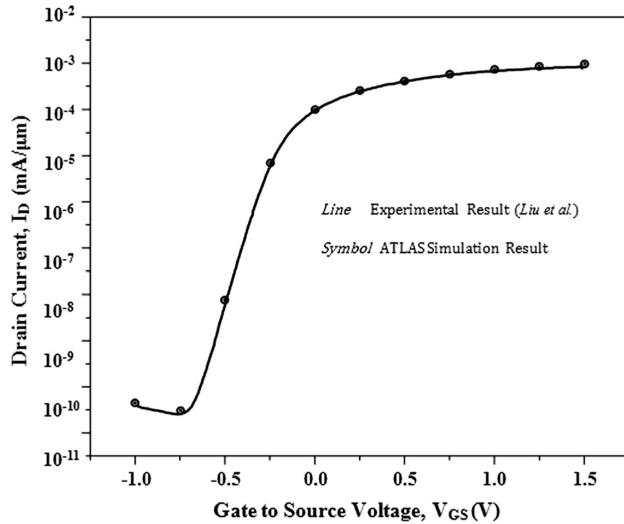

Fig. 2. Current versus gate-to-source voltage at V_{DS} = 1.0 V, parameters used as per Ref. 27.

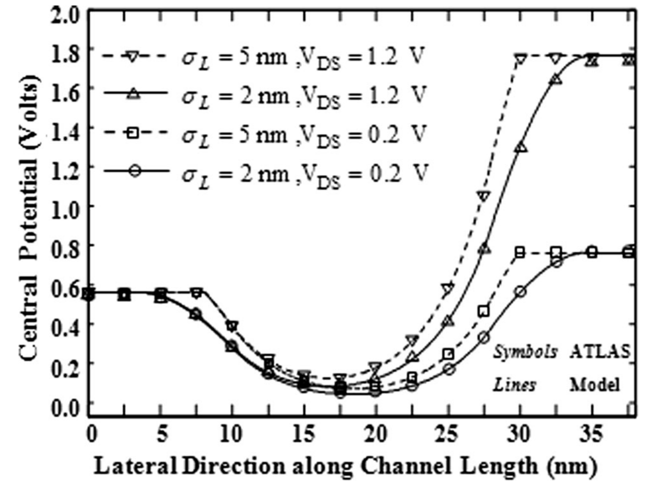

Fig. 3. Central potential along channel length, parameters used: $V_{GS} = 0.1$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $t_{si} = 7$ nm, $t_{ox} = 1$ nm.

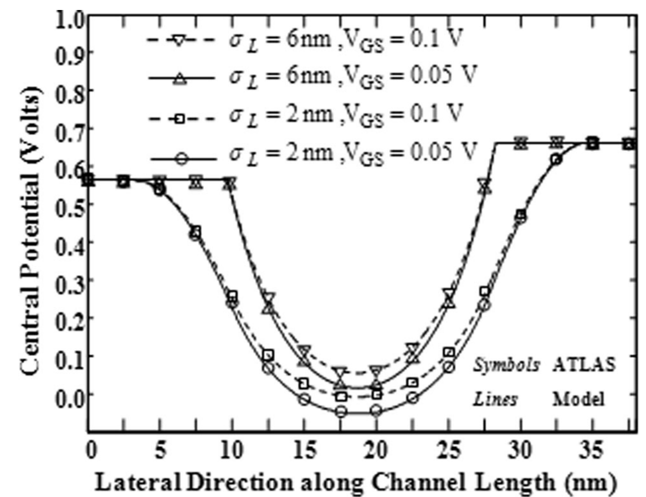

Fig. 4. Central potential along channel length, parameters used: $V_{DS} = 0.1$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $t_{ox} = 1$ nm, $t_{si} = 7$ nm.

the Wigner function equations-of-motion[25,26] which employs the quantum correction potential in the carrier current and energy flux equations. Modeling has been done under the assumptions of identical front and back gate structures with the same gate oxide thicknesses and tungsten (with work function $\phi_M = 4.7\ eV$) as the gate electrode material for both of the gates of the device. In order to investigate the validity of the TCAD simulation software, we have first compared the TCAD simulation data with the experimentally measured data of an experimentally fabricated DG MOSFET structure reported by Liu et al.[27] The reasonably good matching of the TCAD results with the reported experimental data compared in Fig. 2 clearly demonstrates the validity of the ATLAS™ device simulation software used for the simulation of our proposed device structure in this paper. The TCAD data are thus used for validating the analytical model results presented in the following.

The variations of the central channel potential $\psi_{ci}(x) - \phi_f$ measured with respect to the Fermi potential $\phi_f = V_T \ln(N_a/n_i)$ as a function of lateral channel position have been shown for different combinations of σ_L and V_{DS} in Fig. 3, σ_L and V_{GS} of σ_L and L_G in Fig. 5while keeping the underlap length (L_{ul}) and other parameters constant. The central channel potential profiles shown in Figs. 3, 4, 5, and 6 clearly demonstrate that the decrease (increase) in source-to-channel barrier [i.e., increase (decrease) in the DIBL] with increase (decrease) in V_{DS}, V_{GS} and t_{si}; and decrease (increase) in L_G is stimulated further by the increase (decrease) in the straggle parameter value (σ_L). This may be attributed to the decrease (increase) in the S(D)-channel abruptness with the increase (decrease) in σ_L, which, in turn, reduces (increases) the effective channel length and hence increases (decreases) SCEs. Thus, unlike the uniformly doped S/D gate underlap DG MOSFETs, the value of the straggle parameter (σ_L) of the lateral Gaussian doping in the S/D region can be explored as an additional parameter for controlling DIBL and SCEs as well as the threshold voltage of the underlap DG MOSFETs. The combined effects of σ_L and underlap length L_{ul} on the threshold voltage (V_{thf}) have been demonstrated by plotting the V_{thf} as a function of L_{ul} in Fig. 6 for different values of σ_L but fixed values of other device parameters. It is observed that, for a fixed value of L_{ul} (and other device parameters), the threshold voltage (V_{thf}) is decreased with the increase in σ_L as evidenced from the potential profiles shown earlier in Figs. 3, 4, 5, and 6. Further, for a fixed value of σ_L, the threshold voltage roll-off is observed to be increased with the decrease in the gate underlap spacer length L_{ul} due to enhanced SCEs. It is also observed from Fig. 7 that the roll-off becomes the lowest for $\sigma_L \sim 3$ nm for all values of the underlap length considered in the

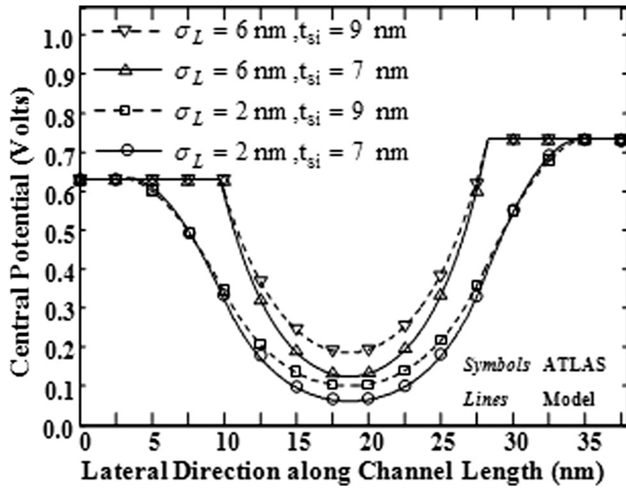

Fig. 5. Central potential along channel length, parameters used: $V_{GS} = 0.1$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $V_{GS} = 0.1$ V, $t_{ox} = 1$ nm.

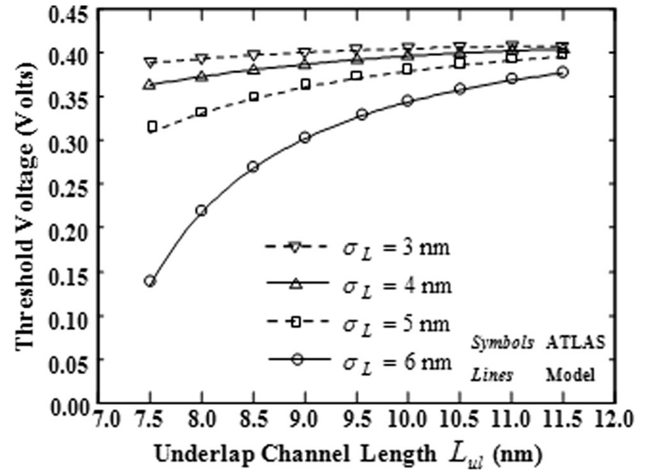

Fig. 7. Threshold voltage versus underlap channel length for different values of σ_L parameters used: $t_{si} = 7$ nm, $t_{ox} = 1$ nm, $V_{DS} = 0.1$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm.

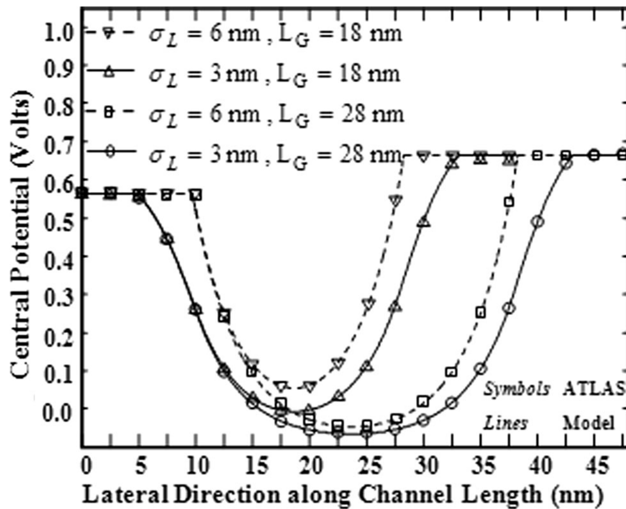

Fig. 6. Central potential along channel length, parameters used: $V_{DS} = 0.1$ V, $t_{si} = 7$ nm, $L_{ul} = 10$ nm, $V_{GS} = 0.1$ V, $t_{ox} = 1$ nm.

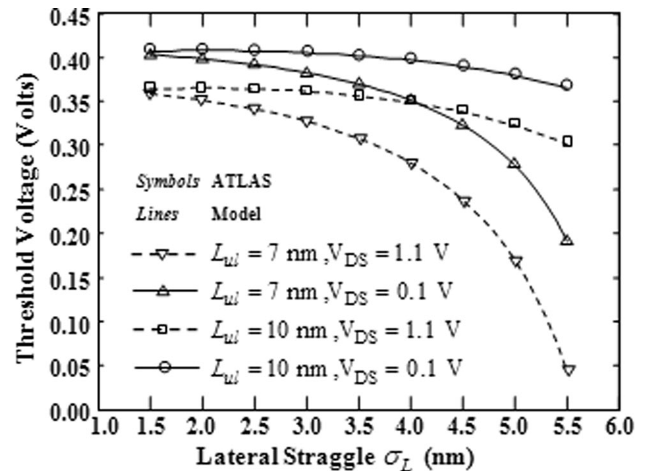

Fig. 8. Threshold voltage versus lateral straggle for different values of L_{ul} and V_{DS} parameters used: $t_{si} = 7$ nm, $t_{ox} = 1$ nm, $L_G = 18$ nm.

present study. Clearly, the threshold voltage roll-off of underlap DG MOSFETs with a lateral Gaussian doping profile S/D region can be optimized by selecting a suitable value of the lateral straggle parameter σ_L of the profile. To investigate further the effect of σ_L on the threshold voltage, the variation of threshold voltage as a function of σ_L for two pairs of L_{ul} and V_{DS} values has been plotted in Fig. 8. Clearly, V_{thf} is decreased with the increased value of σ_L as well as V_{DS} for all values of L_{ul}. However, the smaller difference between the threshold voltages for $L_{ul} = 10$ nm, $V_{DS} = 1.1$ V and $L_{ul} = 10$ nm, $V_{DS} = 0.1$ V pair than the difference between the threshold voltages for $L_{ul} = 7$ nm, $V_{DS} = 1.1$ V and $L_{ul} = 7$ nm, $V_{DS} = 0.1$ V pair observed in Fig. 8 implies that the smaller DIBL (i.e., better SCEs) is achieved for 10 nm than that for the 7-nm underlap length devices. Figure 9 shows the variation of the V_{thf} as a function of the gate oxide thickness t_{ox} for different values of σ_L and L_G. The V_{thf} is observed to be decreased with increased t_{ox}, decreased L_G and increased σ_L due to the increased SCEs. The variation of V_{thf} with t_{ox} for two sets of values of L_{ul} and σ_L plotted in Fig. 10 shows that deterioration of threshold voltage (DIBL) with the increase in σ_L is smaller for $L_{ul} = 10$ nm than that for $L_{ul} = 7$ nm device. Similarly, Fig. 11 demonstrates the decrease V_{thf} with the increased channel thickness (t_{si}), and σ_L, but decreased channel length L_G. The plot of V_{thf} versus t_{si} for two sets of σ_L and L_{ul} values in Fig. 12 confirms the smaller degradation of V_{thf} of underlap DG MOSGETs with $L_{ul} = 10$ nm than that of the devices with $L_{ul} = 7$ nm underlap lengths. The threshold voltage degradation shown in Figs. 11 and 12 with the increased channel thickness may be attributed to the reduction in the gate control over the channel carriers owing to the decrease in the L_{eff}/t_{si} ratio. We now consider the DIBL characteristics as a function

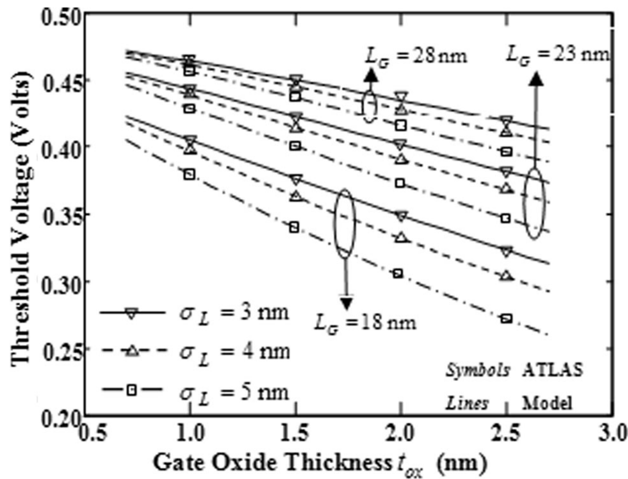

Fig. 9. Threshold voltage versus gate oxide thickness for different values of σ_L and L_G parameters used: $V_{DS} = 0.1$ V, $L_{ul} = 10$ nm, $t_{si} = 7$ nm.

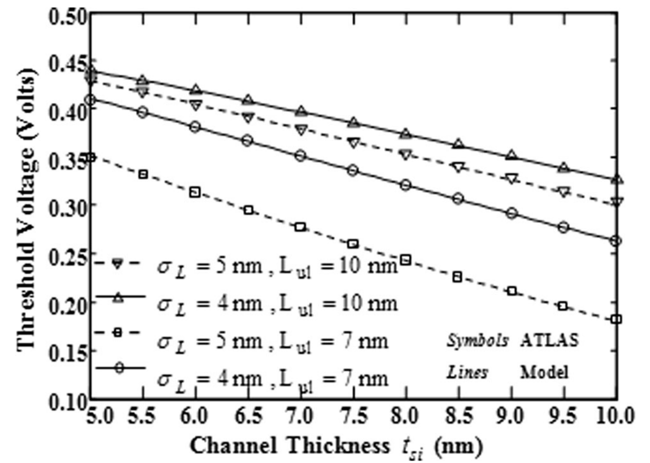

Fig. 12. Threshold voltage versus channel thickness for different values of σ_L and L_{ul} parameters used: $V_{DS} = 0.1$ V, $L_G = 18$ nm, $t_{ox} = 1$ nm.

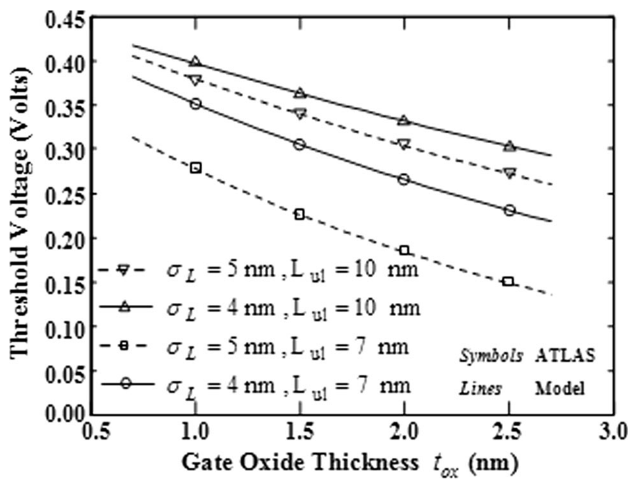

Fig. 10. Threshold voltage versus gate oxide thickness for different values of σ_L and L_{ul} parameters used: $V_{DS} = 0.1$ V, $L_G = 18$ nm, $t_{si} = 7$ nm.

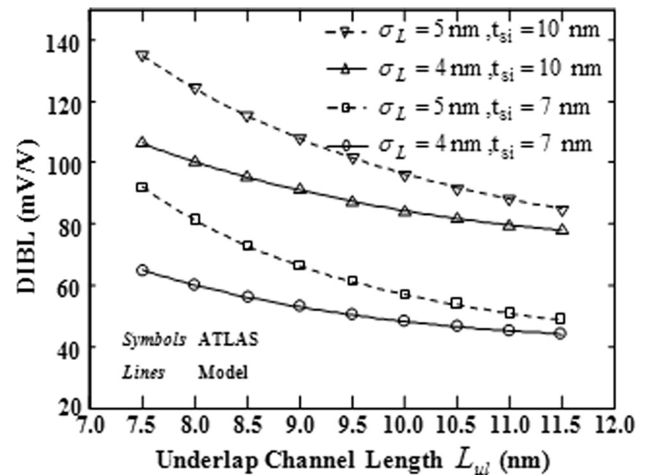

Fig. 13. DIBL versus underlap channel length for different values of σ_L and t_{Si} parameters used: $V_{DS} = 0.1$ V, $L_G = 18$ nm, $t_{ox} = 1$ nm.

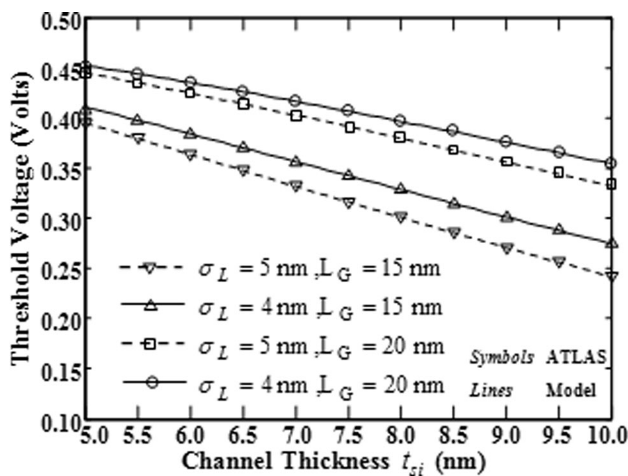

Fig. 11. Threshold voltage versus channel thickness for different values of σ_L and L_G parameters used: $V_{DS} = 0.1$ V, $L_{ul} = 10$ nm, $t_{ox} = 1$ nm.

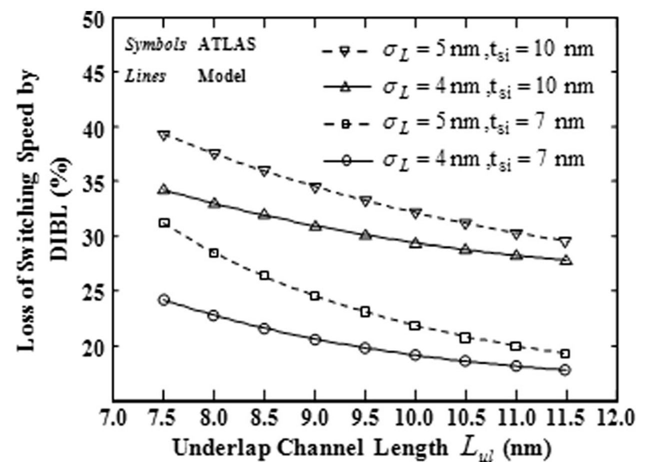

Fig. 14. Loss in switching speed by DIBL versus underlap channel length for different values of σ_L and t_{Si} parameters used: $V_{DS} = 0.1$ V, $L_G = 18$ nm, $t_{ox} = 1$ nm.

of the underlap length L_{ul} shown in Fig. 13. It is observed from the figure that, while the DIBL is decreased with L_{ul}, it is increased with both the channel thickness (t_{si}) and lateral σ_L. The deteriorations of the DIBL at larger channel thickness and larger σ_L are attributed to the poor control of the gate over the channel carriers and decrease in the source-channel abruptness respectively, as discussed earlier. Finally, the loss of switching speed described by Eq. 44 due to the DIBL has been plotted in Fig. 14. The loss is found to be ~3% to 4% lesser in the underlap DG MOSFET devices with body thickness of $t_{si} = 7$ nm than the devices with $t_{si} = 10$ nm with every ~ 1 nm increase in the value of σ_L. Thus, the loss in switching speed of the DG MOSFETs can be optimized by controlling the values of the additional parameters σ_L and L_{ul} introduced with the USJ underlap DG MOS structures considered in the present study.

CONCLUSION

A comprehensive analytical study has been presented for the modeling of 2D potential distribution and threshold voltage of underlap DG MOSFETs with lateral Gaussian doping in the S/D regions. Parabolic approximation along with the conformal mapping technique has been used for obtaining the potential function by solving the 2D Poisson's equation with suitable boundary conditions. The effects of the lateral struggle parameter (σ_L) and the underlap length (L_{ul}) on the potential distribution, threshold voltage, DIBL and switching speed of the devices have been analyzed in details. While the threshold voltage was decreased with the increase in σ_L, the same was observed to be improved with the increase in L_{ul}. The DIBL, threshold voltage roll-off, and loss of switching speed were also found to be deteriorated with the increase in σ_L but can be improved with the increase L_{ul}. Noticeable control of the threshold voltage with the control of σ_L and L_{ul} parameters may be explored for achieving a higher drive current with lower SCEs in the underlap DG MOS device structures with lateral Gaussian doping in S/D over the conventional DG MOSFETs. Proper optimization between the geometrical parameters and doping profile parameters should be made in order to make a healthy trade-off among the drive current, SCE and electrostatic integrity of the device. Thus, the USJ underlap DG MOSFETs with lateral Gaussian doping S/D structures can be considered as a potential candidate both for high drive current and better switching speed. An excellent agreement between the analytical results and the ATLAS™ based TCAD simulation data confirms the validity of our proposed model.

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