Journal of ELECTRONIC MATERIALS, Vol. 45, No. 1, 2016
DOI: 10.1007/s11664-015-4074-0

Interfacial Electrode-Driven Enhancement of the Switching Parameters of a Copper Oxide-Based Resistive Random-Access Memory Device

L.D. VARMA SANGANI,[1] CH. RAVI KUMAR,[1] and M. GHANASHYAM KRISHNA [1,2]

1.—Centre for Advanced Studies in Electronics Science and Technology, School of Physics, University of Hyderabad, Hyderabad, Telangana 500046, India. 2.—e-mail: mgksp@uohyd.ernet.in

The characteristics of an Au/Cu_xO/Au bipolar resistive random-access memory device are reported. It is demonstrated that switching parameters of this device structure can be enhanced by introducing an interfacial Al layer between the Au top electrode and the Cu_xO-based dielectric layer. The set and reset voltages are, respectively, between −2.5 V to −6.0 V and +1.2 V to +3.0 V for the Al-based device. In contrast, the range of values are −0.5 V to −2.5 V and +0.5 V to +1.5 V for the set and reset voltages in the absence of Al. The Al-based device has a higher low resistance state value of 5–6 KΩ as compared to the 0.3–0.5 KΩ for the Au-based device, which leads to a 12 times lower power dissipation factor and lower reset current of 370 μA. Endurance studies carried out over 50 switching cycles show less than 2% variation in both the low resistance and high resistance values. The conduction is ohmic at low values of bias and non-ohmic at higher bias voltage which shows that the enhanced behaviour is a result of the formation of an insulating aluminum oxide layer at the Al-Cu_xO interface.

Key words: RRAM, resistive switching, copper oxide, interfacial electrode, low reset current, low leakage current

INTRODUCTION

The development of non-volatile, random-access memories has been the focus of intense research in the last few years. Resistive random-access memories (RRAMs) belong to this class of devices and have received considerable attention due to their simple structure and possibility of high speeds.[1–3] They exhibit characteristics that compare favorably with existing non-volatile memories such as flash-memory, magnetic and phase-change random-access memories. However, there are many challenges that need to be addressed before RRAMs can achieve commercial viability. These include optimization of (1) properties of transition metal oxides (TMOs) such as Cu_xO ($1 \le x \le 2$), TiO_2, NiO, HfO_2 used as dielectrics, (2) fabrication processes and (3) device structures.[1,4–8] One of the TMOs under active consideration is copper oxide which is intrinsically a p-type semiconductor, but can be grown either as direct band gap CuO or indirect band gap Cu_2O, enabling the possibility of fast switching (up to 100 ns for the set operation) and multi-bit operation.[2,3,6,9–15] Notwithstanding the progress made in copper oxide-based RRAM devices, some issues such as high reset and leakage current still need to be resolved. Reset current and sneak leakage must be reduced to enable low-power devices and, in particular, sneak leakage current from other devices in the matrix should be reduced to increase the density of RRAM matrix array.[4] Different strategies have been adopted to solve this problem. For example, Hyung et al. introduced a Ni interfacial layer to reduce the reset current of unipolar NiO-based RRAM device.[16] Wu et al. demonstrated an

(Received March 14, 2015; accepted September 18, 2015; published online October 16, 2015)

AlO_x-based device with low reset current as well as higher resistance in the low resistance state (LRS).[17]

In the present work, the role of an interfacial metal layer between the resistive oxide (Cu_xO, $1 \le x \le 2$) and the top electrode, Au, is examined. Two device structures were fabricated for comparison; the first device consisted of a Cu_xO layer sandwiched between Au electrodes (Au/Cu_xO/Au) and the second device consisted of a Cu_xO layer with Au as the bottom electrode but included Al as an interface layer between the oxide and top Au electrode (Au/Al/Cu_xO/Au). It is shown that the Al interface layer enhances the resistive switching characteristics of the fabricated RRAM device.

EXPERIMENTAL METHODS

The materials comprising the different layers of the device were first optimized for thickness, morphology and structure. The Au films, of 100-nm thickness, were deposited by thermal evaporation at a pressure of 5.0E−5 mbar. The Cu films, of 50-nm thickness, were deposited by radio frequency magnetron sputtering from a cathode of 50-mm diameter in a pure Ar atmosphere at a pressure of 1.8E−2 mbar followed by post-deposition annealing in air at 250°C for 4 h to obtain the oxide film. The interfacial Al layer, of 50-nm thickness, was then deposited on the thermally oxidized Cu layer by thermal evaporation at a pressure of 5.0E−5 mbar. This was followed by Au metal deposition as described earlier. All device structures were fabricated using a photo lithography technique with the process flow of lithography, deposition and liftoff. A positive tone *i*-line photo-resist was used and an ultraviolet (UV) mask aligner (MJB4 of Suss Microtech) was used for photoresist exposure.

Two device structures of 20 × 20 μm^2 area were then fabricated; D1 with Au/Cu_xO/Au and D2 with Au(top)/Al/Cu_xO/Au (bottom) as shown in the schematic views in Fig. 1a and b, respectively.

The crystal structures of the films were examined by x-ray diffraction (XRD) using a Cu Kα line of a 0.15406-nm wavelength. The microstructures of the films were imaged in a field emission scanning electron microscope (FE-SEM Model Ultra55, Carl Zeiss, Germany). The morphologies of the films were observed with an atomic force microscope (AFM Model NT–MDT of Solver Pro M) in semi-contact mode using a cantilever with a force constant of 10 Nm^{-1}. X-ray photoelectron spectroscopy (XPS) measurements were carried out using a PHI 5000 Versa Probe II scanning XPS microprobe with a monochromatic Al Kα source (1486.6 eV). The current–voltage (*I–V*) characteristics and endurance measurements of the memory cells were carried out using a semiconductor device analyzer (Agilent B1500A). A voltage sweep was used for current–voltage measurements as well as for the endurance property measurements of the memory cell. The sweep was applied to the top electrode and the bottom electrode was grounded.

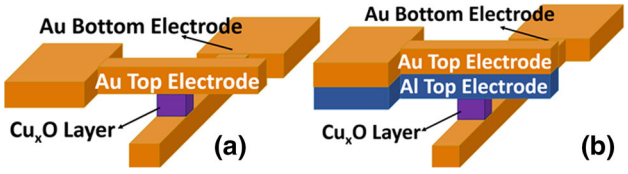

Fig. 1. Schematic views of two device structures fabricated; (a) D1 with Au/Cu_xO/Au and (b) D2 with Au(top)/Al/Cu_xO/Au (bottom).

RESULTS AND DISCUSSION

The XRD patterns of the Au, Cu and thermally oxidized Cu films are shown in Fig. 2a–c, respectively. The XRD data reveals that all the three layers are crystalline with Au displaying a Bragg reflection along the (111) plane and Cu film exhibiting the (111) and (200) peaks. The Cu film, on thermal oxidation, showed two peaks which can be assigned to Cu_2O (111) and CuO (111), respectively, and confirms the film was Cu_xO ($1 \le x \le 2$).

The FE-SEM and AFM images of these films are displayed in Fig. 3a–f. The FE-SEM images in Fig. 3a–c reveal a densely packed granular microstructure in all the films. The AFM images in Fig. 3d–f show that the bottom gold electrodes are reasonably smooth and the root mean square roughness values, at two different locations over 5 × 5 μm^2 areas, are 3.5 nm and 3.6 nm. The root mean square roughness values of the Cu and Cu_xO films, at two different locations over 5 × 5 μm^2 areas, are 8.9 nm, 19.8 nm and 7.6 nm and 18.1 nm, respectively.

The resistive switching characteristics of the devices D1 and D2 are shown in Fig. 4a. In both cases, it is observed that with gradual increase in negative bias, there is a gradual increase in the current through the device up to the set voltage (indicated in the figure). The set voltage for D1 is −1.7 V whereas it is −3.5 V for D2. At this point there is

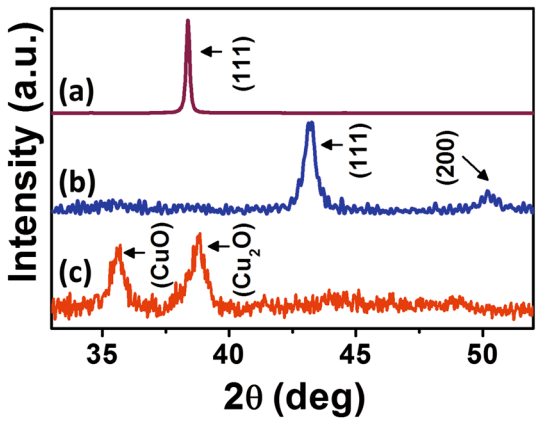

Fig. 2. The XRD patterns of the Au, Cu and thermally oxidized Cu films are shown in top (a), middle (b) and bottom (c), respectively.

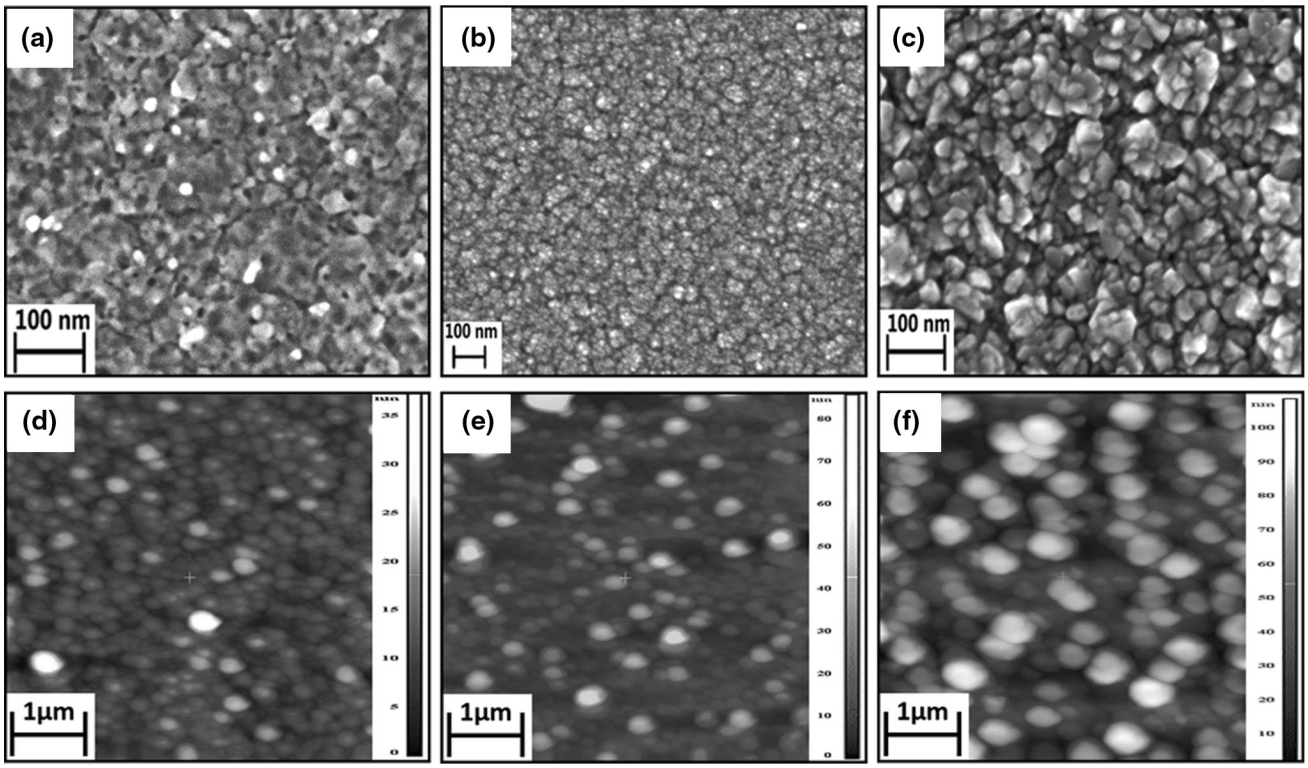

Fig. 3. (a)–(c) are the SEM images and (d)–(f) are the AFM images of the Au, Cu and thermally oxidized Cu films, respectively.

sudden increase in current for both the devices and a compliance current is reached. This is the transition from the high-resistance state (HRS) to the low-resistance state (LRS), called the set process. The switching process of device D2 is shown in the Fig. 4b, and device D1 also followed similar process cycles with different slopes, and set and reset voltages. From the Fig. 4b, the hysteretic behavior in both devices is evident when bias from the set voltage is decreased towards zero and the path taken in cycle 2 is different from the cycle 1. Cycle 3 represents the *I–V* behavior with an increase in positive bias up to the reset voltage, at which point there is a transition from the LRS to HRS. The reset voltage and currents are +1.2 V and 2.0 mA, respectively, for D1 in comparison to +1.7 V and 0.4 mA for D2. The hysteretic behavior is again evident when the bias voltage is decreased to 0 V in both cases in cycle 4. As part of this study, 16 devices were fabricated and the lowest resistances in the LRSs are 0.4 KΩ and 5.5 KΩ for D1 and D2 respectively, while the corresponding HRS values are 45 KΩ and 54 KΩ, respectively. A review of literature shows that these values compare favorably with reported values.[2,6,11] The forming voltages of the devices D1, D2 are −3.1 V, −6.0 V, respectively. The switching speed of the devices was on the order of micro seconds. Clearly this needs improvement. It is evident that the devices are bipolar RRAM devices and their behavior is asymmetric in nature. The endurance behavior tested for device D2 over 50 cycles shows that the device is stable, as evidenced from the typical *I–V* characteristic displayed in Fig. 4c and d. The resistance variation is less than 2% in both LRSs and HRSs over 50 cycles. From Fig. 4d, the HRS to LRS windows are 100× and 10× for the devices D1 and D2, respectively. To understand the mechanism of charge transport, double-log *I–V* plots were plotted, as shown in Fig. 5a and b for both the devices. The slopes of linear fitting curves of both the devices in the LRS are nearly equal to one which indicates that the devices are ohmic in nature in the LRS. This ohmic behavior in the LRS supports the filamentary conduction mechanism wherein filaments are formed by de-oxidation of Cu_xO due to a high electric field applied between the electrodes at the set process. The switching into the HRS can be attributed to rupturing and re-oxidation of small portions of the filaments in proximity to the electrode, due to heat generated by high current density in the filament at the reset process. The schematic of devices D1 and D2 and the filament formation and rupturing processes are depicted in Fig. 6a–e.

The significant effects of introduction of the interfacial layer is doubling of reset voltage, decrease in read, set currents by one order and decrease in resistance window by one order. For a reliable bistable storage device, a 10× window is considered significant. Hence, the reset voltage and set current are the parameters that can be used to derive information about device performance.

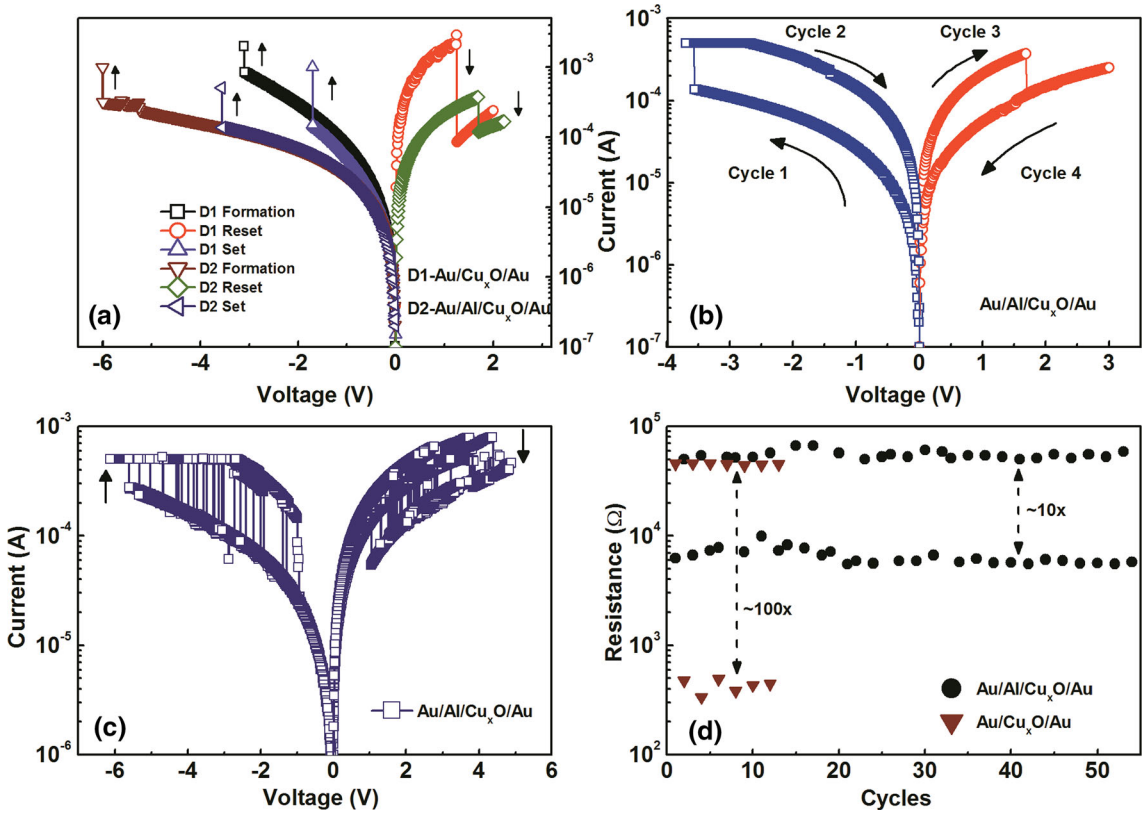

Fig. 4. (a) The resistive switching characteristics of the devices D1 and D2. (b), (c) Switching process cycles and the endurance behavior tested over 50 cycles of the device D2, respectively. (d) HRS and LRS resistance values of both the devices D1 and D2 for different cycles.

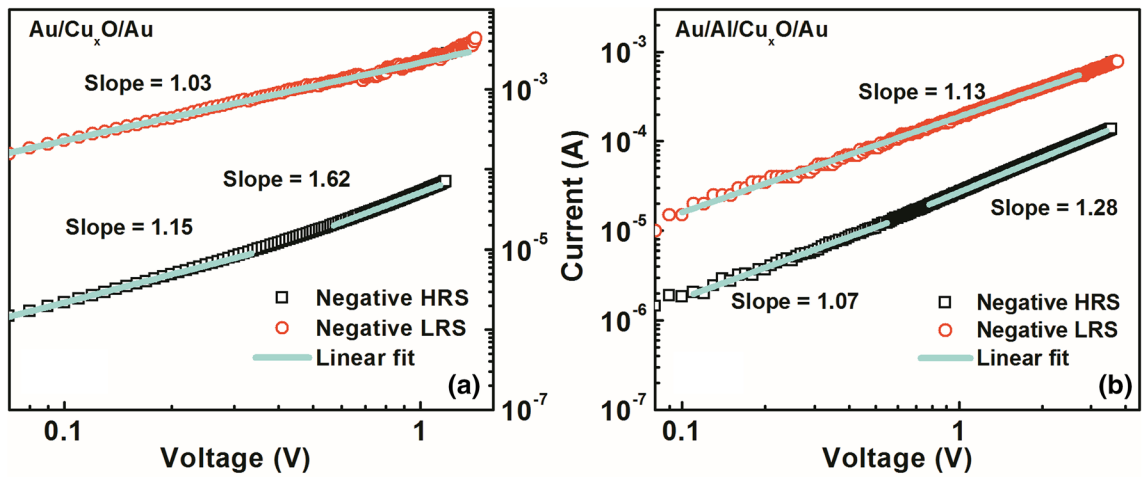

Fig. 5. (a), (b) The double-log *I–V* plots, linear fittings for the devices D1, D2, respectively.

However, since it is quite difficult to derive information directly from these parameters, it is necessary to perform power consumption calculations for the device as it is a combination of both voltage and current. Power consumption must be low for a good device.

To quantify this effect in terms of device performance, the power dissipation ratio of the devices was calculated. It is well known that ohmic loss (I^2R loss) must be low for a low-power RRAM device. This, in turn, this means that the device should have a low I_{reset} and a high LRS resistance value, in order to reduce the I^2R loss in the read process as well as in the reset process. The power dissipation ratio at the LRS or at the reset process of both the devices is calculated below,

$$\text{Power dissipation ratio at LRS} = P_{D1}/P_{D2} \quad (1)$$

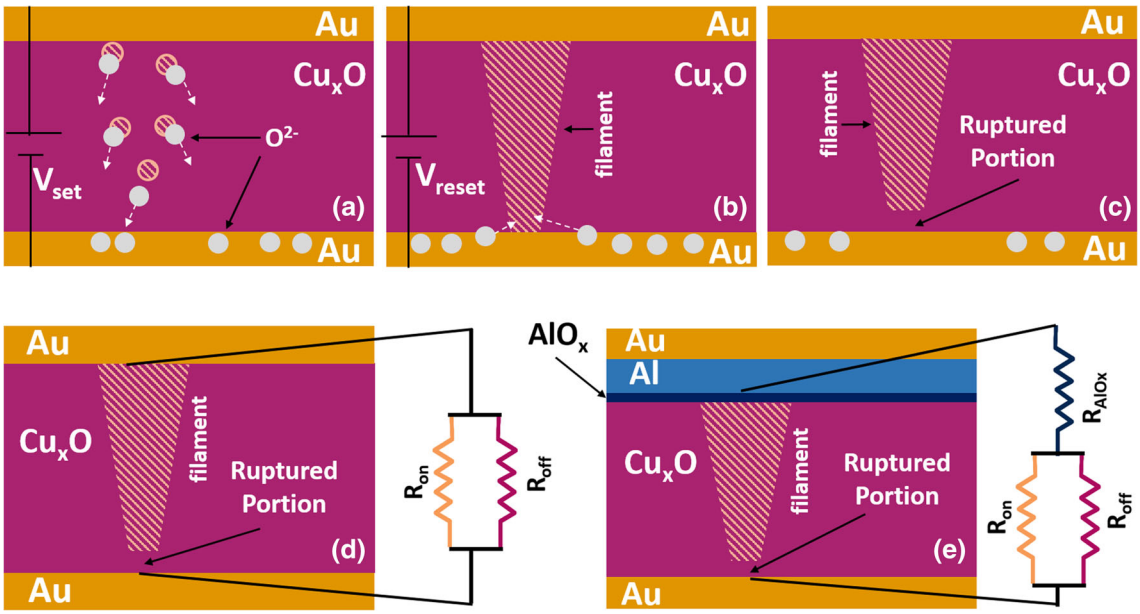

Fig. 6. Schematic diagram of (a) filament formation in an as-prepared cell due to de-oxidation at V_{set}, (b) De-oxidation of a portion of the filament at V_{reset}, (c) HRS with ruptured portion after the reset process. The different interfaces in the devices D1 and D2 are schematically displayed in (d) and (e) respectively.

where P_{D1} is the power dissipation in D1 and P_{D2} is the power dissipation in D2

$$P_{D1}/P_{D2} = (I_{2reset}/I_{1reset})^2 (R_{2LRS}/R_{1LRS}) = 12\,(\text{approx.}) \quad (2)$$

From the above calculations, it is evident that the power dissipation in the Al-based device is 12 times lower than the device without the interfacial layer. LRS resistance or ON resistance (R_{on}) also affects the density of the device matrix. Leakage current from other devices plays a crucial role in reading the correct state (LRS or HRS) of a device in a cross-bar device matrix array. Leakage current increases with an increasing density of the matrix array, limits the matrix size, and high LRS resistance leads to a low leakage current.[4] This would suggest that, in the present case, the device D2 (Au/Al/Cu$_x$O/Au) is superior to D1 (Au/Cu$_x$O/Au) due to its one order higher resistance in the LRS.

The results presented above demonstrate that the presence of the interfacial Al layer causes significant changes in the resistive switching characteristics of the device. It is pertinent to note that in the device D1 (Au/Cu$_x$O/Au), there are two interfaces; one between the top of Au and bottom of Cu$_x$O and the other between the top of the Cu$_x$O layer and the bottom of the Au top electrode. The interfacial Al layer between Cu$_x$O and Au introduces two new interfaces in D2 (Au/Al/Cu$_x$O/Au), one of which is between the top of the Cu$_x$O and bottom of the Al layer and the other is between top of the Al layer and bottom of the Au top electrode. The interfaces are schematically displayed in Fig. 6d and e. It is, thus, possible to correlate the difference in behavior of the devices D1 and D2 with the nature of charge transport at these two "new" interfaces. The possible metal–metal oxide interfaces in the present case are Au–Cu$_x$O, Al–Cu$_x$O and possibly an Au–AlO$_x$ interface. The formation of AlO$_x$ is possibly due to the low heat of formation of Al$_2$O$_3$ (−1582 kJ/mole at 300 K[18]), as a result of which Al can be easily oxidized even during deposition of Al by thermal evaporation.[19] Au-Cu$_x$O is the common interface in both the devices and, hence, it can be speculated that the change may either be due to the Al–Cu$_x$O interface or the Au–AlO$_x$ interface. To verify which one of these interfaces is contributing to the observed behavior, a test structure consisting of Au/Al/

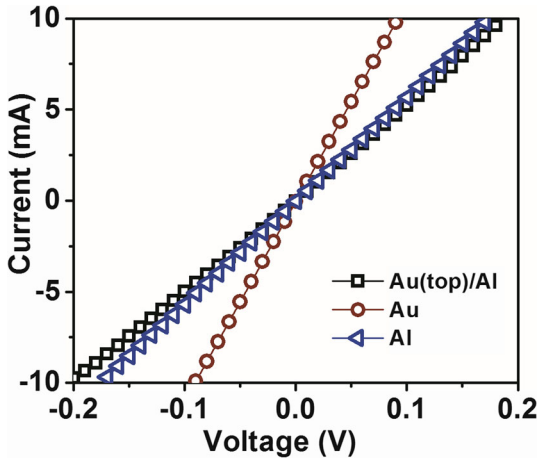

Fig. 7. *I–V* characteristics of the Au/Al/Au structure.

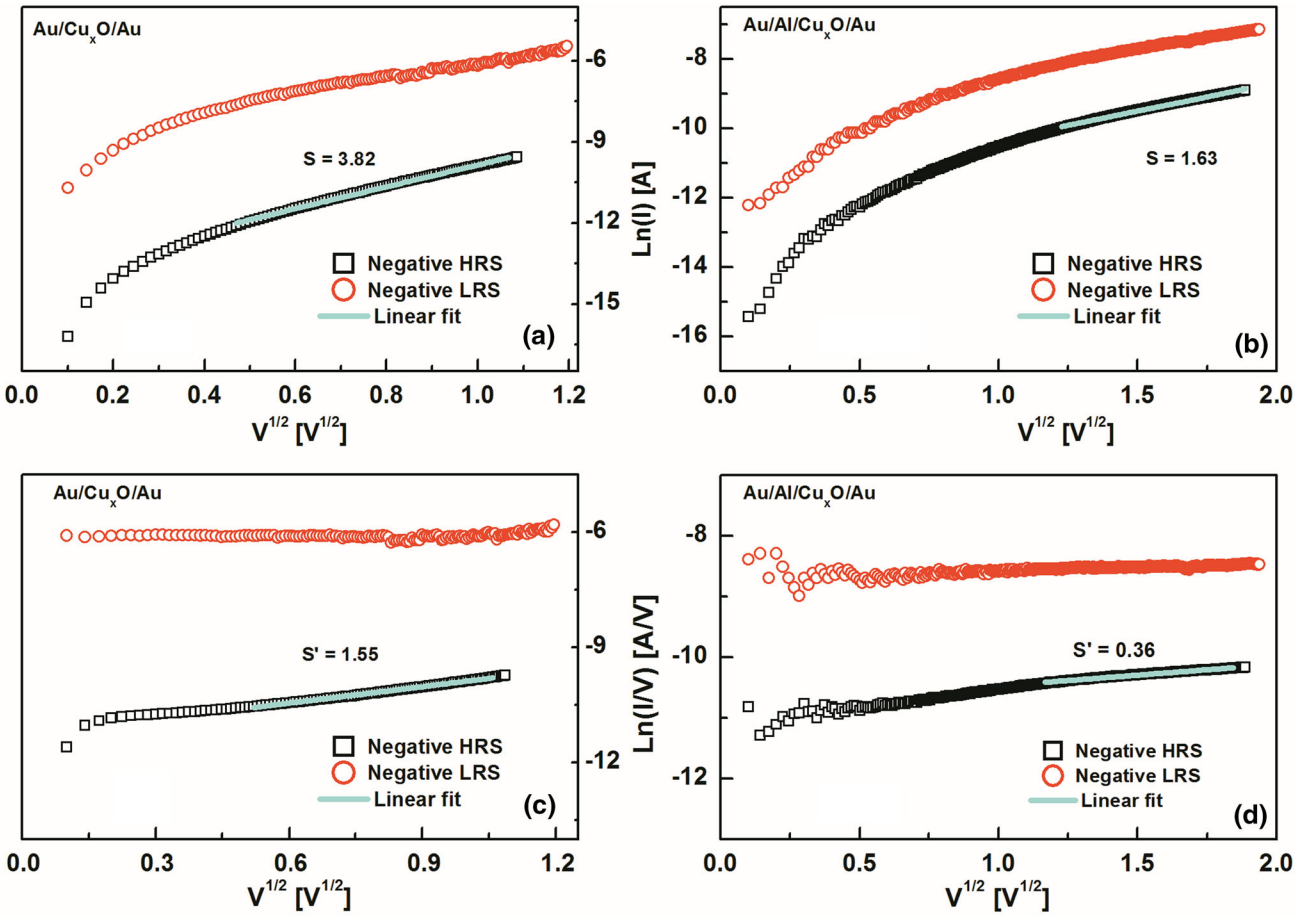

Fig. 8. Fitting of measured data using (a), (b) Schottky model and (c), (d) Poole–Frenkel model for the devices D1, D2, respectively.

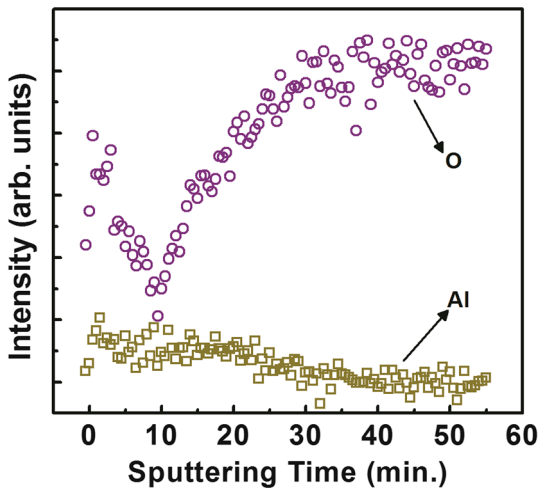

Fig. 9. XPS depth profile on a typical 20-nm Al thin film deposited on Cu_xO film.

Au was fabricated. *I–V* characteristics of this structure shown in Fig. 7 confirmed that Au/Al contact was ohmic in nature, indicating the absence of an insulating AlO_x layer at that interface. It has been demonstrated that switching in the RRAM device occurs at the metal–metal oxide interface.[17,20,21] The inference from this experiment is that the increase in LRS and HRS resistances in the Al-based device is a consequence of the formation of an insulating AlO_x layer at the Al–Cu_xO interface and the sandwich structure is equivalent to two resistors in series. It was confirmed by XPS studies that the AlO_x forms during deposition itself, as discussed later. Furthermore, the differences between the LRS and HRS resistances of both the devices (D1 and D2) are nearly the same. This indicates that the AlO_x layer is only acting as an additional resistance and not switching between the LRSs and HRSs like Cu_xO.

It is evident that the high voltage region of the HRS showed non-ohmic behavior for both the devices with the slopes of the linear regions being greater than one in both cases. Significantly, the slope is lower for D1 in comparison to D2. To further understand the differences in behaviour between devices D1 and D2, the data was fitted using the Schottky (SC) model for device D1, as shown in Fig. 8a and b, and the Poole–Frenkel (PF) model for device D2, as shown in Fig. 8c and d. The dielectric constants for devices D1 and D2, respectively, were

calculated from the SC model (Eq. 3) and PF model (Eq. 4),[22]

$$\varepsilon_{SC} = \frac{q^3}{(kTS)^2 4\pi\varepsilon_0 d} \quad (3)$$

$$\varepsilon_{PF} = \frac{q^3}{(kTS')^2 \pi\varepsilon_0 d} \quad (4)$$

where q is electron charge, k is Boltzmann's constant, T is temperature, S and S' are the slopes of SC and PF linear fits, respectively, ε_0 is dielectric constant of free space and d is the thickness of the oxide film. The calculated dielectric constants using Eqs. 3 and 4, are, respectively, 2.6 and 78.5 for D1 in contrast to 16.2, and 133 for D2. It is evident that both models indicate a higher dielectric constant for the Al-based device D2 than that for D1.

The reason for the higher dielectric constant is the modification of the Al-Cu_xO interface due to formation of a thin layer of AlO_x at the interface. This was confirmed from the XPS depth profile carried out on a typical 20-nm Al thin film deposited on Cu_xO film under the same conditions as the film used in device D2. The XPS depth profile, in Fig. 9, shows the presence of Al and Oxygen in the first 10 min of sputtering, indicating surface oxidation of Al and confirms oxidation of the Al layer during deposition. Therefore, the probability of $CuAlO_x$ has been ruled out.[19]

CONCLUSIONS

In summary, the role of an interfacial Al electrode in improving switching parameters of an Au/Cu_xO/Au device was investigated. In the absence of Al, the device operates at a relatively high reset current accompanied by a higher LRS leading to a low-power device. In contrast, reduction in reset current was achieved for the Al-based Cu_xO RRAM device. The enhancement is shown to be due to the formation of an insulating aluminum oxide layer at the Al-Cu_xO interface. It is shown that, of the two oxides AlO_x and Cu_xO which are in series, only Cu_xO participates in the switching process.

ACKNOWLEDGEMENTS

The first author acknowledges a UGC-RFSMS fellowship. Facilities provided by the School of Physics and the Central facility for Nanotechnology are also acknowledged. The DST-FIST-funded XPS facility at the Department of Physics and Meteorology, IIT Kharagpur is acknowledged.

CONFLICT OF INTEREST

The authors of this paper declare that there were no conflicts of interest in carrying out this work.

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