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High-Temperature (1200–1400°C) Dry Oxidation of 3C-SiC on Silicon

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In a novel approach, high temperatures (1200–1400°C) were used to oxidize cubic silicon carbide (3C-SiC) grown on silicon substrate. High-temperature oxidation does not significantly affect 3C-SiC doping concentration, 3C-SiC structural composition, or the final morphology of the SiO_2 layer, which remains unaffected even at 1400°C (the melting point of silicon is 1414°C). Metal-oxide-semiconductor capacitors (MOS-C) and lateral channel metal-oxide-semiconductor field-effect-transistors (MOSFET) were fabricated by use of the high-temperature oxidation process to study 3C-SiC/SiO_2 interfaces. Unlike 4H-SiC MOSFET, there is no extra benefit of increasing the oxidation temperature from 1200°C to 1400°C. All the MOSFET resulted in a maximum field-effect mobility of approximately 70 cm^2/V s.

Key words: SiC, high-temperature oxidation, conductance, AFM, SIMS, XRD, interface trap density, mobility

INTRODUCTION

There is renewed interest in cubic silicon carbide (3C-SiC), which can, potentially, be grown heteroepitaxially on 12-inch Si substrates, because it would result in a drastic reduction of the cost of SiC semiconductor devices compared with the successful but prohibitively expensive SiC hexagonal polytype technology (4H-SiC).[1] It has been reported that lateral power transistors manufactured from 3C-SiC could be suitable for the 1200-V range, and are an alternative to gallium nitride (GaN) heterojunction transistors for typical power applications in which normally-off operation is required.[2] Devices with these voltage ratings could be used in automotive and other domestic appliances and hence have huge potential for reducing the global carbon emissions.[3]

Because the band gap of the 3C polytype (2.2 eV) is smaller than that of the 4H polytype (3.2 eV), fewer traps lie within the energy bandgap of 3C-SiC in metal-oxide-semiconductor (MOS) structures, resulting in better field-effect mobility.[4] Unlike 4H-SiC/SiO_2 interfaces, little research has yet been performed on 3C-SiC/SiO_2. The oxidation chemistry of 3C-SiC is different from that of 4H-SiC.[5] For the Si face in 4H-SiC, it has been observed that mobility increases with decreasing D_{it}. To reduce the D_{it} of 4H-SiC MOS devices, it is a common practice to perform post-oxidation annealing of the interface in a gaseous environment (e.g. nitrogen or phosphorus).[6–10]

Recent reports on high-temperature oxidation of 4H-SiC have shown that this process could be beneficial for the 4H-SiC/SiO_2 interface.[11–14] It has been reported[12] that as-grown 4H-SiC oxidized at 1500°C resulted in a 4H-SiC MOSFET with maximum field-effect mobility of 40 cm^2/V s; here we investigate a similar effect for the 3C-SiC/SiO_2 interface. In this study, the highest temperature used for oxidation of 3C-SiC was 1400°C, because of the limit imposed by the melting point of Si (1414°C). Also, oxidation was conducted in 100% oxygen. As far as we are aware, oxidation temper-

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atures higher than 1200°C have never been used to fabricate 3C-SiC MOS devices.

EXPERIMENTAL

The material used for this study was purchased from Novasic. To fabricate lateral metal-oxide-semiconductor capacitors (MOS-C) we used a 3C-SiC/Si wafer with heterostructure grown on an on-axis *p*-type Si (001) substrate. The 3C-SiC epilayer was grown by metalorganic chemical vapor deposition at ~1350°C; it was an *n*-type semiconductor with a doping concentration, N_D, of ~0.5–1 × 10^{16} cm^{-3}. The thickness of the epilayer was approximately 10 μm. Lateral MOS-C structures were used to study the electrical properties of the interface. Circular MOS-C of diameter 300 μm were surrounded by a large-area metal grid so that the capacitance of the second capacitor was sufficiently high (inset of Fig. 1a) and could be neglected. Three batches of devices, each with produced with differ-

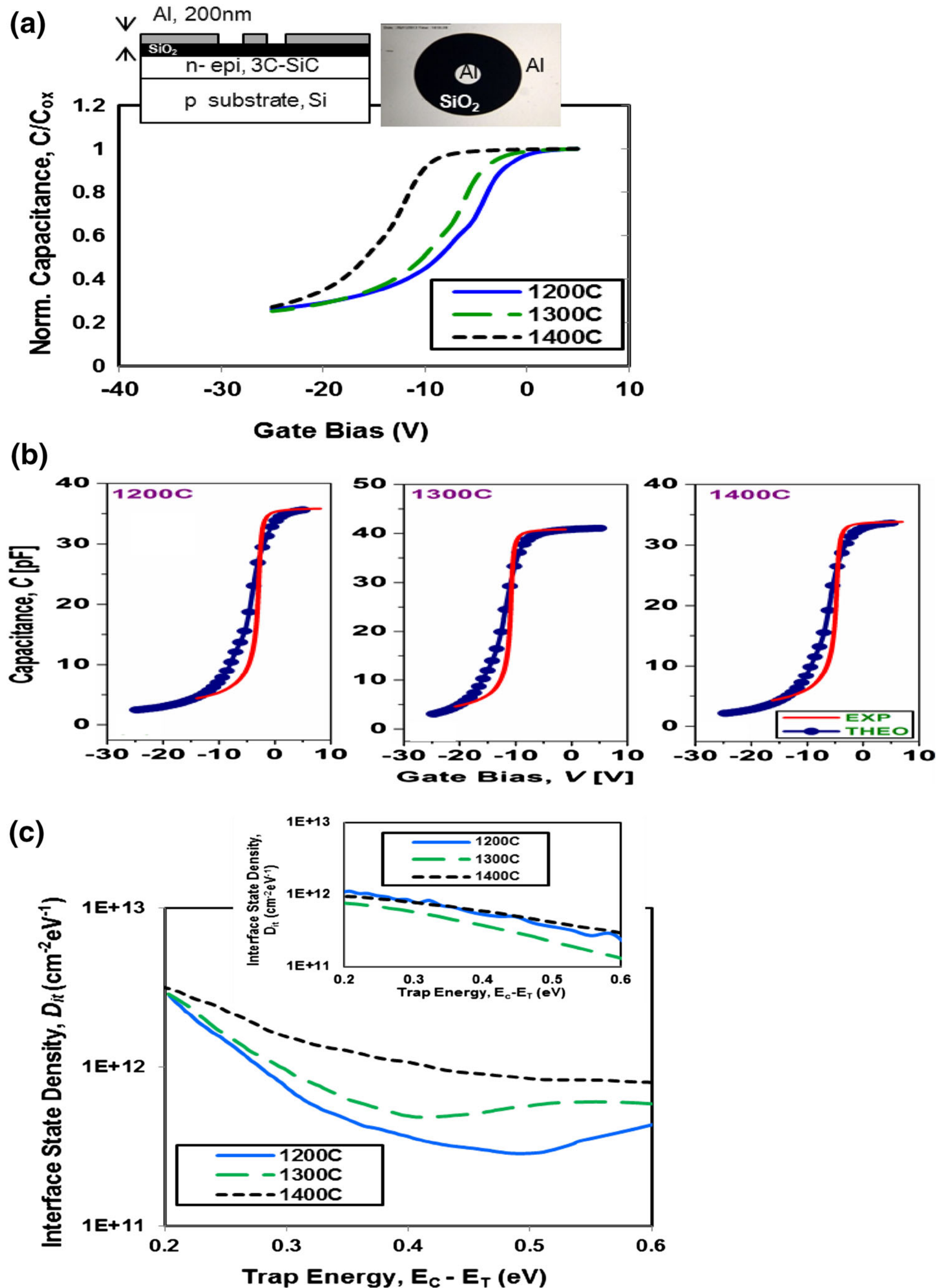

Fig. 1. (a) Typical 1-MHz *C*–*V* curves obtained from 3C-SiC MOS capacitors with thermal oxides grown at 1200°C, 1300°C, and 1400°C. (b) Comparison between the ideal and experimental *C*–*V* curves for each temperature. (c) Interface state densities (D_{it}) for 3C-SiC MOS structures, calculated by use of Terman *C*–*V* and conductance (inset) methods.

ent oxidation temperatures (1200°C, 1300°C, and 1400°C), were investigated during the course of this study. Device fabrication began with standard organic and Radio Corporation of America (RCA) cleaning to degrease the sample and remove metal and alkali metal ion contamination. Dry thermal oxidation was then performed at the aforementioned temperatures followed by 30 min Ar annealing at the temperatures used for oxidation. Single-exposure lithography and lift off procedures were used to define the pattern. Al (200 nm) was deposited as gate metal by use of an e-beam evaporator. Terman and conductance methods were used to analyze the interface. In addition, lateral n-channel MOSFET were fabricated to extract the field-effect mobilities (μ). Planar MOSFET were fabricated on the same substrate and used to fabricate a MOS-C. First, a quarter inch of wafer was implanted with aluminium (Al) at different energies (35 keV to 500 keV) and doses (3×10^{12} cm^{-2} to 2.2×10^{13} cm^{-2}) to form a 700 nm p-region. The Al implants were activated at 1350°C for 2 h in argon (Ar) which resulted in $N_A \sim 5 \times 10^{16}$ cm^{-3}. The surface was protected by use of a carbon cap during activation. The cap was removed by use of an O_2 plasma. Source and drain regions (400 × 200 μm) were formed by nitrogen implantation at 700°C with different energies (20–150 keV) and doses (1×10^{15} cm^{-2} to 5.4×10^{15} cm^{-2}) to form a 8×10^{20} cm^{-3} box profile with an $n+/p$ junction depth of approximately 300 nm. Again, the surface of the implanted p-epilayer was protected with a carbon cap during activation of the nitrogen implants at 1350°C for 2 h in Ar. A thin sacrificial oxide layer (~20 nm) was used to remove surface damage before growth of a gate oxide layer. Source and drain ohmic contacts were formed by evaporation of 10 nm Ti and 200 nm Ni. Ohmic annealing of source and drain contacts was performed at 1000°C in Ar for 1 min. Finally, Al gate contacts were deposited. The channel length and channel width of the lateral MOSFET were 120 μm and 400 μm, respectively.

RESULTS AND DISCUSSION

Figure 1a shows normalized C–V curves at 1 MHz for the ≥different MOS-C. These curves have three distinct features:

- a large flat-band voltage shift ($\Delta V_{FB} = V_{FB,i} - V_{FB,ideal}$) toward negative gate bias;
- increased capacitance on depletion; and
- large stretching of C–V characteristics.

The subscript "i" stands for the different processing conditions used to grow the gate oxide: i = 1, 2, and 3 for oxidation at 1200, 1300, and 1400°C oxidation, respectively. Ideal (theoretical) and experimental C–V curves for each temperature are compared in Fig. 1b. The ideal C–V curve is obtained by solving the electrostatic and Poisson equations and assuming that the 3C-SiC/SiO_2 interface is perfect, i.e. with no defects near the interface, in the bulk of the oxide, or in the 3C-SiC. The doping value used in computations for the high-temperature-oxidized samples was $N_D = 0.63 \times 10^{16}$ cm^{-3} for the entire range of oxidation temperature, i.e., the 3C-SiC doping concentration seems to be stable even at 1400°C. The flat-band voltage shift shows the presence of a net positive fixed oxide charge at the interface. Its origin is believed to be the presence of carbon clusters, positively or negatively charged oxygen–hydrogen–carbon–silicon complexes, and dangling bonds formed after thermal oxidation.[15] Carbon clusters and dangling bonds (two dangling bonds per atom for the (100) surface) act as donor-like states; they are positively charged when empty and, as a result, give rise to a negative shift in V_{FB}; these results are consistent with previous findings.[16] Also, as mentioned above, all the curves are significantly stretched compared with the ideal

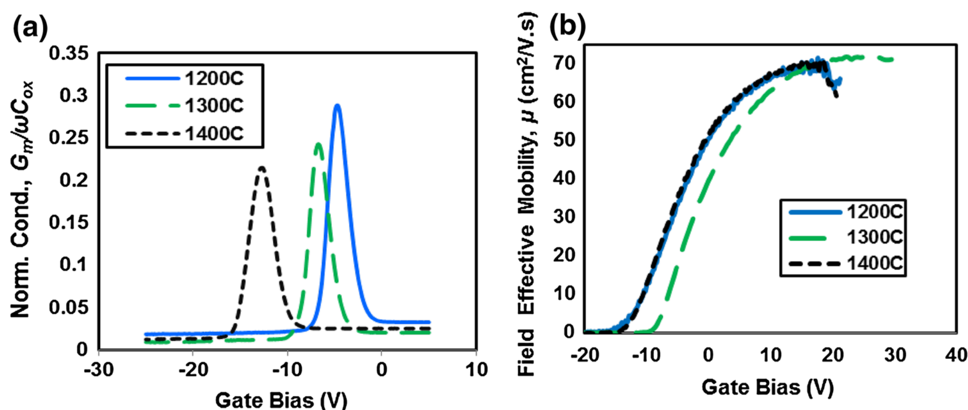

Fig. 2. (a) Normalized conductance curves of 3C-SiC MOS capacitors obtained for different gate voltages at probe frequency (ω) = 100 kHz. (b) Field-effect channel mobility as a function of gate bias for 3C-SiC MOSFET with gate oxides grown at different temperatures.

Table I. Summary of field-effect mobility, material, and processes used to grow gate oxides for fabricated 3C-SiC MOSFET. Mobility results for 3C-SiC MOSFET from the literature are also shown

Sample	Material	Process used to grow the gate oxide	Peak value μ	Ref.
3C-SiC/Si MOSFET (heteroepitaxial)	A *p*-type 3C-SiC, 2×10^{17} cm^{-3}, epilayer on a 2° off-axis *p*-type Si (001) substrate	Wet oxidation at 1150°C for 2.5 h, Ar annealing at 1150°C for 30 min, and re-oxidation at 950 C for 2 h	165 cm^2/V s	21
3C-SiC/SiC MOSFET (homoepitaxial)	Homoepitaxy grown *p*-type, 1×10^{16} cm^{-3}, 3C-SiC films	Pyrogenic oxidation (H_2:O_2 = 1:1) at 1100°C for 20 min	230 cm^2/V s	22
3C-SiC/SiC MOSFET (homoepitaxial)	An *n*-type, 5×10^{15} cm^{-3}, doped epilayer on 3C-SiC (001) substrate Al implants were used to realize a box profile with doping concentration of 1×10^{18} cm^{-3} to fabricate *n*-channel MOSFET	Dry thermal oxidation for 90 min at 1100°C in dry oxygen followed by post-oxidation annealing in wet oxygen at 950°C for 3 h	40 cm^2/V s	23
3C-SiC/Si MOSFET (homoepitaxial)	An *n*-type, 7×10^{15} cm^{-3}, doped epilayer on 3C-SiC (001) substrate Al implants were used to realize a box profile to fabricate vertical *n*-channel MOSFET	Thermal oxidation at 1150°C in H_2O containing O_2 gas/plasma enhanced CVD oxide deposition followed by a wet O_2 annealing at 950°C	370 cm^2/V s	24
3C-SiC/Si MOSFET (heteroepitaxial)	An *n*-type 5×10^{15} cm^{-3} doped epilayer on Si (001) substrate Al implants were used to realize a box profile with doping concentration of 5×10^{16} cm^{-3} to fabricate lateral *n*-channel MOSFET	Dry thermal oxidation at 1200°C for 60 min, 1300°C for 20 min, and 1400°C for 5 min, and Ar annealing at the respective temperatures for 30 min	70, 71, and 70 cm^2/V s	This work

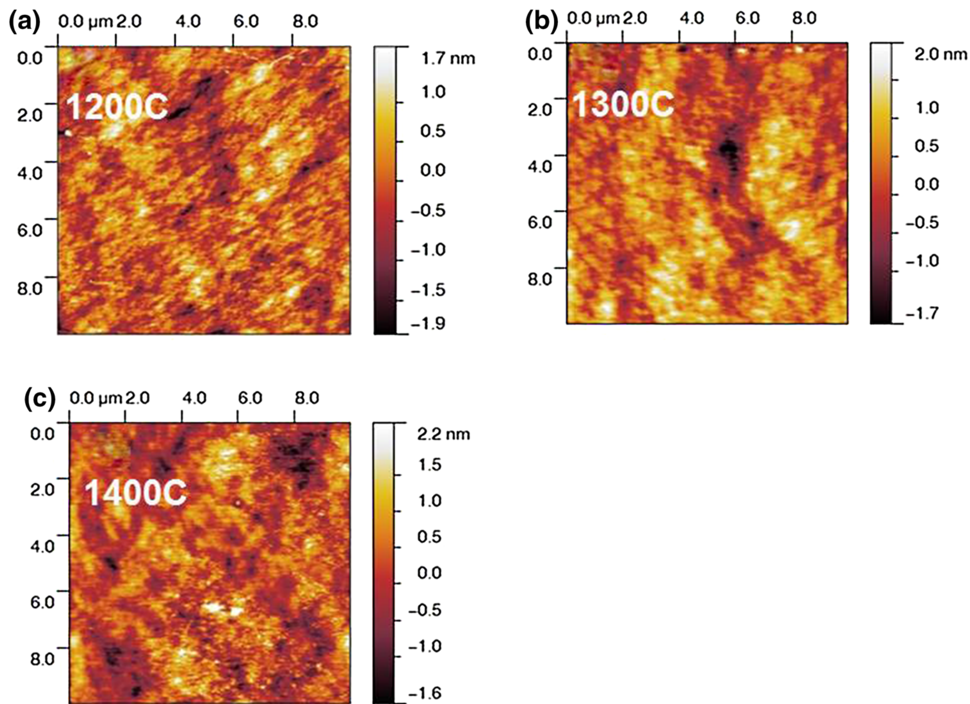

Fig. 3. Atomic force microscopy (AFM) results for MOS capacitors with thermal oxides grown at (a) $T = 1200°C$ (b) $T = 1300°C$, and (c) $T = 1400°C$. The RMS values of roughness are within the range 0.54–0.60 nm, implying high temperature does not degrade the surface morphology of the devices.

curve, indicating the presence of interface traps near the conduction band (CB) edge and/or the presence of oxide near interface traps (also known as "slow traps").[17] The C–V curves have small hysteresis (not shown), indicating precisely the slow nature of some of the traps.[17] In addition, increased net positive fixed charge at the interface causes less band bending, resulting in increased capacitance in the depletion region.[18] The density of interface traps (D_{it}) obtained by use of the Terman C–V and conductance methods (Fig. 1c inset) are compared in Fig. 1c.[19] Both methods give consistent results, with D_{it} values of approximately 1×10^{12} cm^{-2} eV^{-1} at $E_{\mathrm{C}} - E_{\mathrm{T}}$ = 0.25 eV. No extra benefit of using higher temperatures (1300 and 1400°C) is also confirmed by the G–V plot shown in Fig. 2a, obtained at

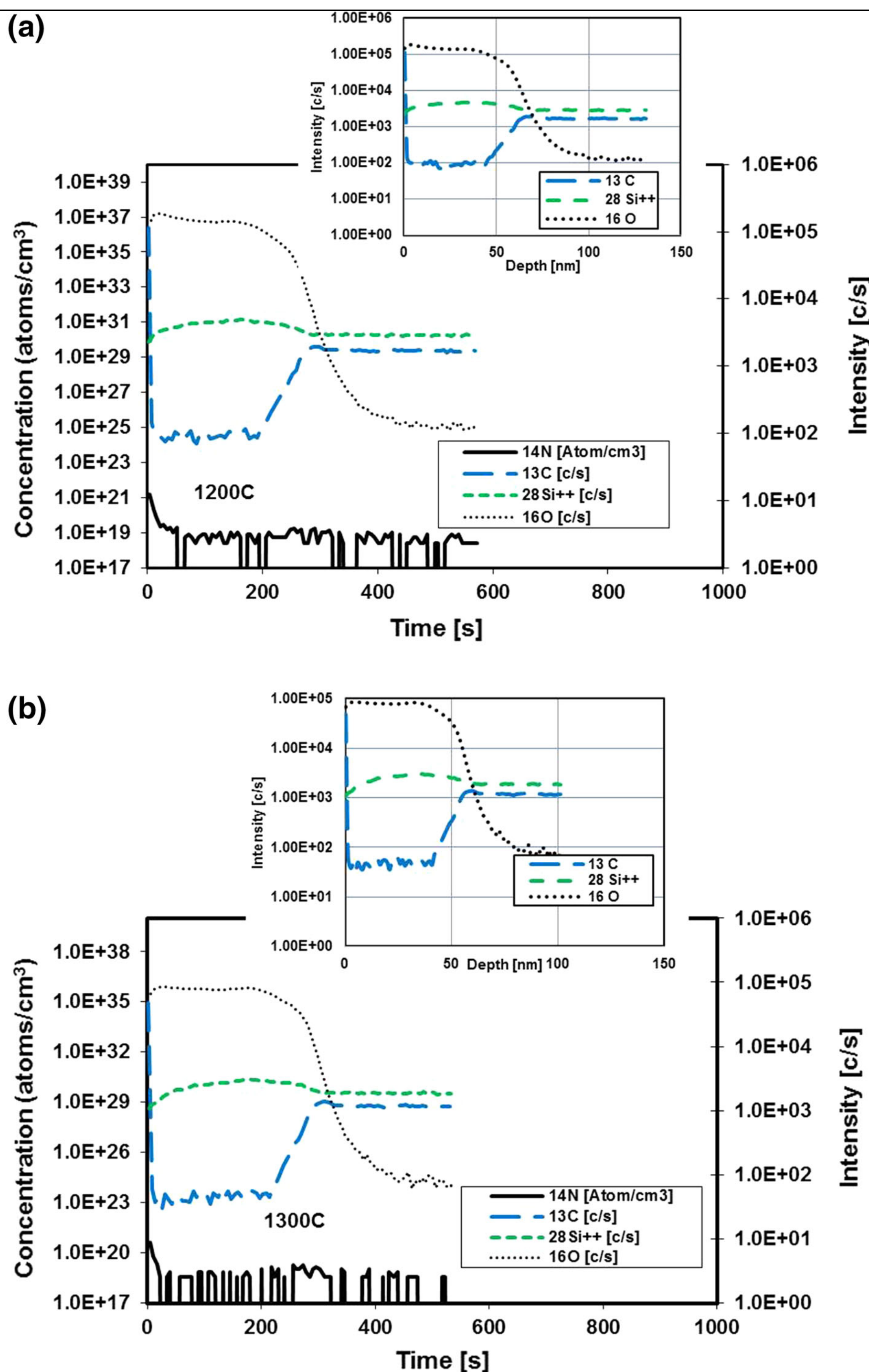

Fig. 4. SIMS profiles of MOS capacitors fabricated under different thermal oxidation conditions: (a) T = 1200°C (b) T = 1300°C, and (c) T = 1400°C. The 3C-SiC/SiO_2 interfaces are located at depths ~50 nm where the oxygen signals drop to half their peak values.

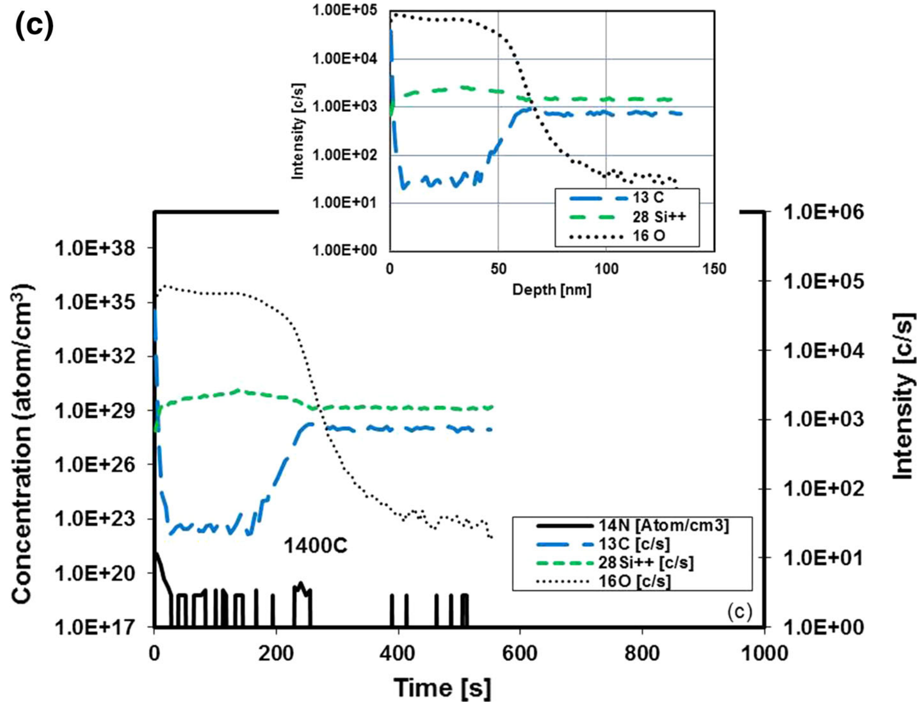

Fig. 4. continued.

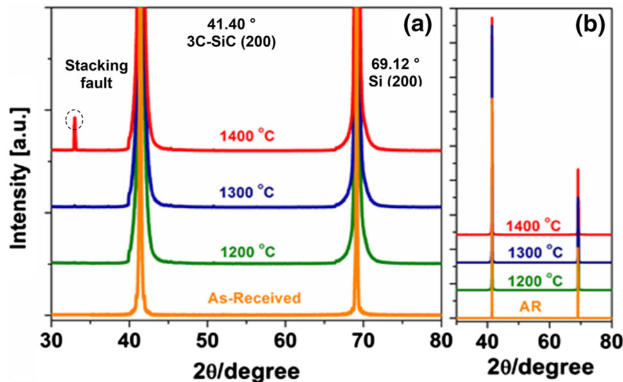

Fig. 5. XRD spectra of 3C-SiC/Si samples before and after dry oxidation: (a) a magnified view; (b) full view. The results show that even after 1400°C thermal oxidation the epilayer is cubic in nature.

100 kHz. The area under the conductance peak is a measure of D_{it}. The position of the peak corresponds to the energy position in the bandgap and, because all these peaks occur at a gate bias close to V_{FB}, it can be inferred that these peaks are a measure of D_{it} close to the CB edge of 3C-SiC. All these devices have almost same area under G–V curves. Also, all of the G–V curves have finite FWHM, suggesting that these traps are distributed over an energy range within the bandgap and are not localized at a fixed energy value. Similar results have been reported for nitrogen-implanted 3C-MOS-C.[20] Also, lateral MOSFET were fabricated by use of different oxidation temperatures. The results of mobility measurements for lateral MOSFET are shown in Fig. 2b. All the MOSFET have a peak field-effect channel mobility of approximately 70 cm^2/V s, implying little improvement of the electrical properties of the interface with increasing oxidation temperature, consistent with the D_{it} results obtained for the MOS-C. In Table I, values of measured field-effect mobility (μ) are compared with data previously reported for 3C-SiC MOSFET.[21–24]

Figure 3 shows results from atomic force microscopy performed for all the devices to determine the effect of temperature on surface morphology. The RMS values of roughness for all these MOS-C lie in the range of 0.54–0.60 nm, showing that high temperatures (≥1300°C) do not affect the surface morphology. Secondary ion mass spectrometry (SIMS) profiles are shown in Fig. 4. There is virtually no appreciable difference between the Si, O, and C profiles for all the devices, possibly because of the absence of out-diffusion or diffusion of species from the interface. Although it is possible the Si, O, and C concentrations decrease monotonically very slightly with temperature, the accuracy of SIMS measurement was insufficient to confirm this. X-ray diffraction (XRD) results are shown in Fig. 5. There is no shift in the 3C-SiC (200) peak before and after high-temperature oxidation, confirming that the cubic structure of the epilayer is intact.

Parallel equivalent conductance spectroscopy was used for further analysis of the effects of high-temperature oxidation. Figure 6 shows plots of G_P/ω as a function of probe frequency for all the MOS-C. By fitting the curves to a Gaussian fit, it possible to extract D_{it}, trap time constant (τ_p), and surface

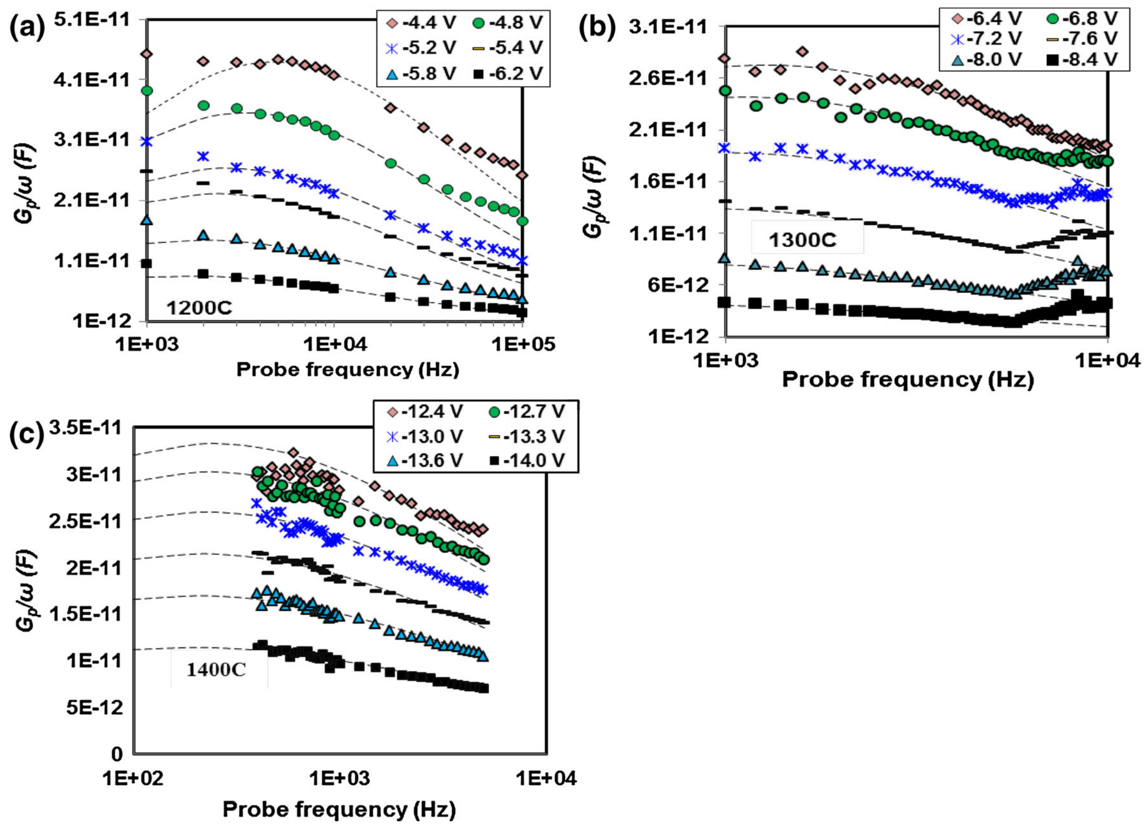

Fig. 6. G_p/ω as a function of probe frequency (ω) at different biases in the depletion region for MOS capacitors with as-grown thermal oxide at (a) T = 1200°C, (b) T = 1300°C (c) T = 1400°C.

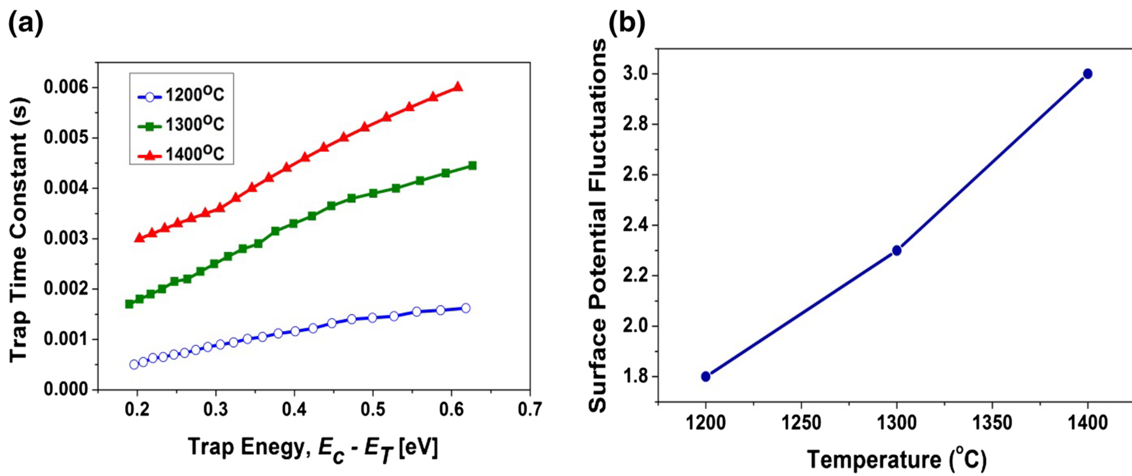

Fig. 7. (a) Trap time constant (τ_p) as a function of trap energy, and (b) the temperature dependence of standard deviation of the surface potential (σ_s) for 3C-SiC MOS-C.

potential fluctuations (σ_s) for the devices. D_{it} extracted by use of this technique for all the devices is shown as the inset of Fig. 1. Figure 7a shows the trap time constant as a function of $E_C - E_T$. Across the different energy levels in the forbidden energy band gap, τ_p increases with increasing temperature. Also, for a given temperature, τ_p increases as we go deeper into the energy band gap. Furthermore, from the curve fitting we are able to extract a value for the surface-potential fluctuation. Figure 7b shows the temperature dependence of the standard deviation of the surface potential (σ_s), which is caused by fluctuations of interface states, for the different devices. σ_s lies in between 2 and 3, which indicates

that the 3C-SiC/SiO_2 interface is electrically better than the 4H-polytype (σ_s = 4 for 4H and approx. 2 for Si). This fairly low value of σ_s, coupled with the low value of D_{it} for as-oxidized MOS devices, suggests that Coulombic interface-scattering-related effects should not limit transistor performance.

CONCLUSIONS

High-temperature oxidation (1200–1400°C) was used to grow 3C-SiC/SiO_2 interfaces. An in depth study of the interfaces was conducted by fabricating MOS-C and lateral MOSFET. Unlike the 4H-polytype of SiC, no extra advantage is gained by growing the 3C-SiC/SiO_2 interface at higher oxidation temperatures (> 1200°C). All the MOSFET with their gate oxides grown at these temperatures have a peak field-effect mobility of 70 cm^2/V s. Low values of σ_s indicate that the 3C-SiC/SiO_2 interface is electrically better than its 4H-SiC counterpart. These findings have important implications for SiC MOS technology because 3C-SiC/Si might be a low-cost alternative even if high-temperature processing is necessary.

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