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High-Performance MWIR HgCdTe on Si Substrate Focal Plane Array Development

R. BOMMENA,[1,4] S. KETHARANATHAN,[1] P.S. WIJEWARNASURIYA,[2] N.K. DHAR,[3] R. KODAMA,[1] J. ZHAO,[1] C. BUURMA,[1] J.D. BERGESON,[1] F. AQARIDEN,[1] and S. VELICU[1]

1.—EPIR Technologies, Inc., Bolingbrook, IL, USA. 2.—Army Research Laboratory (ARL), Adelphi, MD, USA. 3.—Night Vision and Electronic Sensor Directorate (NVESD), Fort Belvoir, VA, USA. 4.—e-mail: rbommena@epir.com

The development of low noise-equivalent differential temperature (NEDT), high-operability midwave infrared (MWIR) focal plane arrays (FPAs) fabricated from molecular beam epitaxial (MBE)-grown HgCdTe on Si-based substrates is reported. High-quality *n*-type MWIR HgCdTe layers with a cutoff wavelength of 4.90 μm at 77 K and a carrier concentration of 1–2 $\times$ 10^{15} cm^{-3} were grown on CdTe/Si substrates by MBE. Highly uniform composition and thickness over 3-inch areas were demonstrated, and low surface defect densities (voids ~5 $\times$ 10^2 cm^{-2}, micro-defects ~5 $\times$ 10^3 cm^{-2}) and etch pit density (~3.5 $\times$ 10^6 cm^{-2}) were measured. This material was used to fabricate 320 $\times$ 256, 30 μm pitch FPAs with planar device architecture; arsenic implantation was used to achieve *p*-type doping. Radiometric and noise characterization was also performed. A low NEDT of 13.8 m K at 85 K for a 1 ms integration time with f/#2 optics was measured. The NEDT operability was 99% at 120 K with a mean dark current noise of 8.14 $\times$ 10^{-13} A/pixel. High-quality thermal images were obtained from the FPA up to a temperature of 150 K.

Key words: MBE, HgCdTe, MWIR, silicon, CdTe, dark current, FPA, NEDT

INTRODUCTION

Mercury cadmium telluride (HgCdTe) focal plane arrays (FPA) have been developed for use at short-wave infrared (SWIR), midwave infrared (MWIR), and longwave infrared (LWIR) wavelengths in several military and civilian applications. Most of these high-performance arrays were manufactured on CdZnTe substrates which are expensive and often limited in size to up to 7 cm $\times$ 7 cm. However, interest in large-format and high-performance focal plane arrays (FPAs) has led to much effort to develop alternative substrates, for example those using silicon (Si), gallium arsenide (GaAs), and gallium antimonide (GaSb). Silicon-based substrates have long been regarded as the most promising, because they are relatively inexpensive, and have high mechanical strength and good thermal properties. Silicon also has the advantage of matched coefficients of thermal expansion (CTE) with the silicon-based read-out integrated circuits (ROICs) on which detector and substrate material are typically hybridized. In this paper we report the development of MWIR HgCdTe detectors on silicon based substrates, by use of conventional planar *p*/*n* technology.

EXPERIMENTAL

FPAs were fabricated from MBE MWIR HgCdTe grown on CdTe/Si substrates. The *p*-on-*n* device architecture was achieved by selective ion implantation of arsenic on the as grown *n*-type material.[1]

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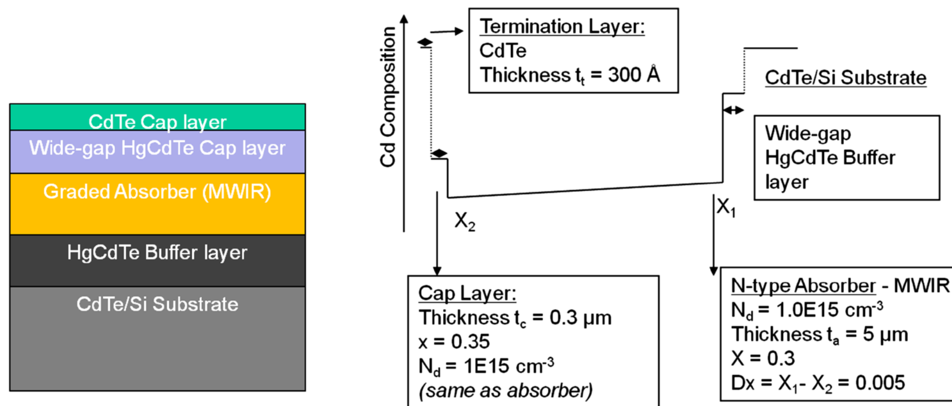

Fig. 1. Device structure for MWIR DLPH HgCdTe.

MBE Growth of CdTe/Si and MWIR Double-Layer Planar Heterostructure (DLPH) HgCdTe

Material growth was performed in two different chambers:

1. MBE growth of CdTe buffer layers on 3-inch silicon substrates in a V100 chamber followed by
2. MBE growth of a conventional MWIR HgCdTe DLPH structure on the previous substrates in a Riber 32P chamber.

The CdTe was grown by molecular beam epitaxy on nominal ⟨211⟩ oriented Si wafers. Wafers were initially cleaned by use of an RCA-type process. After high-temperature de-oxidation under As_4 flux, a thin ZnTe buffer layer was grown by migration-enhanced epitaxy from sources of elemental Zn and Te. A CdTe layer 10 micron thick was then grown by use of a CdTe compound source, with mid-growth annealing several times. The growth processes, which were similar to those reported elsewhere,[2–5] typically yield x-ray DCRC values of 60–70 arc seconds for the CdTe ⟨422⟩ reflection.

MWIR DLPH HgCdTe was grown on the CdTe/Si substrate in a Riber 32p MBE chamber. Before growth, the substrates were chemically cleaned and etched in bromine–methanol solution. After mounting the substrate on a molybdenum holder, the holder was loaded into the vacuum chamber for MBE growth. Once introduced into the growth chamber, each substrate was heated above 350°C. At this temperature, excessive Te and oxides present on the sample surface were removed and a fresh surface was prepared for subsequent HgCdTe growth. Both RHEED and in-situ SE techniques were used to monitor the surface preparation and growth processes. During the growth, compositional gradients were introduced between the absorption layer, the bottom buffer, and the top cap layer. In situ spectroscopic ellipsometry was used during growth to help monitor the growth process. Optical models were set up to fit the experimental data, to determine properties of interest such as surface roughness and optical constants (which are related to layer composition). The optical constants used in this model were acquired experimentally for high-quality single-crystalline HgCdTe wafers.

MWIR DLPH HgCdTe was grown in accordance with the device structure shown in Fig. 1. A widegap HgCdTe buffer layer was initially grown on the CdTe/Si substrate to mitigate the effect of strain from lattice mismatch. The heterostructure for absorption in the MWIR with a graded absorber (5 μm thick, $x = 0.3$ for $\lambda_c = 5$ μm, $N_d = 1 \times 10^{15}$ cm^{-3}) followed by a wide-gap cap layer (0.3 μm thick, $x = 0.35$ and $N_d = 1 \times 10^{15}$ cm^{-3}) was then grown. The growth structure was terminated with a thin CdTe cap layer to protect the HgCdTe surface.

Fabrication of MWIR HgCdTe Focal Plane Arrays (FPA)

Focal plane arrays in the 320 × 256, 30 μm pitch format were fabricated with the p on n planar device architecture by use of a combination of photolithography, ion implantation of arsenic, annealing for activation, passivation, metal deposition for ohmic contacts, and indium bumps. Device fabrication was performed on 12 mm × 20 mm samples which were cut from MBE-grown 3-inch wafers. Photolithography was performed by using a contact mask aligner to define windows for ion implantation of arsenic. Activation[6] of arsenic for p-type doping of HgCdTe was achieved by two-step annealing. Annealing at 435°C for 10 min was followed by annealing at 250°C for 24 h in a sealed quartz ampule. The implanted samples were passivated by MBE-deposited CdTe after which ohmic contacts with the p and n regions were prepared by e-beam deposition of gold (Au). Indium bumps were deposited by e-beam evaporation as the final step in the fabrication of the detector arrays. MWIR HgCdTe detector arrays fabricated by use of this sequence were hybridized to FLIR 9705 ROICs, mounted on 84-pin LCCs, and wire bonded to characterize the FPAs.

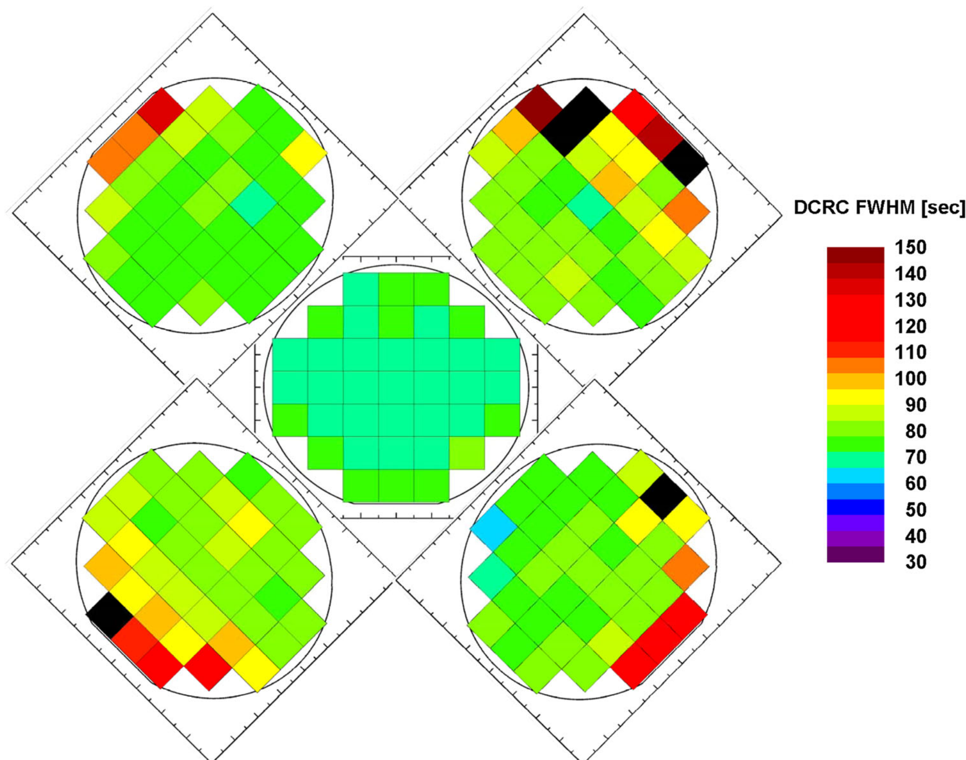

Fig. 2. DCRC FWHM mapping of 5 CdTe/Si wafers grown in a single MBE run in a V100 chamber.

Characterization of FPAs

Imaging and radiometric characterization of FPAs was performed by use of an SE-IR CamIra test station comprising a custom-built integrated Dewar cooler assembly (IDCA) configured for handling ISC9705/9809 ROICs and a camera head to interface with the IDCA. The camera head comprised 4 different 14-bit ADC cards (one for each output channel of the ISC9705/9809), pulse synthesizers for frame sync (FSYNC), line sync (LSYNC), and clock, DC bias generation and control, and analog amplifiers for amplifying the data from the ROIC. After mounting the FPA in the IDCA, its outputs were electrically monitored by checking the signal swing and biases by use of an oscilloscope. Electrical and optical characterization of the FPAs was performed in a temperature-controlled cryostatic Dewar with a blackbody for photon flux calibration. Dark current was measured for each pixel and captured in the temperature range from 80 K to 165 K. The map of NEDT per pixel and related histograms were extracted in the same temperature range and FPA operability was determined with the criteria that to be operable a pixel's value must be less than twice the mean value. Thermal imaging was performed at different temperatures by use of an MWIR lens in a laboratory environment.

RESULTS AND DISCUSSION

MBE growth of CdTe/Si substrates yielded high-quality buffer layers, as indicated by the low FWHM value (< 80 arc sec) from a DCRC measurement on 3-inch silicon substrates. A typical growth run in the V100 MBE chamber included 5 wafers of 3-inch silicon substrates; the CdTe buffer layers grown on these were highly uniform, as was apparent from the quality as measured by DCRC mapping of the samples from one of the growth runs (Fig. 2).

Excellent control of the MBE growth structure of the MWIR HgCdTe DLPH was demonstrated by the uniformity in the FTIR maps of composition and thickness on a typical MWIR HgCdTe/CdTe/Si layer (Fig. 3). The λ_c variations over a 3″ wafer are less than 2% and layer thickness variations were approximately 7.5%. Our FPA sizes (9.6 mm x7.7 mm) are smaller than the wafer, so good uniformity of FPA properties was expected.

The HgCdTe layers were high-quality, as indicated by electrical and structural characterization of the material. The as-grown n-type layers had a carrier concentration of 1–2 $\times$ 10^{15} cm^{-3} and a Hall mobility of 1.2 $\times$ 10^{4} cm^{-2} V s. After Hg vacancy fill annealing, a higher mobility of 3.4 $\times$ 10^{4} cm^{-2} V s was achieved. Low surface defect densities (voids $\sim$5 $\times$ 10^{2} cm^{-2}, micro-defects $\sim$5 $\times$ 10^{3} cm^{-2}) and etch pit densities ($\sim$3.5 $\times$ 10^{6} cm^{-2}) were measured on the MWIR HgCdTe epilayers on CdTe/Si substrates. The fabrication process flow for the p on n photodetector arrays was monitored by use of a Nomarski microscope; good quality control was achieved during lithography, etching, passivation, metal deposition, and indium bump formation processes, as shown in Fig. 4.

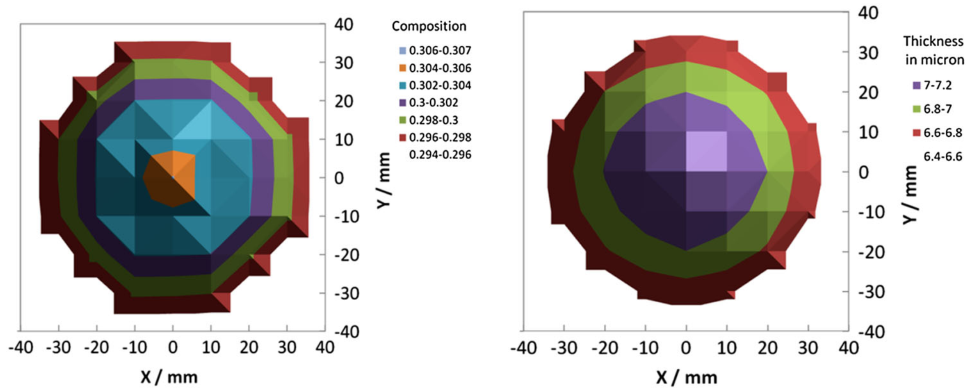

Fig. 3. FTIR Map of cadmium composition and layer thickness on MBE-grown MWIR HgCdTe/CdTe/Si.

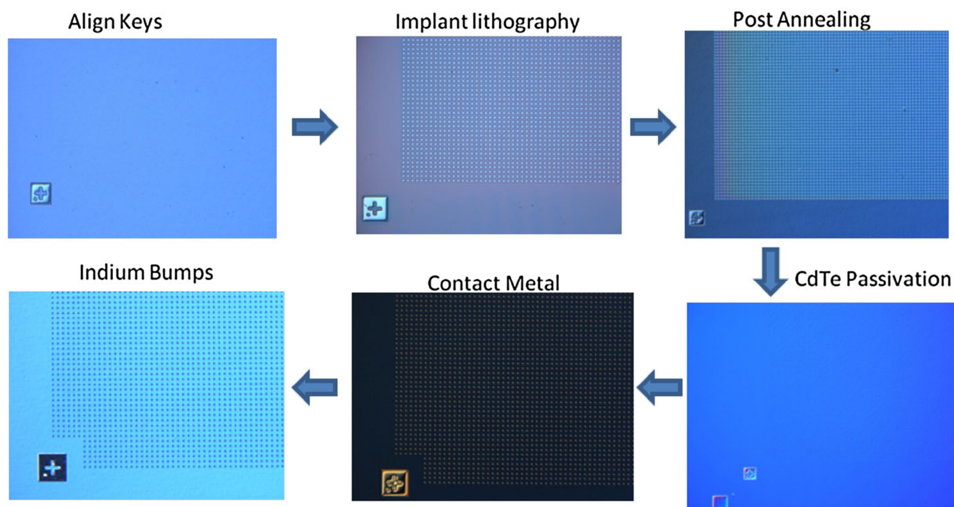

Fig. 4. Nomarski images of MWIR HgCdTe/CdTe/Si 320 $\times$ 256, 30 μm pitch detector arrays during fabrication steps.

Fig. 5. Thermal images taken by use of a 320 $\times$ 256, 30 μm pitch MWIR HgCdTe/CdTe/Si FPA operating at 85 K (frame rate 60 Hz, integration time 1 ms).

Thermal imaging with the hybridized MWIR HgCdTe/CdTe/Si FPA revealed high contrast (Fig. 5) at an initial temperature of 85 K when the detector was biased at a low reverse bias of 42 mV, with a frame rate of 60 Hz and an integration time of 1 ms.

The pixel map under dark conditions revealed high response uniformity (Fig. 6a) across the array, with dark current operability of 99.0% at 85 K from the MWIR HgCdTe/CdTe/Si FPA. The dark current histogram showed a good fit for a mixed 3-term normal

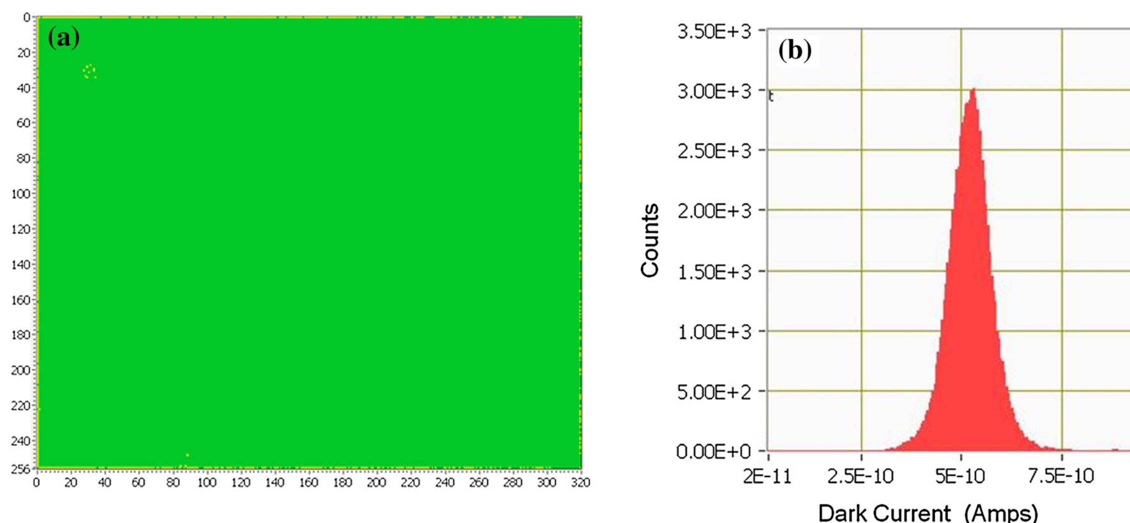

Fig. 6. (a): Dark current pixel map from MWIR HgCdTe/CdTe/Si, 320 × 256, 30 μm pitch FPA (b) Histogram for dark current operability at 85 K for the same FPA.

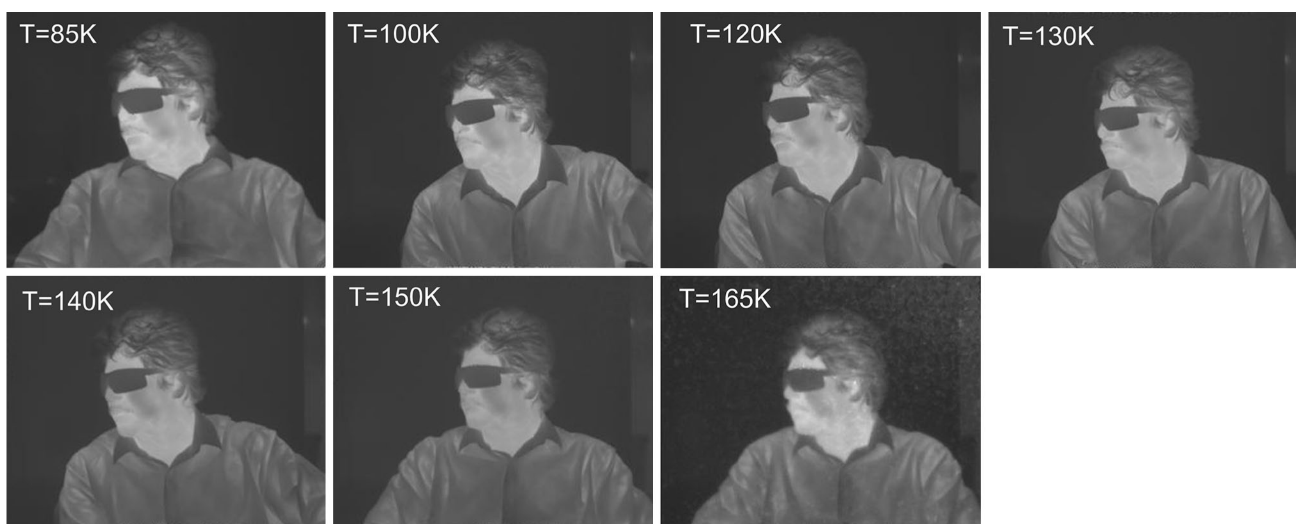

Fig. 7. Thermal imaging at different temperatures captured by MWIR FPA fabricated from MBE grown HgCdTe on CdTe/Si substrate. Non-uniformity corrections were applied.

Gaussian with a positive skewness term of 7.16, indicating a longer tail to the right. The mean dark current value was 5.3×10^{-10} amps/pixel (Fig. 6b) with a standard deviation of 1.1×10^{-10} amps/pixel. Another FPA from the same batch of devices had a mean dark current density of 6.0×10^{-10} amps/pixel at 180 K. According to the "Rule-07",[7] the dark current limit at T = 180 K is 1.5×10^{-10} amps/pixel. With our current system limitations, background photons dominated measured current when the devices were cooled below 150 K, making the dark current unmeasurable. The average quantum efficiency for this FPA in its spectral range is 54% without an AR coating.

High-quality imaging was achieved from the MWIR HgCdTe/CdTe/Si FPA up to a temperature of 165 K (Fig. 7) and saturation of the pixels at elevated temperature beyond 165 K made imaging difficult, because of increased noise.

NEDT measurements were performed by capturing 100 frames at three different black body temperatures of 25, 30, and 35°C. A 50% well fill at 300 K background and an integration time of 1 ms was used. Low NEDT (13.8 mK @ 85 K to 18.5 mK @130 K) with a high operability (99.2% @ 85 K to 98.3% @ 130 K) as shown from the pixel maps and histograms in Fig. 8, was achieved from the FPAs characterized. This is a promising result that could

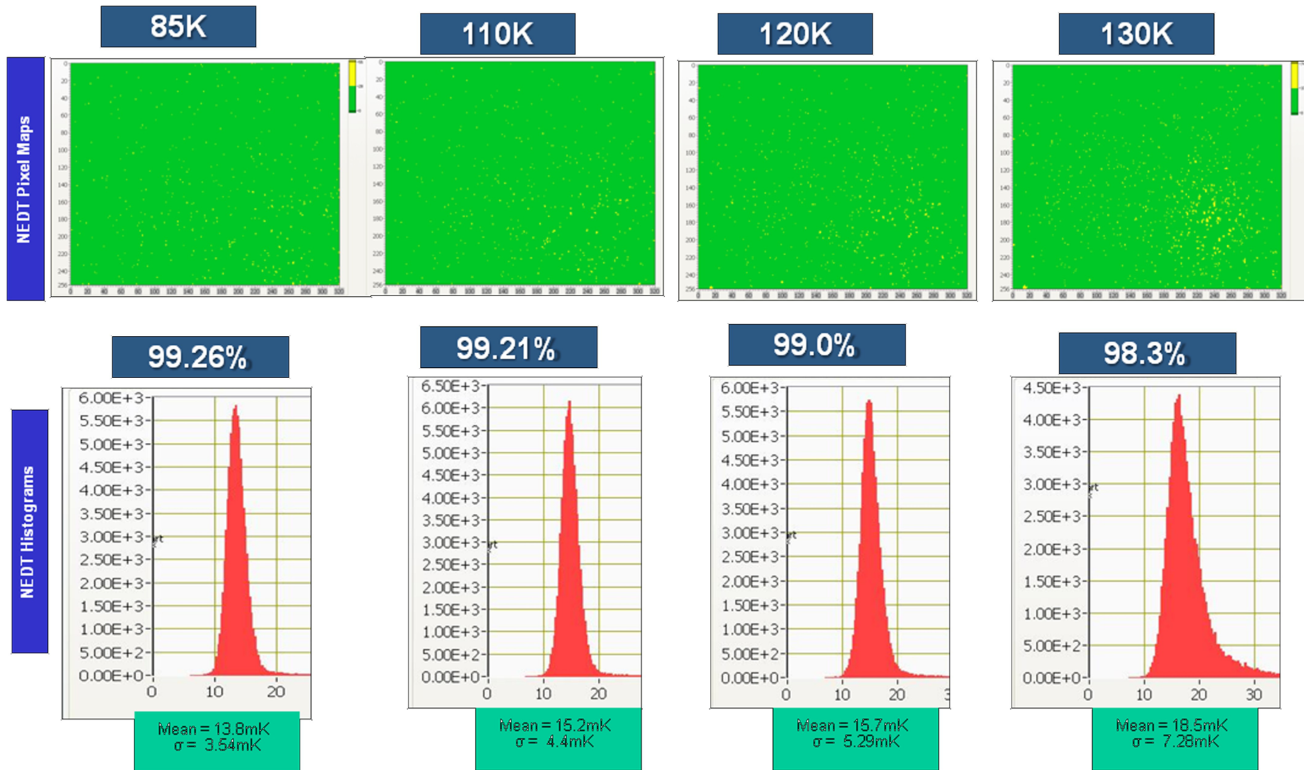

Fig. 8. NEDT pixel maps and histograms at different temperatures measured from a MWIR HgCdTe/CdTe/Si, 320 $\times$ 256, 30 μm pitch FPA.

enable the development of high-operating-temperature large-format FPAs on silicon substrates.

CONCLUSIONS

We report results obtained in the development of 320 $\times$ 256, 30 μm pitch MWIR HgCdTe FPA fabricated from arsenic-implanted *n*-type MBE-grown HgCdTe/CdTe/Si substrates. MBE-grown material on 3-inch substrates was of high composition and thickness uniformity, and qualitative characteristics revealed low surface defect and etch pit densities. Radiometric characterization of FPAs revealed high operability, low NEDT, and high resolution imaging up to 150 K. Future work will focus on increasing the operating temperature and developing larger-format FPAs.

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