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An Investigation into the Package and Printed Circuit Board Assembly Solutions of an Ultrathin Coreless Flip-Chip Substrate

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Flip-chip technology has been widely accepted as a solution for electronic packaging of high-pin-count devices. Due to the demand for smaller and thinner package dimensions, coreless build-up substrates will be used in industry to carry the die by solder bumps due to the advantages of shorter transmission route and lower inductance and thermal resistance. However, coefficient of thermal expansion (CTE) mismatch between the Cu trace and the laminate often causes the coreless substrate to warp, which leads to failures such as nonwetted solder bumps and interfacial cracking during assembly and reliability tests. In a previous study, assembly of a six-layer polyimide-based coreless flip-chip package was achieved by a 17 mm × 17 mm die with 4355 Sn-37Pb solder bumps, an amide-based underfill, and 1521 Sn-3.0Ag-0.5Cu solder balls. For determination of its board-level reliability characteristics, the component was mounted on a printed circuit board (PCB) using a conventional surface mount technology, and 10 test vehicles were assembled for assessment of their reliability under a temperature cycling environment. The experimental results show that the characteristic life of the PCB assembly exceeded 1500 cycles and that failure resulted from fracture of the outermost solder balls on the substrate side. This was different from the failure mode of die cracking when the package experienced hundreds of temperature cycles at the component level because the rigid PCB, through solder balls, moderated the deformation of the coreless flip-chip package. Hence, the concentrated bending stress at the die edge region was lowered. Finally, the local CTE mismatch between the stiffener and the PCB dominated the fatigue fracture of the outermost solder balls to become the main failure mode.

Key words: Flip-chip package, coefficient of thermal expansion, coreless substrate, failure mode

INTRODUCTION

In recent decades, increasing numbers of integrated circuit (IC) devices have used flip-chip technology due to the requirements of high pin counts, ultrafine pitch, lower inductance, and high operation frequency. To reduce the signal loss caused by the higher dielectric constant and dielectric loss induced by glass fibers in the laminates of the substrate, coreless substrate laminated by polyimide (PI) or Ajinomoto build-up film (ABF) has been used to replace the flame retardant 5 (FR5) and bismaleimide triazine (BT) materials in the flip-chip package process,[1,2] and Toppan has reported that such coreless substrate has better high-speed transmission performance than the conventional build-up type of substrate at frequency above 20 GHz (www.toppan.co.jp). However, elimination of the glass fiber reinforcement from the

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laminated core layer causes severe warpage issues during the build-up and assembly processes, significantly deteriorating package yield.

Turning to the reduction of hazardous substances, the popular bromide flame retardant (BFR) tetrabromobisphenol A (PBBPA) is still used in printed circuit boards (PCBs). BFRs and polyvinylchloride (PVC) need to be phased out in the near future because incinerating them releases dioxin and furan. In contrast, PI-based coreless substrate, which needs no added flame retardant because of its excellent thermal stability and good mechanical and chemical properties, could be an ideal solution for halogen-free IC substrate development.

Although the mechanical and electrical performance of standard and coreless substrates have been investigated in previous studies,[3,4] a way to assemble a large die on a coreless substrate is still needed.[5] In our previous study,[6] a silicon chip with dimensions of 17 mm × 17 mm and eutectic Sn-37Pb solder bumps was connected to a six-layer PI build-up coreless substrate by a reflow process in N_2 and sealed by two different underfill materials. Then, Sn-3.0Ag-0.5Cu Pb-free solder balls were mounted on the substrate, after which four reliability tests, namely a temperature cycle test (TCT), thermal shock test (TST), high-temperature storage test (HTST), and thermal humidity storage test (THST), were performed on the package. The results are summarized in Table I. Failure induced by die cracking was discovered in the package sealed by amide-based underfill at around 500 cycles of TCT or TST testing. This failure was attributed to the higher bending modulus of the underfill, which, due to its brittleness, could not adapt to warping induced by the CTE mismatch between the die and substrate. However, the board-level reliability of the coreless flip-chip package is rarely studied.

To clarify the board-level reliability of the coreless flip-chip package, test vehicles were assembled using the same parameters and sealed with the amide-based underfill (with inferior component-level reliability). Afterward, the coreless flip-chip package was mounted on a printed circuit board with an electroless Ni/immersion Au (ENIG) finish layer using surface mount technology (SMT), and then test vehicles assembled with the same conditions were subjected to temperature cycling tests under condition B of the JESD22-A104-B standard[7] until failure occurred so that possible improvement of the board-level reliability of the coreless flip-chip package (CFCP) could be assessed. The failed samples were then cross-sectioned, observed by scanning electron microscopy (SEM), and analyzed by energy-dispersive spectrometry (EDS).

EXPERIMENTAL PROCEDURES

Figure 1 presents the structure of the coreless flip-chip package used in this study. The dimensions of the silicon die (Taiwan Semiconductor Manufacturing Company) were 17 mm × 17 mm × 0.7 mm, and it was connected to a 220-μm-thick coreless substrate by 4355 solder bumps (Chipbond Technology, Taiwan) with composition Sn-37Pb and height 0.1 mm on an under bump metallization (UBM) layer of 5 μm Cu/3 μm Ni. The substrate pad was a solder mask defined with opening sizes of 0.1 mm (flip-chip bump pad) and 0.4 mm (solder ball pad). The surface finish of the substrate pad was electroless Ni/immersion Au (ENIG), and a Sn-37Pb presolder layer was stencil-printed on the flip-chip bond pad, reflowed, and leveled on it. The solder joints were formed by mounting Sn-3.0Ag-0.5Cu solder balls onto the ball grid array (BGA) pads using water-soluble flux. The six-layer polyimide (PI) laminated coreless substrate (Toppan Printing, Tokyo, Japan) after chip connection is shown in Fig. 2. The specifications of the coreless substrate are summarized in Table II, and a numerical analysis model was established accordingly.

The soldering process was conducted in a reflow oven (Hotflow 7; ERSA, London, UK) with seven zones, in which the preheating (120°C to 160°C) time was 143 s, the peak temperature was 227.9°C, and the time above liquidus was 103 s. After the reflow process, the assemblies were cooled to room temperature and the flux residues were removed using an organic solvent. An x-ray system (VXP-160.15; COMET, Garbsen, Germany) with maximum voltage of 160 kV was utilized to observe the solder joint interconnections. Afterward, the gap between the die and substrate was filled with an

Table I. Package-level reliability test results of six-layer coreless flip-chip package[3]

Item	Condition	Fail/Total
TCT	−55°C to 125°C, 1000 cycles, condition B	1/15 (530 cycles) 2/15 (600 cycles) 3/15 (643 cycles) 5/15 (800 cycles)
TST	−55°C to 125°C, 1000 cycles, condition C	1/15 (500 cycles) 5/15 (750 cycles)
HTST	150°C for 1000 h, condition B	Pass
THST	85°C/85% RH for 1000 h	Pass

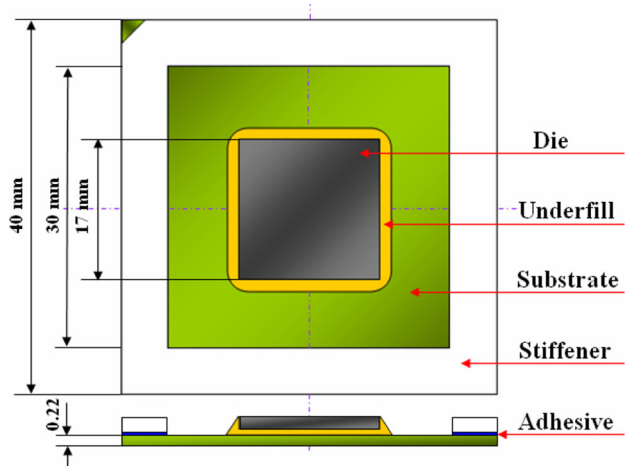

Fig. 1. Structure of coreless flip-chip package used in this study.

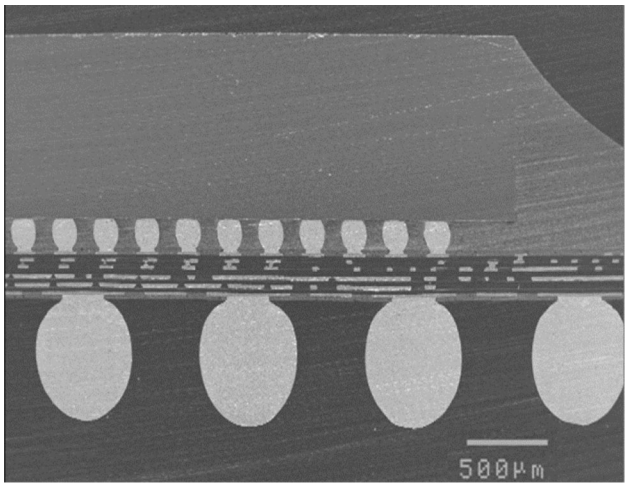

Fig. 2. Cross-sectional view of coreless flip-chip package used in this study.

amide-based underfill using a dispenser (Asymtek DS-9000; Nordson, OH, USA) at 120°C, and then postcured at 150°C for 1 h. Next, Sn-3.0Ag-0.5Cu solder paste was transferred onto a printed circuit board (PCB, 20.5 cm × 9.5 cm × 1.2 mm) using a 120-μm-thick stencil. Then, the coreless flip-chip device was reflowed. The diameter and standoff of the solder joints after surface mounting were 0.64 mm and 0.45 mm, respectively. A total of 10 test vehicles underwent temperature cycling tests from −55°C to 125°C according to the JEDEC standard (JESD22-A104-B, condition B).[7] The experiment stopped when all the test vehicles failed, and a Weibull diagram was prepared to analyze the characteristic life of the coreless flip-chip package on the PCB.

Afterward, the failed samples were mounted with epoxy and then ground and polished with SiC papers and Al_2O_3 pastes, respectively. The cross-sectional microstructures of the solder joints were observed with a scanning electron microscope (SEM, JSM-6100; JEOL, Tokyo, Japan), and the chemical compositions of the intermetallic phases were determined by energy-dispersive spectrometer (EDS).

ANSYS software was used to study the package-level and board-level stress/strain behaviors of the coreless flip-chip package (CFCP) under temperature cycling. The thermomechanical properties of the key components are summarized in Table III[8–10] and Table IV.[10] Additionally, the creep strain constitutive models of Wiese et al.[9,10] were introduced for both solder materials, based on well-described tests on real solder joints and not only bulk material. The models attributed the steady-state creep deformation to climb-controlled (low stress) and combined glide/climb (high stress) behavior, and the steady-state creep behavior was represented using a double power-law model. This equation can decrease analytical errors when little deformation occurs or strain rates are high.

Table II. Specifications of coreless substrate used in this study

	Material	Polyimide/Adhesive
Substrate	Thickness	220 ± 20 μm
	Metal layers	6
Package	Type	FCBGA
	Size	40 mm × 40 mm
	Ball count	1520
Flip-chip bond pad (solder mask defined)	Pad diameter	150 ± 5 μm
	Solder mask opening	100 ± 10 μm
	Bond pad pitch	250 ± 3 μm
BGA pad	Pad diameter	0.6 ± 0.05 μm
	Solder mask opening	0.4 ± 0.05 μm
	Bond pad pitch	1.0 mm
Other	Thickness of solder mask	20 ± 5 μm
	Thickness of presolder	15 ± 10 μm
Stiffener	Thickness	700 μm
	Adhesive	100 μm
	Width	5 μm

Table III. Elastic properties of materials[8–10]

Material	Young's Modulus (MPa)	Poisson Ratio	CTE (ppm/°C)
PCB	22,000	0.28	18
Substrate	3000	0.3	29
Underfill 1	8500	0.28	32
Underfill 2	12,000	0.28	26
Si die	131,000	0.23	2.3
Bump	75,842 – 151.7T (K)	0.4	26
Solder ball	59,533 – 66.667T (K)	0.38	20
Stiffener	200,000	0.29	10.8
Adhesive	1500	0.35	60

Table IV. Stress and strain response of solder alloys[10]

T (K)	ε_1	ε_2	σ_1 (MPa)	σ_2 (MPa)	σ_3 (MPa)
Sn-Pb					
278	7×10^{-4}	3×10^{-3}	21	41	600
323	7×10^{-4}	3×10^{-3}	19	31	400
Sn-Ag-Cu					
278	1.4×10^{-3}	4×10^{-3}	57.4	80	2500
323	1.4×10^{-3}	4×10^{-3}	53.2	72	1900

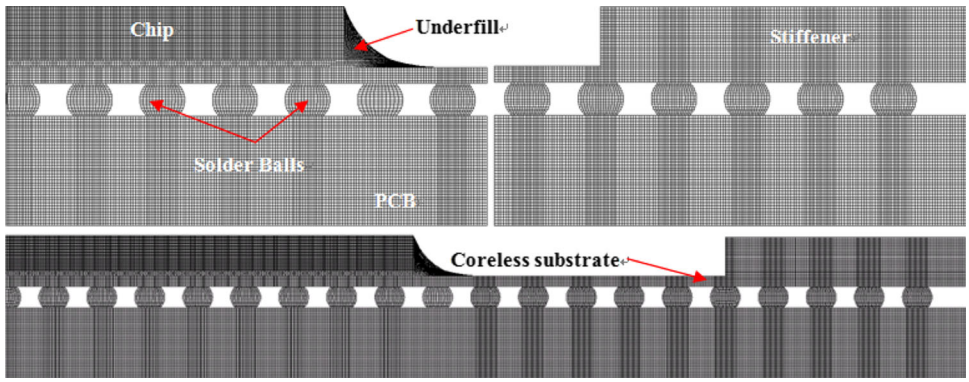

Fig. 3. Finite-element model mesh of coreless flip-chip package.

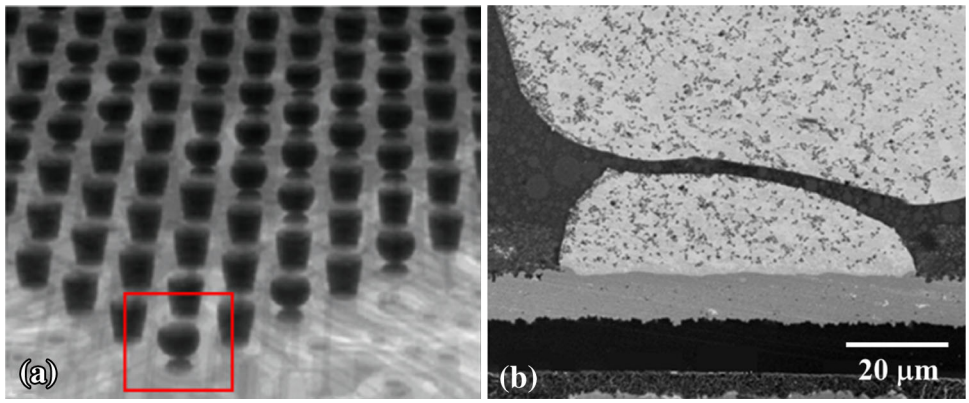

Fig. 4. (a) X-ray and (b) cross-sectional (SEM) images of cold solder joints induced by warping of coreless substrate.

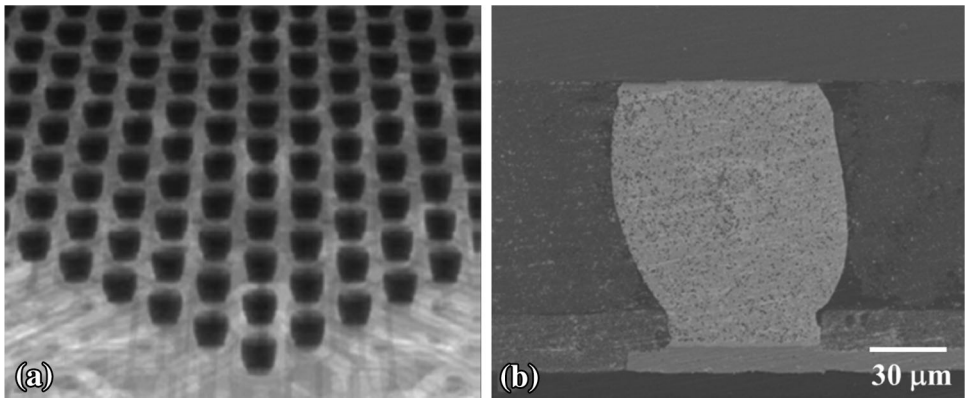

Fig. 5. (a) X-ray and (b) cross-sectional (SEM) images of perfect solder joints after tuning of reflow profile.

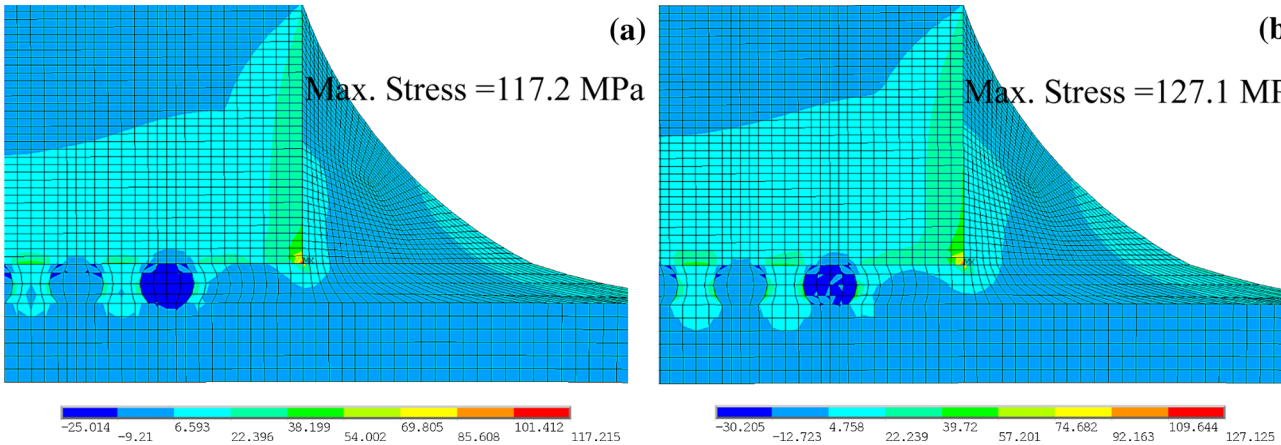

Fig. 6. Bending stress contour plot of component-level test for (a) phenol-based (left) and (b) amide-based (right) underfills.

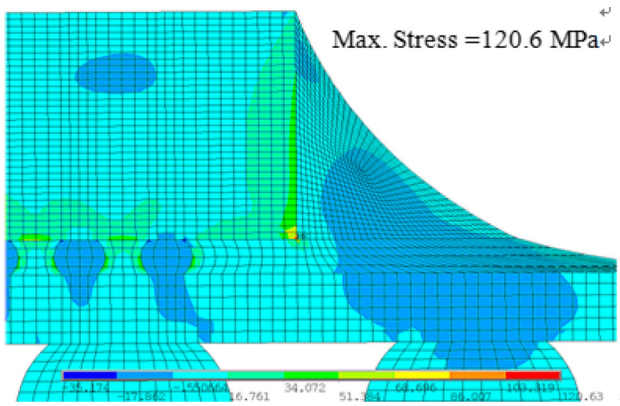

Fig. 7. Bending stress contour plot of board-level test for amide-based underfill.

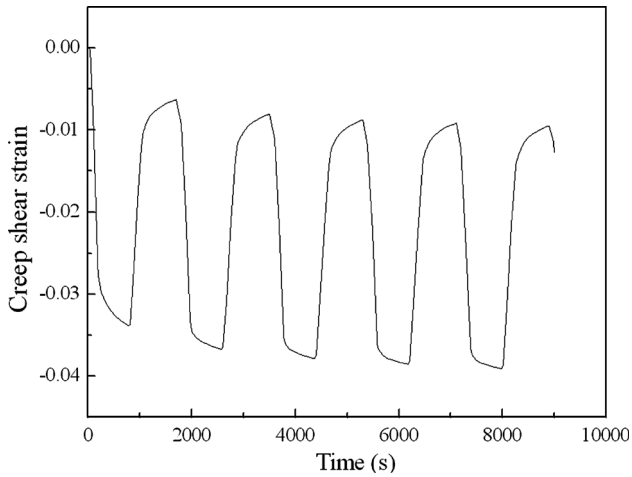

Fig. 8. Creep shear strain for Sn-3.0Ag-0.5Cu corner.

Sn-Pb[8]:

$$\dot{\varepsilon} = 0.4 \cdot \sigma^2 \cdot \exp\left(-\frac{5400}{T}\right) + 21 \cdot \sigma^7 \cdot \exp\left(-\frac{9500}{T}\right),$$

Sn-Ag-Cu[9]:

$$\dot{\varepsilon} = 4 \times 10^{-7} \cdot \sigma^3 \cdot \exp\left(-\frac{3223}{T}\right) + 1 \times 10^{-12} \cdot \sigma^{12} \cdot \exp\left(-\frac{7348}{T}\right),$$

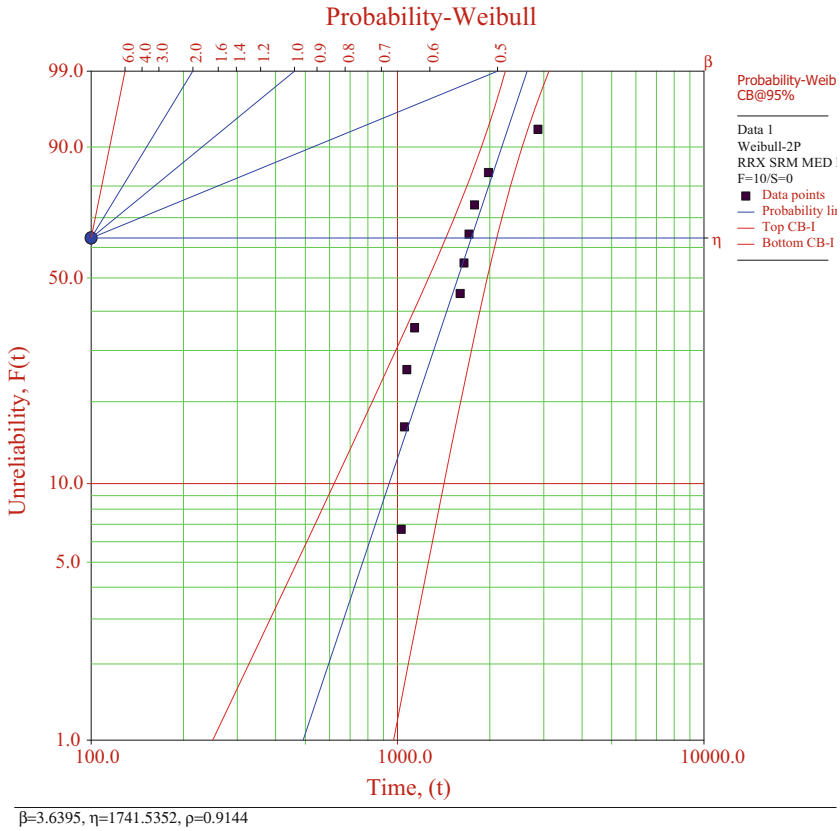

Fig. 9. Weibull distribution of CFCP/PCB after TCT.

with T in K and σ in MPa.

To simplify the analysis, only a two-dimensional (2D) model was established because the pin counts exceeded the capabilities of the available computers. Figure 3 shows the half-symmetry meshing model, which contained 43,889 plane solid elements and 134,223 degrees of freedom (using the PLANE183 element). The transient finite-element analysis for the CFCP assembly was assumed to be under the 2D plane strain condition and five cycles.

RESULTS AND DISCUSSION

According to the results of the previous investigation,[6] the CFCP assemblies have to overcome the defects of cold solder joints in the reflow process resulting from warpage of the coreless substrate, as the x-ray image shows in Fig. 4, because the coreless substrate easily varies from a concave shape to a convex one and vice versa on heating or cooling, with a variation of 25% to 50% higher than the thin core substrate at the peak temperature in the reflow process due to the CTE mismatch between upper and lower layers.[11] Furthermore, the chip attachment on a coreless substrate is more greatly deteriorated because the warpage varies depending on the thermal condition, and a cover jig can reduce warpage by more than 30% during heating.[11] However, mechanical support was not considered here because of throughput concerns. Because the CTE value of polyimide (29.2 ppm/°C, measured value) is higher than that of Cu, and the stiffener acts as a heat sink, it was assumed that the coreless substrate would show a convex shape when reflowed at 240°C because the PI layer at the bottom side would be heated and expand, and then it would convert to a concave shape during the cooling process due to the higher heat storage in the stiffener. The cold solder joint issue shown in Fig. 4 was always found when the cooling rate was below 2°C/s because the surface PI layer shrank more rapidly than the Cu, and the substrate adopted a concave shape before the solder joints at the corners solidified. To enhance the thermal dissipation of the stiffener and keep the substrate flat, a higher cooling rate of 5°C/s was adopted to make the solder bumps solidify before the coreless substrate could change from concave to convex. The defects of cold solder joints were significantly improved, and the eutectic Sn-37Pb solder bumps formed interconnections with the coreless substrate well, as can be seen in Fig. 5. Since a considerable amount of thermal stress was generated by the rapid cooling rate, it was decreased to 3°C/s or less as the temperature passed through the melting point of Sn-37Pb.

In the package-level reliability tests, the CFCP passed a high-temperature storage test at 150°C for 1000 h and a humidity/temperature storage test

under conditions of 85°C/85% RH for 1000 h. However, failure occurred in the temperature cycling test (TCT) and the thermal shock test (TST) at 530 and 500 cycles, respectively.[6]

The root cause of the failure mode was chipping defects formed at the edge of the die, and the CFCP vehicle was continuously bent during the temperature transition. The thermal stress concentrated at the defects could not easily be released by underfill material because of its high brittleness; hence, fracture was induced, and the crack initiated from the defects that had formed. According to the finite-element (FE) simulation results for phenol-based (underfill 1, 8.5 GPa) and amide-based (underfill 2, 12 GPa) underfills, the stiffer underfill was sensitive to bending stress, namely the first principal stress, as indicated in Fig. 6. This sensitivity did not result in permanent cracks instantly at the beginning, but it may have caused residual stresses to increase during repeated thermal cycling, thus constituting a reliability risk. In this case, the die cracking depended on a combination of the factors listed below. The first one was the bending stress near the die edge, which resulted from resistance to deformation of the coreless substrate by the stiffness of the die and underfill. The second was brittle fracture of the underfill at the upper edge, which resulted from the material mismatch. We note that the FE simulation predicted that failure should initiate in the bottom corner of the die because the simulation assumed ideal conditions, wherein the chipping defect and underfill fracture did not exist. In terms of the chip, the outermost corners bore the brunt of the stress assault as the substrate warped.

To identify the actual thermomechanical stress/strain behaviors of the CFCP on PCB, a simulation model of the CFCP with the amide-based underfill was established in this work (Fig. 7). It was found that the bending stress at the die edge decreased from 127.1 MPa to 120.6 MPa (a reduction of 5.1%) because the PCB restrained the warpage of the coreless flip-chip package and affected the distribution of bending stress. Figure 8 shows the creep shear strain contour of the solder joint between the CFCP and PCB, in which the maximum creep shear strain accumulated near the upper corner of the solder joint. It could be that local thermal expansion mismatch between the stiffener, substrate, and PCB, in combination with the relatively high stiffness of the stiffener and the high flexibility of the plastic laminate substrates, generated the complex interaction. As the rigid PCB, through the solder balls, attempted to obstruct the CFCP warpage, the change in stress conditions could have degraded the quality of the solder joint.

As Hossain et al.[12] reported, higher dynamic warpage can lead to electrical open and solder bridge defects in the SMT assembly process. In this study, we never found the mentioned defects after SMT because of the ideal design of the experiments.

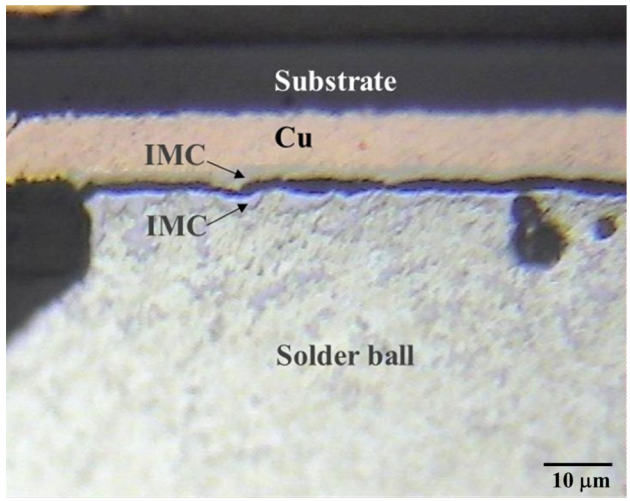

Fig. 10. Cross-sectional image of failed solder joint; IMC, intermetallic compound.

The coreless flip-chip packages were all well connected to the test board after the reflow process.

Figure 9 shows the Weibull analysis results of the CFCP assembled on board. Based on the statistical data, the characteristic life (η) of the printed circuit board assembly (PCBA) was around 1742 cycles, and the shape parameter (β) was 3.64. The mean time to failure (MTTF, or mean life) was determined to be 1570 cycles by $[\eta\Gamma(1 + 1/\beta)]$ for the CFCP on board. The failure percentage corresponding to the mean life of the CFCP on board was determined by $[1 - \exp(-(x/\eta)^{\beta})]$ to be 49.5%. No failures occurred before 1000 cycles for the board-level test; thus, the lifetime of the CFCP on board could meet industry specifications because the test condition (−55°C to 125°C) in this study was more severe than those in the previous studies, which used 0°C to 100°C or −40°C to 125°C,[13] and TCT for 1000 cycles is an acceptable criterion for commercial prototypes.[14] Furthermore, the bump crack issue after temperature cycling found in the previous study[15] did not occur here, even though the coreless substrate warped more easily. Based on the results, it can be said that the CFCP showed acceptable reliability when mounted on a printed circuit board, although it demonstrated inferior component-level reliability.

Solder joint failure was induced in this study by fracturing of the solder ball close to the substrate. The glass-transition temperature (T_g) of the coreless substrate is estimated to be 220°C, which is higher than the peak temperature in the TCT of 125°C; hence, the warpage of the coreless substrate was related to the CTE before the T_g point. That was obtained as 29.2 ppm/°C by thermomechanical analysis (TMA). In addition, the standard PCB before the T_g point expands at a rate of 18 ppm/°C, which is almost the same as that of Cu trace (17 ppm/°C). In fact, the warpage of the PCB was related to the Young's modulus of the materials and

the CTE mismatch between the Cu trace and the resin. Furthermore, the coreless flip-chip package was placed in the center of the PCB, and the thickness and Young's modulus of the PCB were much greater than those of the coreless substrate. Considering the size effect, the PCB was assumed to be flat during TCT. The warpage was induced by the coreless substrate but constrained by the PCB because of the interconnection of the solder balls. The bending stress on the underfill was shared with the solder balls, so the die cracking issue did not arise. On the other hand, the solder mask opening of the substrate was smaller than that of the PCB, which induced a lower standoff height and made the bump shape imperfect, like the solder joints of a solder grid array in a previous report.[15] Therefore, the stress accumulated and concentrated at the notch junction of the solder mask and the Pb-free solder ball as the temperature cycled, until the solder joints failed. The fracture formed at the corner solder bulk and then propagated along the interface between the intermetallic layer, and a brittle crack was found, as shown in Fig. 10. A larger solder mask opening at the substrate side (equal to or not less than 80% of that at the board side) is recommended to enhance the solder joint reliability during temperature cycling.

CONCLUSIONS

The thermomechanical stress/strain behaviors of the coreless flip-chip package and its board-level reliability have been investigated by both simulation and experiments. The important results of this work can be summarized as follows:

1. The package yield of the coreless flip-chip substrate was greatly improved by increasing the cooling rate during reflow, because this resulted in solidification of the solder joints at the outermost region before the coreless substrate adopted a concave shape.
2. Fracture of the outermost solder ball was the main failure mode under board-level TCT because the warping of the substrate was restricted by the interconnection with the PCB with about a 5% reduction of thermomechanical stress being obtained from the simulation model. As a result, the concentrated stress was dispersed from the die edge and shifted to the solder balls. The solder balls resisted the substrate deformation and the very large local CTE mismatch between the stiffener, substrate, and PCB.

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