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Electrical Characteristics of Hybrid-Organic Memory Devices Based on Au Nanoparticles

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We report on the fabrication and characterization of hybrid-organic memory devices based on gold (Au) nanoparticles that utilize metal–insulator–semiconductor structure. Au nanoparticles were produced by sputtering and inert-gas condensation inside an ultrahigh-vacuum compatible system. The nanoparticles were self-assembled on a silicon dioxide (SiO_2)/silicon (Si) substrate, then coated with a poly(methyl methacrylate) (PMMA) insulating layer. Aluminum (Al) electrodes were deposited by thermal evaporation on the Si substrate and the PMMA layer to create a capacitor. The nanoparticles worked as charge storage elements, while the PMMA is the capacitor insulator. The capacitance–voltage (C–V) characteristics of the fabricated devices showed a clockwise hysteresis with a memory window of 3.4 V, indicative of electron injection from the top Al electrode through the PMMA layer into Au nanoparticles. Charge retention was measured at the stress voltage, demonstrating that the devices retain 94% of the charge stored after 3 h of continuous testing.

Key words: Organic memory devices, nanoparticles, Au

INTRODUCTION

Memory devices are a key element of electronic devices to provide or store information for logic operation.[1] Research on memory devices has attracted many researchers to enhance the performance and reduce the size of the devices, which will lead to the development of novel structures.[2] Organic materials have received much attention due to their flexibility, ease of production, and low cost.[3–8] Those materials have applications in different fields such as organic solar cells,[5] organic light-emitting diodes (OLEDs),[6] sensors, and organic thin-film transistors (OTFTs).[3,7,8] Investigations on organic memory devices were established in the late 1950s; however, further experimental and theoretical studies are still needed to enhance their efficiency.[7]

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Nano-floating gate memory devices using metallic nanoparticles (NPs) as discrete charge storage elements are considered to be one of the promising memory devices for different applications.[4,9] These memory devices were reported to exhibit enhanced memory performance with long data retention time and lower operation power compared with conventional memory devices.[10] A main advantage of these embedded storage elements is the flexibility of their density, shape, size, and type, which can be easily controlled to lead to new structures and different impacts on the memory device.[11–15] Many types of metallic nanoparticles have been used as charge storage elements in memory devices, such as silver (Ag), gold (Au), copper (Cu), and aluminum (Al).[12–23]

Au nanoparticles have attracted a wide share of research attention due to their high work function and chemical stability characteristics compared with other metal nanoparticles.[17] To the best of our

knowledge, all previous reports on utilization of Au nanoparticles for memory devices used chemical methods to synthesize those nanoparticles.

The metal–insulator–semiconductor (MIS) structure is an important structure in electronics, being a building block of the most widely used components in computers and digital hardware. In this work, we investigated the utilization of the MIS structure as a hybrid organic–silicon memory device with Au nanoparticles as charge storage elements. The nanoparticles were prepared by sputtering and inert-gas condensation inside an ultrahigh-vacuum (UHV) compatible system. To the best of our knowledge, this is the first report on utilization of Au nanoparticles fabricated by sputtering and inert-gas condensation for organic memory devices. This technique of nanoparticle production has many advantages over the other techniques, such as:[24] the produced nanoparticles have high purity, since the nanoparticles are produced inside a UHV chamber (unlike nanoparticles prepared using chemical methods); size selection of nanoparticles is possible using a mass filter, since the produced nanoparticles are charged; the produced nanoparticles have a narrow size distribution; the size of the nanoparticles can be easily tuned within a range of sizes that correspond to the source design; the produced nanoparticles can be self-assembled directly on a substrate to create a device; and the coverage of nanoparticles deposited on a substrate is controllable by controlling the deposition time.[25–28] Therefore, this technique could be utilized for production of nanoparticles for organic memory device applications on an industrial scale.

EXPERIMENTAL PROCEDURES

The structure of the fabricated device is shown schematically in Fig. 1, consisting of the following layers: aluminum back contact (~100 nm thick), *p*-type silicon substrate, silicon dioxide insulator (~10 nm), Au nanoparticles (~5 nm thick), poly (methyl methacrylate) (PMMA), and aluminum front contacts (~100 nm thick). Commercial *p*-type silicon wafers coated with a SiO_2 layer were used as a substrate for the device. The wafers were originally coated with photoresist protection layers to prevent growth of a SiO_2 layer. Thus, the photoresist layer was removed and the wafers were cleaned prior to deposition of Au nanoparticles.

Nanoparticle Production

Au nanoparticles were prepared using a sputtering and inert-gas condensation technique inside a UHV compatible system as shown schematically in Fig. 2.[24,29,30] The system was evacuated using two turbo pumps (TPs) to a base pressure of $\sim 10^{-8}$ mbar. The nanoparticles were produced from a 99.99% pure Au target fixed on a water-cooled magnetron sputter head inside the source chamber. The sputter head was mounted on a motorized linear translator so its

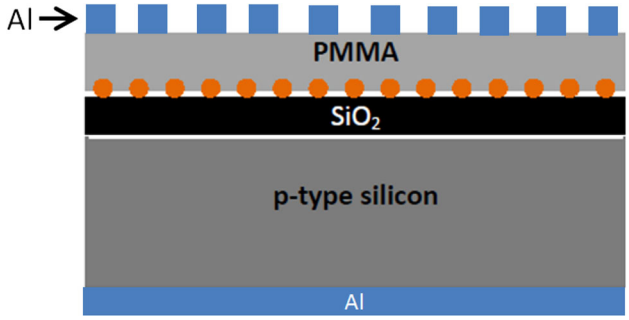

Fig. 1. Schematic of MIS structure utilizing embedded metallic nanoparticles as charge storage elements.

location, defined as the aggregation length (L), could be varied without venting the UHV system. The plasma was generated using 99.999% pure argon (Ar) gas with flow rate (f_{Ar}) controlled between 0 sccm and 100 sccm using an MKS Instruments mass flow controller. The nanoparticles were produced inside the source chamber and then traveled to the deposition chamber through two nozzles, forming a beam of nanoparticles. The deposition rate could be measured using a quartz crystal monitor (QCM) placed on a motorized linear translator that allowed it to be placed in front of the nanoparticle beam to measure the nanoparticle deposition rate, and then pulled back, away from the nanoparticle beam. The nanoparticle size and deposition rate could be varied by controlling three main factors: f_{Ar}, L, and the sputtering discharge power (P).[24,31] The nanoparticle size distribution could be measured inside the UHV system using a quadrupole mass filter (QMF) placed between the source and deposition chambers.[24] Au nanoparticles used in this work were produced using f_{Ar} = 80 sccm, L = 60 mm, and P = 119 W. Figure 2c shows the size distribution of Au nanoparticles as measured using the QMF. The produced nanoparticles exhibited an average size of 4.8 ± 0.2 nm. Au nanoparticles were self-assembled on SiO_2/Si substrates fixed on a rotating table (Fig. 2a). The rotation of the substrate guarantees a uniform distribution of nanoparticles.

PMMA Dielectric Layer

Three different PMMA solutions were tested for the dielectric layer and used for device fabrication in this work. PMMA solutions were prepared in chloroform (CF), chlorobenzene (CB), and anisole. The solutions were applied onto the Au-NPs/SiO_2/Si substrates by spin coating, performed initially at 500 rpm for 10 s, then at 6000 rpm for 50 s. The samples were annealed at 120°C for 1 h.

Tests

Aluminum electrodes were deposited by thermal evaporation on the Si substrate and PMMA layer to create a capacitor structure. All capacitance–voltage (C–V) tests were carried out at room

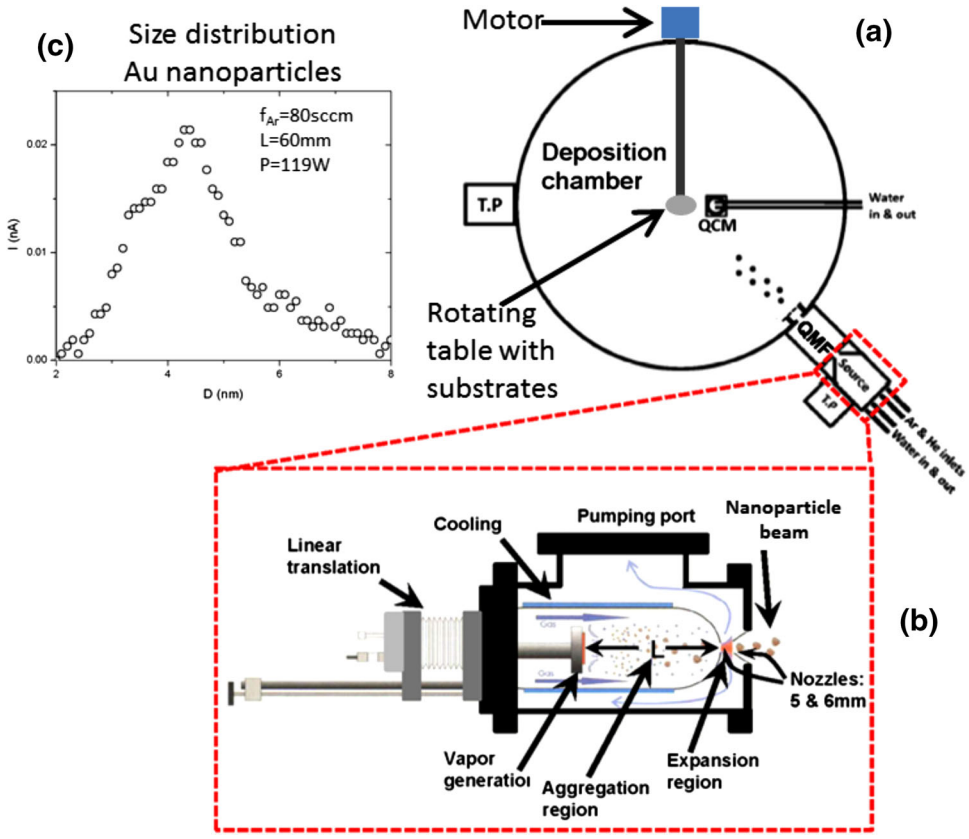

Fig. 2. Schematic of UHV nanoparticle deposition system (a) and source chamber (b),[24,30] where the QMF is placed between the source and deposition chambers. (c) Size distribution of Au nanoparticles as measured using the QMF.

temperature inside a test chamber. *C–V* tests were performed using an *LCR* impedance analyzer (HP4192) at voltage ranging between −6 V and 6 V and a double sweep. The frequency was varied between 1 kHz and 2 MHz. Atomic force microscope (AFM) was used to image Au nanoparticles.

RESULTS AND DISCUSSION

Reference Device

Figure 3 shows the *C–V* characteristics of an Al/SiO_2/Si/Al reference device at two different frequencies. Negligible hysteresis can be observed in the figure. The *C–V* curves are slightly shifted toward the positive voltages, with a center at about 0.5 V. This suggests the presence of negative trapped charges according to Eq. 1.

$$V_{FB} = \phi_m - \phi_S - \frac{Q_{SS}}{C_{ox}}, \quad (1)$$

where V_{FB} is the flat-band voltage (beginning of the depletion region), ϕ_m is the metal work function, ϕ_S is the semiconductor work function, Q_{SS} is the equivalent trapped oxide charge per unit area, and C_{ox} is the oxide capacitance. Since ϕ_m and ϕ_S are fixed, V_{FB} will have the opposite sign to that of the equivalent trapped oxide charge.

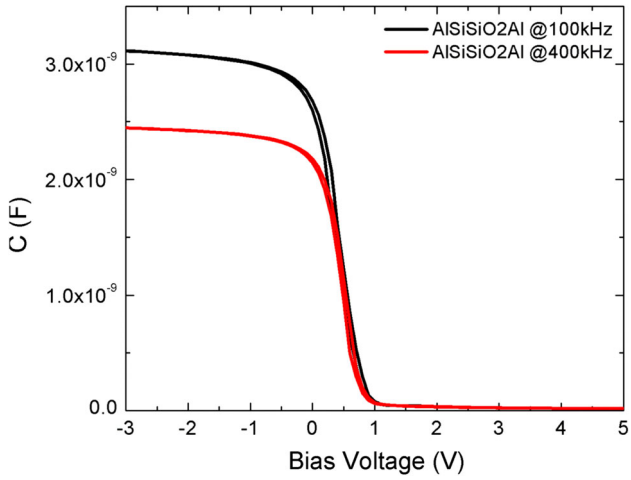

Fig. 3. *C–V* measurements of a reference device with Al/SiO_2/Si/Al structure at two frequencies.

The accumulation capacitance for the 100 kHz frequency measurement is higher than that for 400 kHz: 3 nF and 2.5 nF, respectively. This

difference is attributed to marginal differences in oxide thickness and device area, and experimental error.[28] The SiO_2 thickness can be calculated using Eq. 2.[32,33]

$$C_{max} \cong C_{Ins} = A\frac{\varepsilon_{Ins}}{d_{Ins}} = A\frac{\varepsilon_0\varepsilon_{ox}}{d_{ox}}, \quad (2)$$

where A is the device area = 0.785×10^{-6} m^2, ε_{Ins} is the permittivity of insulator/oxide, d_{Ins} is the cumulative insulator thickness, d_{ox} is the SiO_2 thickness, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space, and $\varepsilon_{ox} = 3.9$[33] is the relative permittivity of SiO_2. Equation 2 yields $d_{ox} = 10.8$ nm using the maximum capacitance at 400 kHz, and 9.0 nm using the maximum capacitance at 100 kHz. These values are close to the value quoted by the wafer manufacturer (10 ± 1 nm).

The capacitance at the flat-band voltage can be used to determine the intrinsic doping concentration (N_a) of the applied semiconductor (Si in our case) from the following equation[34]:

$$C_{FB} = A\frac{\varepsilon_{Ins}}{d_{Ins} + \frac{\varepsilon_{Ins}}{\varepsilon_s}\sqrt{\frac{K_bT}{e}\frac{\varepsilon_s}{eN_a}}}, \quad (3)$$

where C_{FB} is the flat-band capacitance, K_b is the Boltzmann constant, T is the temperature in Kelvin (300 K), $d_{Ins} = 10$ nm, $\varepsilon_{Ins} = 3.9\varepsilon_0$, $\varepsilon_s = 11.9\varepsilon_0$[33] is the semiconductor permittivity, and e is the electron charge.

The flat-band capacitance measured at 400 kHz is 2 nF according to Fig. 3, thus Eq. 3 results in a doping concentration of $\sim 1.45 \times 10^{23}$ m^{-3}. In the inversion region, majority carriers are repelled from the insulator interface and gradually depleted due to the increase in the positive bias at the gate. Therefore, only minority carriers accumulate at the interface and produce the minimum capacitance in the C–V curve. The minimum capacitance (C_{min}) corresponds to the semiconductor and insulator capacitors in series. From this value, the maximum depletion width (W_{max}) can be calculated using Eq. 4.[34]

$$C_{min} = \frac{C_{Ins}}{1 + \frac{C_{Ins}}{C_S}} = A\frac{\varepsilon_{Ins}}{d_{Ins} + \frac{\varepsilon_{Ins}W_{max}}{\varepsilon_S}}, \quad (4)$$

where C_{Ins} is the insulator capacitance connected in series with a semiconductor capacitance (C_S). From Fig. 3, $C_{min} = 4 \times 10^{-11}$ F, thus W_{max} equals approximately 22 μm.

PMMA Selection

Figure 4 shows the C–V curves of three reference devices with Al/PMMA/SiO_2/Si/Al structure obtained using PMMA solutions in chloroform, chlorobenzene, and anisole. The figure reveals that the sample coated by PMMA in CB produced the highest capacitance, thus this solution was used as an insulator for the fabrication of memory devices. The

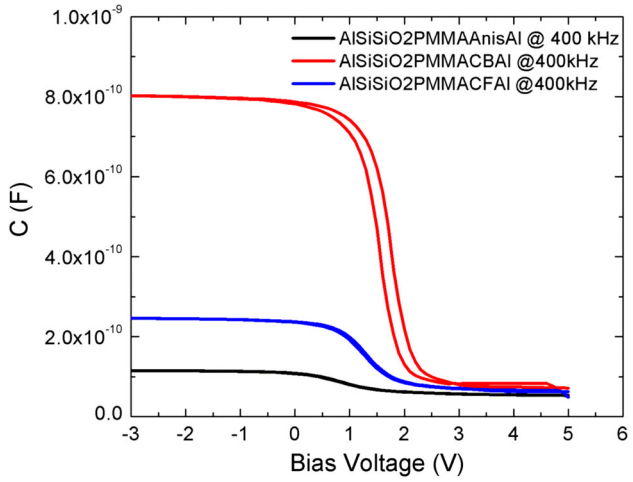

Fig. 4. C–V measurements for reference devices with Al/PMMA/SiO_2/Si/Al structure obtained using three different PMMA solutions. The measurements were performed at 400 kHz.

PMMA layer thickness was calculated using the following equation[35]:

$$d_{PMMA} = \frac{\varepsilon_{PMMA}\varepsilon_0}{C_{PMMA}}A, C_{PMMA} = \frac{C_{ox}C_{max}}{C_{ox} - C_{max}}, \quad (5)$$

where d_{PMMA} is the PMMA layer thickness, $\varepsilon_{PMMA} = 3.7$ is the relative permittivity of PMMA,[36] and C_{PMMA} is the capacitance of the PMMA layer. C_{ox} is the maximum capacitance for the reference device in Fig. 3, where the maximum capacitance represents the oxide capacitance of the device only (Eq. 2). C_{max} is the maximum capacitance that includes both PMMA and oxide capacitors in series. Equation 5 yields thicknesses of $d_{PMMA\text{-}CB} \approx 49$ nm, $d_{PMMA\text{-}CF} \approx 200$ nm, and $d_{PMMA\text{-}Anisole} \approx 490$ nm. The highest capacitance is associated with the least thickness, thus PMMA in CB was chosen for device fabrication.

Comparing the C–V curves for reference devices with PMMA (Fig. 4) and without PMMA (Fig. 3), it is noticed that the curves are shifted to more positive voltages in Fig. 4. This indicates that the PMMA solution contains trapped negative charges so the device needs more positive charge to reach the flat-band voltage and start charging the device in the accumulation region. Also, the accumulation capacitance for the device decreases from ~ 2.5 nF without PMMA to ~ 0.8 nF for CB-PMMA at 400 kHz. This decrease is due to the increase in the insulator thickness (see Eq. 5).

Devices with Storage Elements

Atomic force microscopy imaging was carried out for Au nanoparticles deposited on SiO_2/Si substrates as shown in Fig. 5. The nanoparticle size can be estimated as 5 nm, which is consistent with the average size as measured using the QMF in Fig. 2.

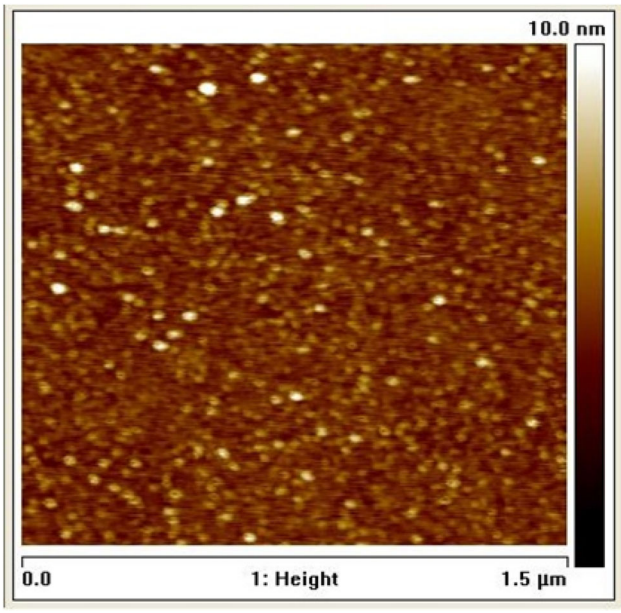

Fig. 5. AFM topographical image for the Au nanoparticles.

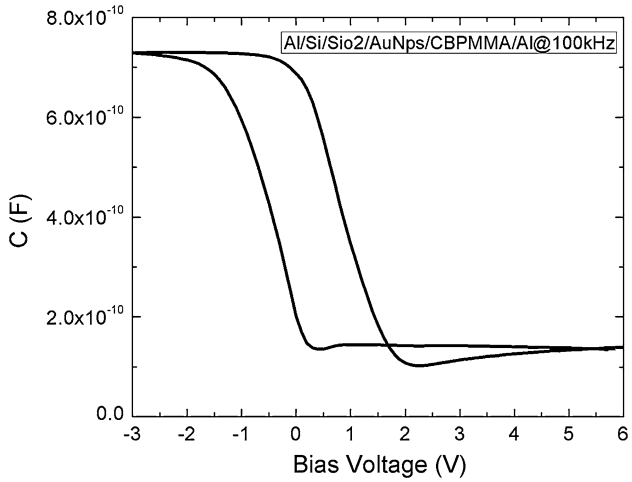

Fig. 6. *C–V* measurements of a memory device with Al/CB-PMMA/Au-NPs/SiO_2/Si/Al structure.

Figure 6 shows the *C–V* curve of an Al/PMMA/Au-NPs/SiO_2/Si/Al device. The figure reveals a hysteresis window which demonstrates that Au nanoparticles work as charge storage elements. Similar behavior was observed for all tested devices. The *C–V* curve in Fig. 6 exhibits a clockwise hysteresis, with a window of 1.75 V. The curve is centered at −0.5 V approximately, and its flat-band voltage is at −1.25 V. The center of the hysteresis is close to zero, which is the optimal value for low operating voltage and to reduce overheating. The shift in the center to the negative voltage indicates that there are positive charges trapped within the dielectric, although negative trapped charges were found in the PMMA and SiO_2 layers for the reference devices before adding the nanoparticles. This suggests that the trapped positive charges are associated with Au nanoparticle deposition, which can be rationalized given that the majority of nanoparticles produced by sputtering are charged.[24]

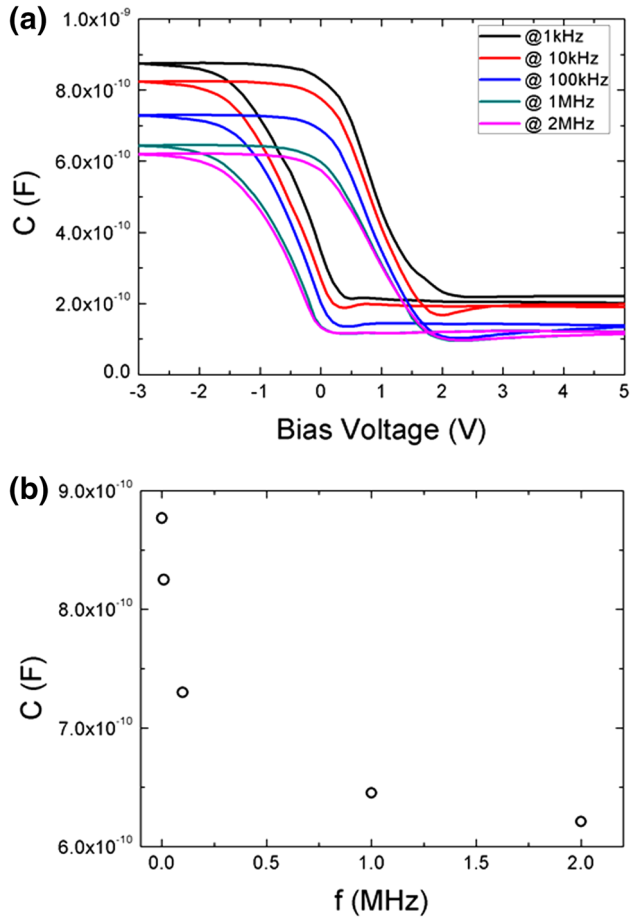

Fig. 7. (a) *C–V* measurements of a Au nanoparticle-based memory device with Al/CB-PMMA/Au-NPs/SiO_2/Si/Al structure at different frequencies. (b) Maximum capacitance as a function of frequency.

Capacitance–voltage curves of all measured samples exhibited clockwise (CW) hysteresis, where each *C–V* curve starts from the inversion region to the accumulation region and then returns back to inversion. This behavior, similar to that of *p*-type semiconductors, results from ion drift or polarization. Previous studies[37,38] suggest that the clockwise hysteresis results because Au nanoparticles are charged by electrons injected at the accumulation region where negative voltage is applied from the top electrode. However, if electrons were injected through the SiO_2 layer, the *C–V* curves would show counterclockwise hysteresis. At the inversion region (positive voltage applied), electrons are extracted from the nanoparticles to the top electrode and the nanoparticles are discharged. Electrons are injected and extracted through the PMMA layer, where less resistance exists for effective tunneling and carrier transportation.[39]

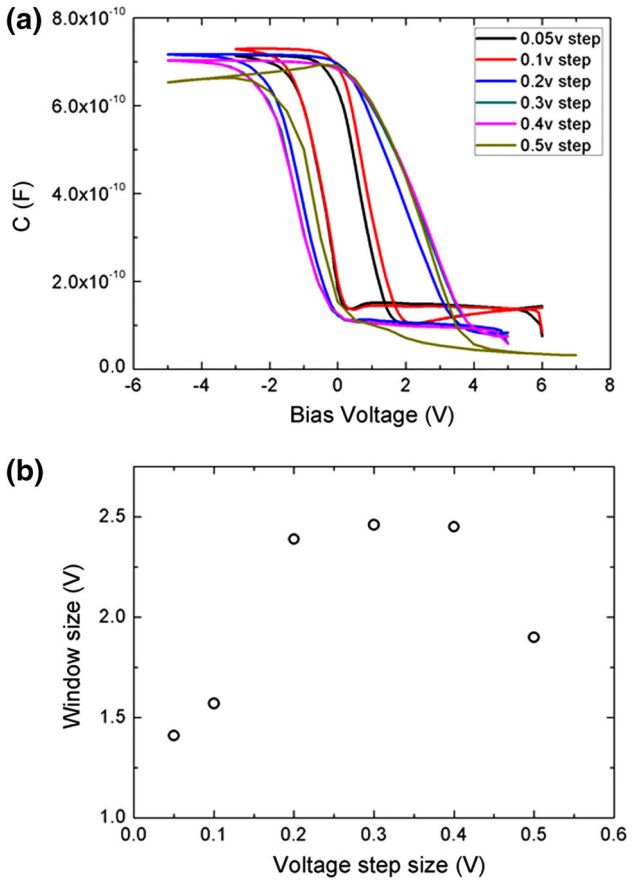

Fig. 8. (a) *C–V* measurements of a Au nanoparticle-based memory device with Al/CB-PMMA/Au-NPs/SiO_2/Si/Al structure for different voltage scanning steps. (b) Variation of hysteresis window size as a function of voltage step size.

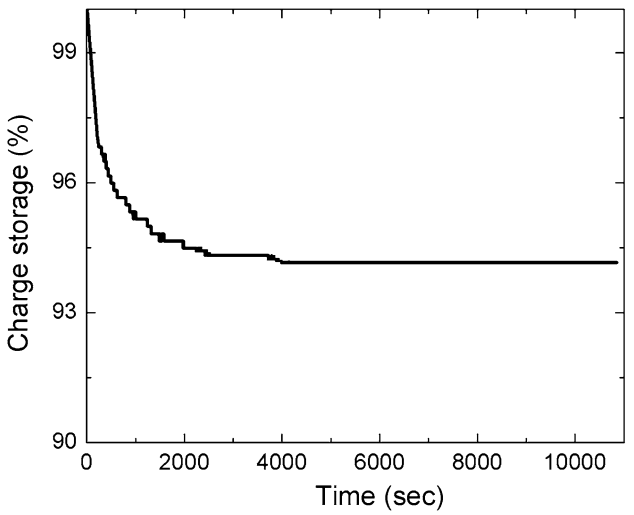

Fig. 9. Charge retention measurements for a Au nanoparticle-based memory device with Al/CB-PMMA/Au-NPs/SiO_2/Si/Al structure.

To study the frequency dependence of the *C–V* curves, tests were carried out at different frequency values from 1 kHz to 2 MHz (at a step voltage of 0.1 V), as shown in Fig. 7a. The maximum capacitance as a function of frequency is shown in Fig. 7b. The figure shows that, as the frequency increases, the maximum capacitance decreases exponentially. At high frequencies, the inversion layer caused by minority carriers (electrons for *p*-type MIS) will not respond as quickly as at low frequencies.[37] This is a result of the rapidly changing bias voltage at high frequencies, where the inversion layer will not respond quickly and will show a reduction in capacitance. In addition to the capacitance decrease with increasing frequency, the effect of impurities (interface trap charges) is reduced at high frequencies, where charging and discharging cannot respond as quickly as at low frequencies. This can be noticed in Fig. 7 where the *C–V* curves for high frequencies are slightly shifted to negative voltages. It should be noted here that differential pulse voltammetry measurements could be used to determine whether quantized capacitive charging of nanoparticles (suspended in solution) is adding to the voltage shift.

The effect of the scan voltage step size on the *C–V* curves is shown in Fig. 8a (at frequency of 100 kHz). Figure 8b shows the dependence of the hysteresis window size (measured at the flat-band voltage) on the scan voltage step size for each *C–V* curve. The two figures demonstrate that, as the scan voltage step size increases, the hysteresis window size increases until 0.2 V. The hysteresis window size becomes constant between 0.2 V and 0.4 V, and then it decreases at 0.5 V. The best hysteresis window size was found to be 3.4 V for a voltage step size of 0.3 V, as shown in Fig. 8. The amount of charge per unit area for this device was found using $Q = C\Delta V$. From Fig. 8a, $C = 7 \times 10^{-10}$ F and $\Delta V = 3.4$ V, thus $Q = 2.4 \times 10^{-9}$ C, which gives a charge density $Q_p = Q/A = 3 \times 10^{-3}$ C/m^2.

Charge retention was measured at the stress voltage for the above device (with a hysteresis window of 3.4 V) using a double *C–V* voltage scan. The voltage scan was used to determine V_{FB}, then a 2-s pulse was applied with $V < V_{FB}$ (−3 V was used in this experiment). The charge retention was determined from the capacitance measurement of a device as a function of time. The charge retention measurement is shown in Fig. 9, demonstrating that the device retained 94% of the charge stored for more than 3 h of continuous testing. This result demonstrates that the device exhibits excellent charge retention capacity. Furthermore, the measured percentage of retained charge is higher than the previously reported value for memory devices utilizing Au nanoparticles, i.e., 87%,[18] or alloy of Au nanoparticles, i.e., 75%.[40]

CONCLUSIONS

Organic–silicon hybrid MIS memory devices based on PMMA and gold (Au) nanoparticles were fabricated and characterized in this work. Au nanoparticles were fabricated using a sputtering and inert-gas condensation technique inside an

ultrahigh-vacuum compatible system. *C–V* measurements were carried out for all fabricated devices, all of which exhibited hysteresis windows with centers at small voltages (~0.5 V). Devices with embedded Au nanoparticle storage elements showed clockwise hysteresis. The nanoparticles were charged by electrons injected at the accumulation region where negative voltage was applied from the top electrode. The maximum capacitance value was dependent on the measurement frequency and step voltage scanning rate. The devices were found to retain 94% of the charge after 3 h of continuous testing. This work demonstrates that Au nanoparticles fabricated by sputtering and inert-gas condensation are suitable candidates for use as storage elements for memory devices with large hysteresis window. Such devices could have potential applications in the field of organic memory devices.

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