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High-Performance, Wide-Bandgap Power Electronics

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APEI has developed high-performance electronics to exploit the unique capabilities of wide-bandgap devices. Crucial enabling features include high current density, fast switching speed, high-voltage (>10 kV) blocking, high-temperature operation (>200°C), and inherent radiation tolerance, features which have the potential to completely revolutionize existing electronics, from milliwatt to megawatt levels, and enable operation in new environments. Full realization of these extraordinary capabilities led to significant challenges in package and system design, including high electric fields, high power density, high di/dt's and dv/dt's, and high temperatures. Because of the limitations of traditional design methods and traditional electronics, designers unknowingly lack understanding of packaging material thermal properties at temperature extremes, of package-fabrication techniques, and of the inability to operate continuously at elevated temperatures, and use a set of qualification standards designed for lower-temperature, previous generation technology.

Key words: Wide bandgap, silicon carbide, power electronics, power packaging, high temperature, high performance, high frequency, reliability

BACKGROUND

Power electronic systems are being applied more than ever and can be found in almost every application powered by electricity, from laptop power supplies to traction drives and battery-management systems in hybrid electric vehicles and mobile smart device chargers, to name just a few. In Ref. 1 it was predicted that the total energy processed by power electronics, which is currently approximately 30%, will be 80% in 2030. To save consumer space, enable increased performance, and reduce purchase and operating costs such systems must become smaller and more efficient.

Wide-bandgap (WBG) devices, for example those manufactured from silicon carbide (SiC) and gallium nitride (GaN), enable the design engineer to investigate how high power density and high efficiency can both be used to enable new applications and increased performance. In these devices junction temperatures >200°C are possible, enabling reduction of the size or complexity of the thermal management system. In addition, the devices also have significantly fewer on-state conduction losses and higher switching speed, even at elevated temperatures. This faster switching speed enables traditional applications, for example DC/DC converters, typically switched at 100s of kHz, to be extended well into the megahertz (MHz) range. This dramatic increase in switching frequency enables reduction of system size by use of smaller magnetic components and capacitors.

Reduction in the size and complexity of the thermal management system, and the increased switching frequency enable a tenfold increase in power density.[2] This dramatic increase in power density does come at a price, however. There is now a need to implement a new means of making semiconductor chips compatible with the system load. This starts at the chip pad terminals and extends through the method of interconnection, package

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bussing, and system bussing. In its simplest form this process can be reduced to modification of the power module, high-frequency capacitors, bus capacitors, drive electronics and power supplies, and bussing. This combination is loosely termed the power module system, and is a highly complex system in itself, including:

1. an electrical domain: the interaction over temperature of the semiconductors, parasitic packaging elements, control signals, power signals, ballasting and clamping mechanisms, and voltage-withstand capability;
2. the mechanical domain: void-free die attachment, low coefficient of thermal expansion (CTE) mismatch, rugged construction as protection against shock and vibration, strong terminal attachment for rigid bussing attachment, close mounting of auxiliary components for low inductance, and ultra-low junction-to-case thermal resistance; and
3. the chemical domain: high-dielectric-strength materials for high electric fields, materials capable of maintaining favorable electrical and mechanical properties at high temperature, and low outgassing materials.
4. the thermal domain: high thermal conductivity materials capable of temperature extremes, optimized trade-off between low CTE mismatch, voltage withstand capability, thermal interface conductivity, and voiding.

It is apparent the power module is a system of small, interdisciplinary subsystems, all intimately compatible, working in sync over ranges of power levels, temperatures and environmental conditions.

HIGH-TEMPERATURE PACKAGING REQUIREMENTS

For electronics to operate reliably at temperatures greater than 150°C, the materials, components, and processes used to package the devices must be compatible with the high-temperature operating conditions. Common materials and components used in high-temperature electronics packaging include die attachments, substrates, interconnections, potting or encapsulation, case, and heat spreader or baseplate. It is typically at the interfaces within these components (e.g., metal bonded to a ceramic to form a substrate) or where these components are connected together (e.g., a substrate soldered to a mechanical baseplate) that failures occur as a result of the effects of thermal or power cycling.

Crucial properties of high-temperature die-attachment materials include high thermal conductivity, minimum CTE mismatch between die and substrate, high electrical conductivity, compatibility with different industry standard die–substrate metallization, high reflow temperature, low thermal and mechanical fatigue, high operation temperature, and low cost. The thermal conductivity of some of the more common high-temperature die-attachment solders, in order of reflow temperature, are listed in Table I. One disadvantage of most of these solders is their relatively high CTE. High-CTE solders can cause cracking and, ultimately, device failure because of different rates of deformation as temperature changes. Two high-temperature die attachments used in a variety of applications are gold–germanium 88:12 (Au88Ge12) and gold–tin 80:20 (Au80Sn20). Both solders provide great joint strength, high resistance to corrosion, compatibility with precious metals, high thermal conductivity, and low CTE compared with other solders.

Sintering pastes are an alternative to solder preforms and solder pastes, with the added advantages of being solvent-free, flux (residue)-free, having extremely high thermal conductivity (>100 W/mK), and requiring low processing temperatures. Sintering pastes are also an alternative to conductive adhesives, with the added advantages of long-term contact stability and high electrical conductivity. In general, sintering materials are processed similarly to adhesives. However, formation of metallurgical interfaces results in enhanced thermal and electrical properties.

Because of the harsh environments in high-temperature applications, potting, encapsulation, and case materials must withstand high temperatures while providing sufficient voltage blocking and protection from the environment. To prevent arcing within a package, gels have traditionally been used as the encapsulation materials of choice in power modules. Although these materials are extremely elastic, they are still prone to cracking and delamination during power cycling and at high ambient temperatures if appropriate materials are not selected. These materials can also lead to stress of wire bonds at elevated temperature, because of their high CTEs, eventually leading to disconnection. Thus, care must be taken when selecting the dielectric materials used in high-temperature packages.

Metal–matrix composites (MMCs) with low CTEs are typically used to reduce the thermal–mechanical stress induced in a package. Some of the more common MMCs include copper molybdenum, copper tungsten, copper graphite, aluminium graphite, and aluminium silicon carbide. One of the advantages of these materials is that their CTE can be adjusted to match the rest of the package assembly while retaining acceptably high thermal conductivity.

These components are typically attached by use of flux-free preforms in a vacuum reflow oven. Eliminating flux from the assembly is crucial. High-temperature flux residues are difficult to remove, may corrode wire bonds or sensitive surfaces, and trapped vapor on large-area bonds may lead to voids in the solidified bond. Void-free bonding can be achieved by surface preparation by plasma cleaning of the surfaces to be joined and both sides of the

Table I. Comparison of some common die attachment solder alloys

Solder alloy	Liquidus (°C)	Solidus (°C)	Density (g/cm^3)	Thermal conductivity (W/mK)	CTE (ppm/K)	Comments
Au80, Sn20	280	280	14.51	57	16	Pb-free, eutectic
Sn10, Pb88, Ag2	290	267	10.75	27	29	High-temp solder
Sn5, Pb92.5, Ag2.5	296	287	11.02	26	29	High-temp solder
Sn10, Pb90	302	275	10.75	25	29	High-temp solder
Sn2, Pb95.5, Ag2.5	304	299	11.20	–	–	Low Sn
Sn1, Pb97.5, Ag1.5	309	309	11.28	23	30	Low Sn, eutectic
92.5Pb, 5In, 2.5Ag	310	300	11.02	25	25	In adds fatigue resistance
Sn5Pb95	312	308	11.06	23	30	High-temp solder
Au88Ge12	356	356	14.67	44	13	High-temp eutectic

solder preforms, precision assembly hardware, and customized reflow profiles in a vacuum/pressure reflow oven. Low-profile, heavy-gauge power wire bonds with highly repeatable loop heights can be formed by use of a semi-automatic bonder. For long-term reliability, it is crucial that the wire bond material and pad metallization of the substrate and die are compatible such that a high-quality bond can be achieved and intermetallic diffusion is eliminated.

MODELING FOR HIGH-TEMPERATURE AND HIGH-FREQUENCY SOLUTIONS

When fully embraced by a designer, the nearly ideal characteristics of WBG devices can be used to achieve systems which are more efficient (reduced conduction and switching losses), higher-voltage, higher-current, higher-temperature, faster, more reliable, and ultimately smaller (reduced volume of the heat-removal system and smaller magnetic components, and filtering capacitors). These striking advantages are resulting in electronic systems which are revolutionarily more efficient, smaller, and capable of being implemented in environments in which conventional technology simply cannot operate.[3]

To fully capitalize on these advantages, it is imperative to develop new approaches to the requisite packaging, gate drive, and system-integration methods.[4] Conventional power packages, materials, and techniques severely limit the performance of these advanced devices. Specifically, increasing the peak current and temperature, while minimizing parasitic impedance, thermal resistance, and cost, are an enormous challenge.

Although several varieties of power module are now available for these devices, there are few suitable high-performance solutions. APEI's high-performance package (Fig. 1), specifically targeted at emerging WBG devices, improves on the thermal, mechanical, and electrical performance and high-temperature capability of established transistor outline (TO)-style housings at comparable or lower cost. The new packages are capable of withstanding 250°C peak temperatures, currents much greater than 50 A, 1200 V, and high-frequency (1 MHz and higher) switching. The package is capable of using either an upper substrate to flip-chip attach lateral parts (e.g., GaN) or more conventional approaches, for example wire bonding for vertical devices (e.g., SiC).

APEI has developed an adaptive modeling process,[5] in which an automatically configurable model is paired with finite-element analysis (FEA) and which determines response to a given change of conditions. This substantially increases the speed of the design process, enabling the designer to systematically evaluate thousands of potential configurations with minimum input beyond the initial modeling phase. To acquire the large volume of data generated (e.g., temperatures, weight, etc.), "sensors" are placed at regions of interest. Results are analyzed and informed decisions can be made which accurately assess design compromises.

By use of this approach, an adaptive computer-aided design (CAD) model of the custom package was developed and optimized to maximize heat removal and reduce parasitic impedances. For the purpose of comparison, a simulation model of the finished package and a TO-254 were established in COMSOL (a multiphysics FEA design tool). Each package model contained configurations for a Rohm Trench MOSFET (TMOS) SiC device[6] and a GaN Systems GaN-on-SiC HEMT.[7] Each package model assumes aluminium nitride (AlN) direct-bond copper substrates for interconnection and isolation and 80Au20Sn solder attachment. For the TO package, a copper–tungsten baseplate was assumed, and the custom package used an etched copper plate. Relevant properties over the range of temperatures used were applied for these materials, and thermal and electrical simulations under the same loading conditions were performed, to accurately contrast the performance of each package.

The thermal simulation models included an emulated heat sink (to imitate the effects of the package–heat sink interface). The power loss for the devices was set at 30 W, and sensors measuring peak, average, and minimum temperature were

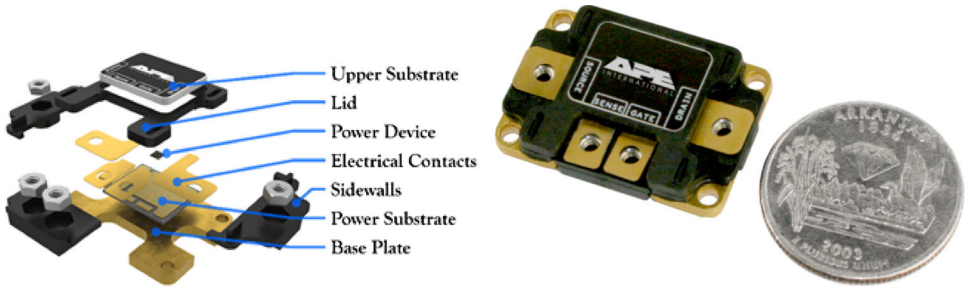

Fig. 1. Exploded view displaying the multiple substrate configuration for lateral power devices (left) and the completed package next to a US quarter as an indication of size.

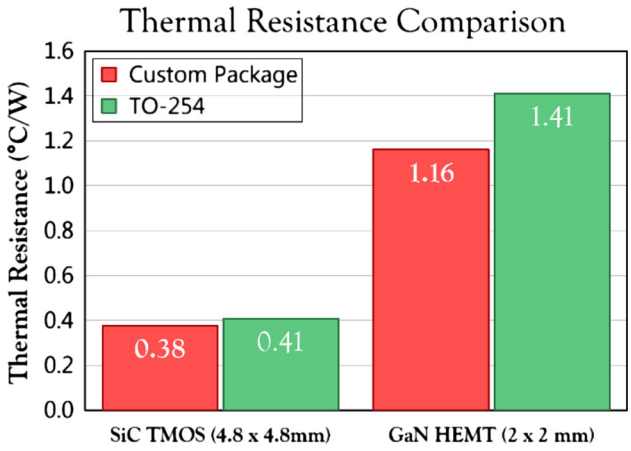

Fig. 2. Thermal resistance of both packages with two types of wide bandgap device.

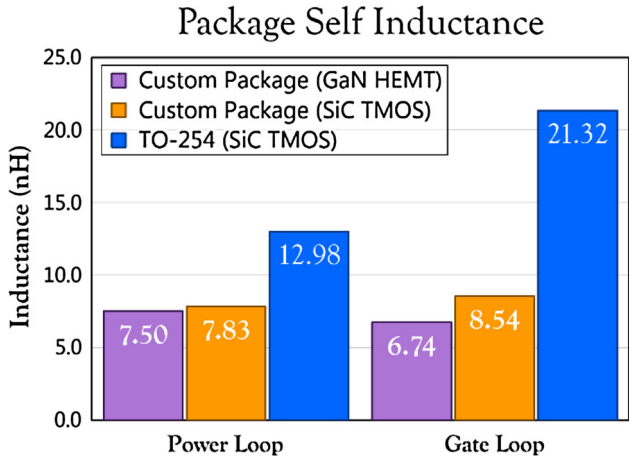

Fig. 3. Parasitic inductances of the power and gate loops of each package configuration.

placed in critical regions. Resulting junction-to-case thermal resistance ($R_{\theta j-c}$) data for the four variations are compared in Fig. 2. A small improvement (~0.03°C/W) is observed for the larger Rohm TMOS die, but a major difference (0.25°C/W) for the smaller GaN devices. This is in agreement with the tendency of smaller devices to benefit more from thermal spreading whereas better results for larger devices are obtained by use of thinner base plates.

Next, the parasitic impedances were extracted by using the AC/DC module in COMSOL. For these models, the electrical paths (including wire bonds) were modeled, as were the surrounding air and the return path (to close the electrical loop). The results, displayed in Fig. 3, are a compelling case for packages specifically designed for WBG devices. It is apparent both configurations of the custom package have a lower inductance than a similarly configured TO-254 package. The power loop is a factor of ~1.7× lower and the gate loop (cross sectional area of the electrical conduction path) is reduced by a factor of ~2.8×. This is chiefly because of the large, wide conduction planes, the low profile of the structure, and (for the SiC wire-bonded version) shorter and lower profile bond loops.

These direct advantages have a prominent bearing on the performance possible from currently available and forthcoming WBG devices. More current, higher temperatures, lower losses, and faster switching are all possible with the combination of innovative device design and superior packaging.

COMPONENT TESTING FOR HIGH-TEMPERATURE ELECTRONICS

WBG devices have enabled application of power electronics in extreme environments in which temperatures can range from cryogenic to well above the maximum operating limit of standard silicon technology. To accommodate this new device technology, materials that can also operate over a wide range of temperatures must be identified and vetted for reliability.[8]

Substrate Reliability

Commonly used substrate technology for power electronics includes direct-bond copper (DBC), direct-bond aluminium (DBA), and active metal braze (AMB). These substrates utilize two metal layers; typically, WBG devices would be attached to a side with the metal layer circuit routing whereas the bottom side is attached to a heat-spreader material. Between these two layers is a ceramic layer that provides electrical isolation, thermal

stability, and heat spreading capability. Because the ceramic and metal layers are dissimilar materials, their interface boundary can be a potential point of failure. To compare the substrate reliability of each technology, samples with different layer thickness and metal trace geometry were subjected to rapid thermal cycling from −50°C to +250°C. The substrate materials tested (metal/ceramic/metal thicknesses listed in milli-inches, or mil) were:

1. Direct-bond copper (DBC)

(a) 8/25/8 AlN
(b) 12/25/12 AlN

2. Direct-bond aluminium (DBA)

(a) 16/25/16 AlN
(b) 16/25/16 Si_3N_4

3. Active metal braze (AMB)

(a) 8/12/8 Si_3N_4

Visual inspection, by use of a digital microscope, and scanning acoustic microscopy (SAM) were used to evaluate the performance of the samples. SAM analysis is a non-destructive means of obtaining an image of the internal layers of a material by measuring the reflection of sound waves. Effectively, SAM analysis can be regarded as taking digital slices of a material. This analysis is required to find cracks that can develop in the ceramic beneath the metal layers—a failure that would not be noticeable by visual inspection only.

After 100 cycles, all of the DBC samples had suffered catastrophic mechanical failure. Figure 4 is a photograph of DBC samples with 12-mil copper layers on each side of a 25-mil AlN ceramic layer (12/25/12 AlN DBC). As seen in the photograph, the metal layer has become completely separated from the ceramic layer. On closer inspection it is evident the interfacial bond between the metal and ceramic layers is still intact. The failure occurred in the ceramic layer, probably because of the mismatch between the CTEs of the copper and ceramic layers. The resulting stresses that occurred during thermal cycling cracked the ceramic to the point of complete failure directly beneath the copper.

Figure 5 is a photograph of a side view of a piece of DBC with copper layers 8 mil thick and a AlN ceramic layer 25 mil thick (8/25/8 AlN DBC). It is apparent that the metal layers have begun to cause fracture of the ceramic beneath the copper traces. However, the thinner copper has not caused fracture of the underlying ceramic to complete failure and subsequent separation.

This type of failure was observed for all samples of DBC (28 in total), irrespective of size or geometry. Because these failures were classified as catastrophic, the DBC samples were excluded from subsequent tests.

The remaining DBA and AMB samples performed very well over the course of over 1000 cycles with no cracking of the ceramic substrate or delamination of the metal traces. This was consistent for all sizes and geometries.

Another effect that was noticed during SAM analysis was a change in surface roughness of the DBA and AMB samples that underwent thermal cycling. It is possible a similar result would have been obtained for the DBC samples, but none survived the first 100 thermal cycles.

When the SAM images were analyzed, the change in surface roughness was apparent when images of the upper surface at different times throughout the thermal cycle study were compared. The upper surface SAM image shown in Fig. 6 has a smooth surface, which is apparent from the uniform coloring across the surface. As the substrate undergoes thermal cycling, SAM images of the upper surface reveal signs of a change in surface roughness, apparent as the mottled pattern apparent in Fig. 7. Studies have shown that substrate surface roughness is important in determining the reliability of a package.[9] For example, if the surface roughness is minimized, stress induced in a die attachment or wire bond is minimized.

Passivation Reliability

Passivation and encapsulation materials are crucially important in WBG device technology because a WBG device is sometimes required to support its full voltage capability across drain and source (or anode and cathode). When tested in open air, some WBG devices could arc at higher voltages. Passivation and encapsulation materials are required not

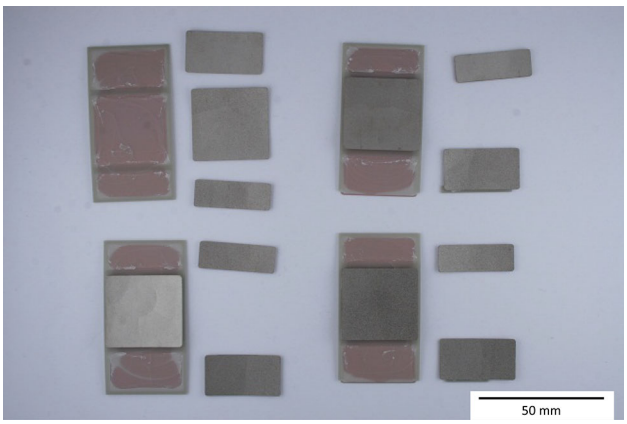

Fig. 4. Photograph of 12/25/12 mil AlN DBC samples after 100 cycles showing metal delamination from the ceramic.

Fig. 5. Photograph of 8/25/8 mil AlN DBC sample after 100 cycles showing cracking and bowing of substrate.

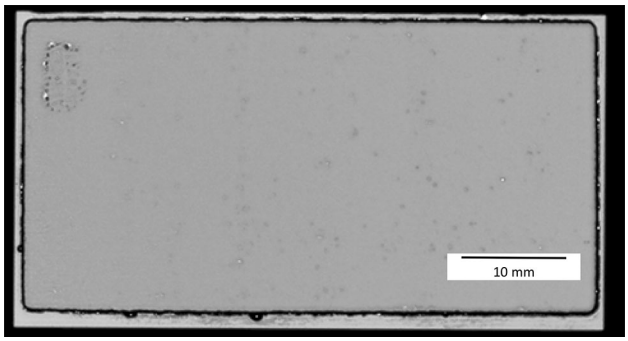

Fig. 6. Upper surface SAM image of an Si_3N_4 DBA substrate after 0 cycles.

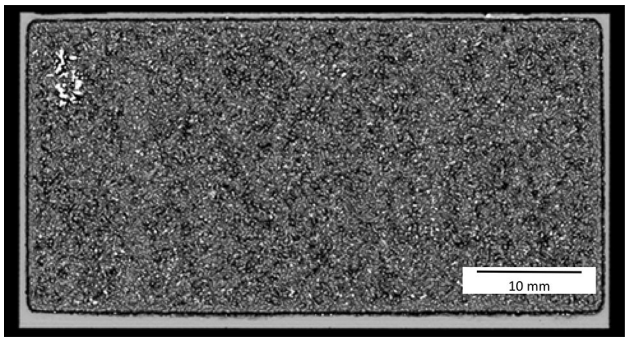

Fig. 7. Upper surface SAM image of an Si_3N_4 DBA substrate after 300 cycles.

only to protect the device from environmental conditions, for example humidity, but to help support high voltage operation. Because of thermal cycling or thermal ageing, these passivation and encapsulation materials can crack, delaminate, or harden over time; this is a potential source of failure that could be catastrophic for the entire system.

Thermal cycling was again used to compare the reliability of different passivation materials. The materials included silicon gels, hard silicone coatings, and chemical vapor deposition (CVD) polymers. The test sample was a SiC MOSFET in a TO-254 package which was coated with a passivation material. The samples were thermally cycled from −50°C to 250°C. After every 100 cycles, the samples were visually and electrically characterized to determine whether the passivation material had failed. The main electrical test of interest to determine passivation failure is high-voltage drain to source blocking capability. Because the SiC MOSFET cannot block the full rated voltage of 1200 V in open air, a passivation failure would cause a portion of the device to be exposed to open air and, therefore, catastrophic failure. Additional electrical tests are used to find device failures independent of passivation failing—in which case the device failure would not be included in the results. The results of this testing are presented in Fig. 8.

As is apparent from Fig. 8, two out of four of the silicone passivations performed very well and did not suffer a single failure through 800 cycles. Failure of the other two silicone passivations increased with increasing number of cycles.

SYSTEM CONSIDERATIONS

World-wide competition requires design and manufacture of high-performance power electronic systems to be cost competitive, with long life, high performance, and high reliability. High-performance power electronics can be characterized by one or more of the system attributes: high frequency, high efficiency, high power, high reliability, high radiation tolerance, high temperature, minimum size, minimum form factor, and minimum weight, among others. In many applications, for example the automotive and aerospace industries, power electronics are correctly regarded as the basis of the system. It is here that the system attributes listed above lead to the use of using WBG rather than silicon-based power electronics.

There are several theoretical reasons why WBG power electronics add significant value at the system level. A key metric of significant interest to end users is the overall benefit of replacing a silicon-based power electronic system with a WBG-based one; this is usually reduced to a single metric—overall reduction in system cost. Unfortunately, no generally accepted or widely known method can be used for rigorous quantification of the tangible and intangible cost benefits of using WBG power electronics, and the argument must be handled on a case-by-case basis. Use of WBG power electronics gives rise to system-level improvements compared with silicon, as stated below.[10]

1. WBG-based unipolar power devices can be designed to be thinner and with lower on-resistance than their Si counterparts. The lower on-resistance will result in lower conduction losses, and thus lower heat dissipation and, ultimately, higher overall converter efficiency. The higher converter efficiency enables use of less energy and reduction or perhaps elimination of the thermal-management system, or at least transition to a passive approach. Hence, simple reduction in conduction losses has a positive effect on overall system cost, volume, and mass. For the specific case of hybrid electric vehicles (HEV), electric vehicles (EV), or commercial transportation HEVs/EVs (e.g., buses, trains, trucks, semi-tractors, etc.), minimizing vehicle weight means less energy is required to propel the vehicle, the batteries retain their charge longer, vehicle range increases, overall efficiency is better, less fossil-based fuel is used by the HEV, and less electric energy from fossil fuel-burning generating plants is used. Of course, this leads to a reduction in air pollution by greenhouse gases (e.g., CO_2, CO, NO_x) and airborne particulates from diesel-powered hybrids, leading to better respiratory health.

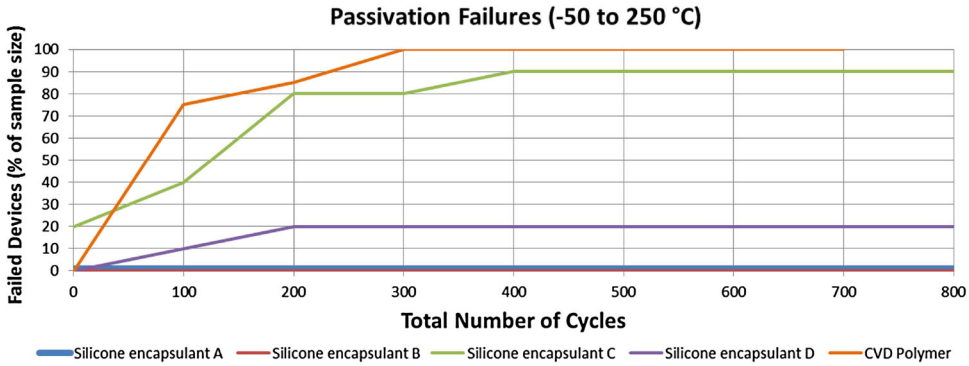

Fig. 8. Passivation failures as a percentage of total sample size.

2. WBG-based power devices can achieve higher breakdown voltages and lower leakage currents because of their higher electric breakdown field. At the system level, the higher breakdown voltage enables a single switch position versus series-connected switches or reduction of the number of electrical levels in a given application. The resulting more compact electrical, and by default mechanical, design results in smaller size, a smaller form factor, and lower mass. Furthermore, with reduced switch count, circuit complexity and cost are substantially reduced (e.g., removing voltage balancing passive networks, etc.) and may reduce control complexity as a result of the use of fewer gate drivers and associated power supplies. As overall system part count decreases, in general, the reliability of the overall system increases.
3. WBG-based power devices, particularly SiC, have higher thermal conductivity (i.e., 490 W/mK for SiC and 130 W/mK for GaN,[11] although thin GaN layers are typically on thinned Si or SiC substrates) than silicon devices. This implies that WBG-based power devices can have lower junction-to-case thermal resistance per unit area, with proper packaging, resulting in a higher heat flux from the power device to the heat sink. This will enable the user to increase the amount of processed power in the system or reduce the rate of temperature rise at the device's junction resulting in a lower steady-state junction temperature for similar losses. As a result, the thermal-management system can be reduced in size and complexity (less cost), or alternatively, for the same thermal system capacity, capacity can be increased before the maximum junction temperature of the power device is reached. This usually results in increased system reliability.
4. WBG-based power devices can operate at higher temperatures. The state of the art of SiC-based electronics and sensors enables proper operation up to 600–650°C,[12] and SiC PiN diodes operating at 900°C have been reported.[13] Silicon devices, on the other hand, can operate reliably at a maximum junction temperature of 150°C (or 175°C for automotive-grade power devices) for short periods. Depending on the ambient temperature, the cooling loop temperature (e.g., 70°C, 85°C, or 105°C), and the total power loss of the power electronics, the circuit designer can now choose among no heat sink, a passively-cooled heat sink, forced-air heat sink, liquid-cooled cold plate, or a more exotic cooling method. From a systems perspective, additional mechanical losses associated with thermal cooling loop—pump, heat exchanger and radiator, and fan to move air past the radiator coils—must be taken into account when evaluating overall system efficiency and cost of WBG versus silicon-based systems.
5. WBG-based bipolar power devices have excellent stored charge recovery characteristics. With less stored charge, there is a reduction in reverse recovery currents in diodes, switching losses, and electromagnetic interference (EMI), thus there is less or no need for power device snubbers and input/output EMI filters. This results in a reduction of volume and weight that results in system cost savings, as mentioned above.
6. The switching frequency of power devices is limited by the power device's switching losses. Because WBG devices are smaller, and because of the transition from Si bipolar to WBG unipolar and/or less stored charge in WBG devices, switching losses are greatly reduced in comparison with Si, enabling WBG devices to operate at higher switching frequencies (>20 kHz) and higher power. An ancillary system benefit of switching power devices above 20 kHz is less audible noise. Also, faster switching can provide many more opportunities to initiate control decisions (i.e., once every switching period) resulting in better system control and better system performance. Last, waveforms containing high-frequency components (i.e., harmonics of the switching frequency) are easier to filter, leading to smaller passive energy-storing components and a resulting overall gain in gravimetric and volumetric power density.

CONCLUSION

The above mentioned advantages of wide bandgap electronics coupled with high-performance packaging and controls enable many new ways to design and implement power electronic systems. The main system-level benefits are:

1. increased efficiency as a result of the use of better semiconductors;
2. increased power density as a result of high $T_{j,\max}$ and switching frequency;
3. reduction in thermal management system size or complexity;
4. environmental challenges overcome; and
5. new topology with increased performance can be considered.

It is apparent WBG devices result in a multitude of system advantages. However, these system advantages require power modules to be designed from the inside out, with WBG devices being designed on the basis of advanced models and design techniques, taking into consideration the more ideal nature of the devices compared with Si components. Electrical parasitics now have different effects and must be taken into account differently, for example by reducing electrical paths or providing compensating elements. As the power module and driver system become more closely coupled, higher dielectric strength materials and temperature capability are required. Because these new electronics can be used in extreme environments, new packaging techniques and materials are required. The benefits of WBG electronics are well known at the device level, but support packaging, controls, passive elements, and circuit design techniques must be used to take power electronics beyond incremental changes to today's Si-based solutions.

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