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Reliability Investigation of Cu/In TLP Bonding

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Die-attach bonding was evaluated using a transient liquid phase (TLP) bonding method on a Cu/In, Au/In and Cu-Sn3Ag metal stack. TLP bonding is a relatively low cost process since thin layers of material are used and, at the same time, has higher reliability due to the good thermal resistance of the intermetallic compounds (IMCs) formed. The bonded samples were aged at 300°C for 500 h and thermal cycled from −40°C to 125°C for 500 cycles. The results showed that the shear strength of the Cu/In joint was higher than that of the Au/In joint with increasing aging time. Cu/In specimens on a ceramic substrate also showed good reliability results during the thermal cycling test. Even though Cu/In TLP bonding is not popular in conventional electronics, it is suitable for high temperature electronics due to the simplicity of the IMC formation.

Key words: Transient liquid phase bonding, rugged electronics, die-attach bonding, high-temperature storage test, temperature cycle test, interfacial microstructure

INTRODUCTION

The demand for extremely high-temperature endurable electronics systems, which require highly reliable and stable functionality, has been rapidly increasing, particularly for electronics for the automotive and aerospace industries, and for down-hole drilling application for the oil and gas industries. The aerospace industry now has a growing movement toward the more electric aircraft (MEA). Moving to a distributed control scheme in aircraft places the control electronics closer to the engine with high-temperature conditions up to 250°C or higher. Deep oil and gas drilling can also be performed in harsh environments, and the tools including control and sensing electronics inside need to survive pressures up to 30,000 psi and temperatures up to 300°C for deeper exploration in the near future. This requirement is far beyond the operational limit of conventional silicon (Si)-based devices and their packaging technologies which are normally considered to be less than 150°C. In order to increase the operating temperature of the devices to meet the requirements of 300°C environment applications or even higher, it is necessary to substitute existing Si-based device technology with the wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN). At the same time, ensuring that the packaging and interconnection technologies for continuous operation under harsh environments up to 300°C is crucial to avoiding any degradation of power and signal integrity, thermo-mechanical stability, interconnection reliability, bonding strength, and so on. This is where highly reliable die-attach technology is required.

Transient liquid phase (TLP) bonding is a novel die-attach method for power devices, due to its properties such as high re-melting temperature, high thermal conductivity, low mechanical stress, and high yield strength. The attractiveness of TLP bonding is that it can be processed at a much lower temperature and remained stable at relatively higher temperatures. This is important for temperature-sensitive materials whose micro-structures can be damaged by too much thermal energy input and therefore have to be joined at lower process temperatures.[1,2] Another advantage of TLP bonding is that the bonding layer often has similar microstructures to the properties of the base material.[3,4] Some studies have reported that they are as strong

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as the base material or even stronger, causing the failure in the base material rather than in the joint.[5–7] Over the past few decades, the diffusion soldering process has been used for die-attach purposes such as Cu/Sn, Ni/Sn and Au/Sn.[8–10] One of the good candidates of TLP bonding for die-attach is indium (In) which can also be applied as a joining material due to its low melting temperature in forming high melting intermetallic compounds (IMC).

Table I shows several intermetallic systems such as Au/Sn, Cu/Sn, Au/In and Cu/In for TLP bonding. The Au/In system exhibits the highest material cost and is susceptible to In oxidation. Cu/Sn, on the other hand, has a complex phase diagram and forms multiple IMCs. In the Cu/In system, In layer is typically covered with a 20-nm-thick Au layer to prevent oxidation, and Cu base metal was chosen to reduce the material cost. Above all, it is noteworthy that the high re-melting temperature of Cu/In IMCs such as $\delta(Cu_7In_3)$ and $\eta(Cu_7In_4)$ enable reliable high-temperature operation up to approximately 600°C.

The aim of this study is to evaluate the reliability of TLP bonding of Cu/In, Au/In and Cu/Sn3Ag joints at elevated temperature aging conditions up to 300°C. This also enabled us to analyze the microstructural changes after reliability testing. A Cu substrate was chosen for this work as Cu is the most commonly used surface finishing in micro-electronic packaging applications. In was selected due to its relatively low melting point (157°C) in comparison to base metal Cu, and because several In-containing alloys are able to be formed at temperatures less than 180°C. In also has a low vapor pressure, making it suitable for use in such high vacuum applications. Nonetheless, as the characteristics of Cu/In IMC as a TLP bonding for die-attach have been little investigated, the evaluation and characterization of Cu/In TLP before and after reliability testing will be the major focus of the current study.

EXPERIMENTAL PROCEDURE

Figure 1 shows the metal stacks schematics of Au/In (a) and Cu/In (b) TLP bonding. Silicon wafers were initially sputter deposited with 0.1 μm Ti and 0.2 μm Cu as adhesion layer and electroplating seed layer, respectively. Half of these wafers were then electroplated with 1-μm-thick Ni and 0.3-μm-thick Au and the rest were electroplated with 1-μm-thick Cu. Finally, 0.5-μm-thick In and 20-nm-thick Au were evaporated sequentially on these wafers to form a stack of Au/In and Cu/In bonding layer. The 20-nm-thick Au capping layer was used to protect In layer from oxidation. The capping layer works to maintain sufficient amount of pure In before reaching its melting temperature, and not to leave any molten In during the bonding process. The fabricated wafers were finally thinned down to 300 μm thickness and diced into chips with dimensions of 3 mm × 3 mm.

Prior to bonding, the dies were cleaned by Ar and H_2 plasma for 60 s. Au/In dies were then bonded together such that the In layers were sandwiched between the two dies under a pressure of 50 MPa and 100 MPa followed by heating up to 200°C. A similar sandwiched configuration was used for Cu/In dies. Bonding time of 300 s at 200°C was used to complete the isothermal reaction of the liquid phase and solid phase to form intermetallics. The

Table I. Comparison of the Cu/In TLP bonding with available TLP bonding methods

Material	Temperature (˚C)		Relative market price	Popularity in conventional electronics	Issue	
	Bonding	Re-melt			Native oxide (ΔG^0) (kJ/mol)	Complex phase diagram
Ni/Sn	○ 300	○ 400	◎ Ni: 1 Sn: 0.8	◎	△ NiO: ~−200 SnO: −260	○
Ag/Sn	○ 250	○ 600	△ Ag: 63 Sn: 0.8	△	○ Ag_2O: −11.2 SnO: −260	○
Au/Sn	△ 450	◎ 900	X Au: 2600 Sn: 0.8	△	◎ Au_2O_3: ~80 SnO: −260	○
Cu/Sn	○ 280	○ 415	◎ Cu: 0.5 Sn: 0.8	○	△ Cu_2O: −146 SnO: −260	△
Au/In	○ 200	○ 495	X Au: 2600 In: 37.5	△	X In_2O_3: −620 Au_2O_3: ~80	○
Cu/In	○ 200	○ 667	○ Cu: 0.5 In: 37.5	X	X In_2O_3: −620 Cu_2O: −146	○

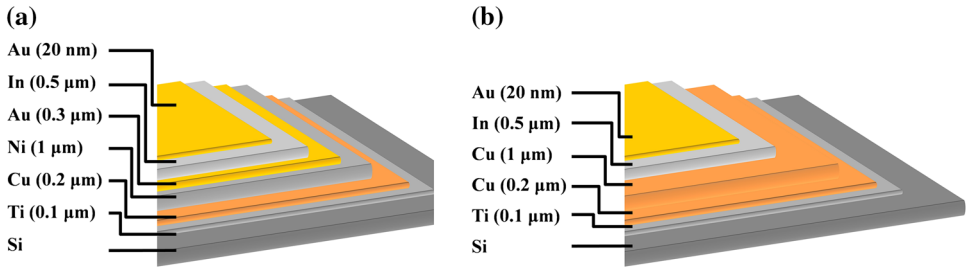

Fig. 1. Metal stacks schematics of the Au/In (a) and Cu/In (b) TLP bonding.

bonding was carried out in ambient air condition. Bonded samples were finally stored in a high-temperature chamber at 300°C for the high-temperature storage (HTS) test. The storage times were 100, 300, and 500 h. After the HTS test, die shear test, cross-section, scanning electron microscope (SEM) and energy dispersive x-ray spectroscope (EDX) investigations were carried out to characterize the joint strength and reliability.

A thermal cycling (TC) test was also performed to determine the ability of the TLP joint to withstand cyclical exposures against the coefficient of thermal expansion (CTE) mismatch between the substrate and the chip. Since the Au/In joint failure was observed after the HTS test, only Cu/In and Cu/Sn3Ag specimens were prepared for the TC test. Instead of the Si substrate, Al_2O_3 ceramic substrates plated with 45-μm-thick Cu were used for Cu/In and Cu/Sn3Ag TLP bonding to study CTE mismatch behavior. For the case of the chip to ceramic substrate, relatively thicker In and Sn3Ag layers (6 μm) were evaporated and electroplated onto the 725-μm-thick Si wafer, respectively, due to relatively high roughness (R_t: ~3 μm) of the Cu surface on ceramic substrate. The thermal cycle profile consisted of 10 min ramps from −40°C to 125°C, then soaking for 20 min, followed by 10 min cooling from 125°C to −40°C and soaking for another 20 min. A die shear test was also used to evaluate the bonding strength at the end of the reliability test. Cross-sectioned samples before and after reliability testing were analyzed using SEM and EDX.

RESULTS AND DISCUSSION

Figure 2 shows the die shear strength of the Cu/In joint bonded with two different bonding pressures after flux and Ar and H_2 plasma treatment. The plasma treatment before the bonding increases the bonding strength significantly. The bonding strength peaked at 16.8 MPa for samples bonded at 50 MPa of bonding pressure after treatment with Ar and H_2 plasma, indicating that the plasma pre-treatment was effective in the removal of the native oxide and activation of the bonding surface. Flux cleaning was also effective in increasing joint strength whereas the shear strength was too low or had irregular values without any pre-treatment. However, the effect of flux cleaning was less than plasma cleaning, probably because of the voids

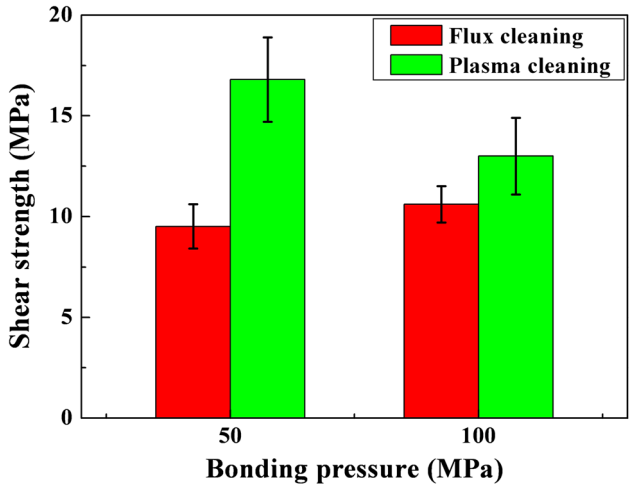

Fig. 2. Shear strength of the Cu/In joint with various bonding pressure after flux and plasma treatment.

generated by evaporation of the flux and the low bonding temperature for the Cu/In joint which was not sufficient to completely evaporate the flux and generated the residue between interfaces.

Figure 3 shows the shear strength of the Cu/In and Au/In joints during the HTS test at 300°C. Increased shear strength of the Cu/In joint at 100 h of storage time was due to the additional reaction of excess In remaining after the initial bonding. A bonding time of 300 s is not sufficient to fully convert the Cu/In metal to IMC. The failure mode of the Cu/In shear test at 100, 300 and 500 h was Si chip fracture and not at the bonding interface. Therefore, the shear strength of the Cu/In joint was saturated within the range of 23–25 MPa. On the other hand, all shear strengths of the Au/In joint were far lower than that of the Cu/In joint after HTS testing at 300°C for all test durations ranged from 0 h to 500 h. Generally, sufficient amounts of In are required for a stable Au/In joint to get better wetting behavior and break the thin $AuIn_2$ layer on the outermost bonding surface, which is formed during the deposition of the thin Au capping layer to prevent In oxidation.[11,12] An In layer 0.5 μm thick between the Au layer and the thin Au protection layer was found to be insufficient to form a continuous IMC layer during the TLP bonding compared to the Cu/In joint, which showed good shear

strength even after 300°C and 500 h of HTS test. The reason for the lower shear strength of the Au/In layer is supposed to be the fast inter-diffusion rate of Au and In during the bonding process. Au and In joints are believed to be the fastest among the TLP bonding of available metals. It is known that the inter-diffusion between Au and In can occur even at −50°C.[13] Therefore, the fast reacting In layer degraded the wettability of the chip to chip bonding surfaces and caused a lower shear strength than that of the Cu/In joint before and after the HTS test.

Figure 4 shows the cross-sectioned images of the Au/In joint after (a) bonding and (b) the HTS test, whereby the stack of the upper and lower chips was Ni/Au/In/Au (1 μm/0.3 μm/0.5 μm/20 nm). The temperature ramping rate of the upper chuck in the bonding machine is usually faster than the lower chuck, resulting in the tendency of In atoms to diffuse to the upper Ni layer rather than to the lower Ni layer, as shown in Fig. 4a. The joint after TLP bonding exhibits good quality, even though some discontinuities between the α_1 and the In-rich IMC phase are observed. The thickness of IMCs is increased after 300°C HTS testing, indicating that the phase evolution has been continued during thermal aging, as shown in Fig. 4b. In was not only reacted with Au but also reacted with Ni, which was uniformly distributed in the (Au, Ni)In_2 layer. The voids and cracks were observed at the boundary between (Au, Ni)In_2 and AuIn IMCs. The crack always presents a brittle appearance due to the large differences of micro-hardness between $AuIn_2$ (77 HV) and AuIn (273 HV).[14] The cracks and insufficient In layer thickness are suspected to be the cause of the degradation in shear strength of the Au/In joint compare to the Cu/In joint.

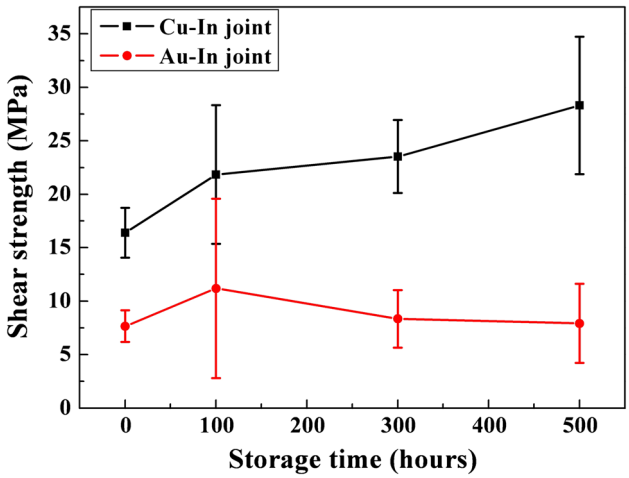

Fig. 3. Variation of the shear strength of Cu/In and Au/In joints during HTS testing.

Figure 5 shows the cross-sectioned images of Cu/In joint after (a) bonding and (b) HTS testing, where the stack of the upper and lower chips was Cu/In/Au (1 μm/0.5 μm/20 nm). The quantitative EDX point analysis showed an In enrichment up to 42–46 at.% in the bright region and 29–31 at.% in the dark region for the joint after bonding. This suggests that the IMCs are composed of Cu_9In_{11} and $\delta(Cu_7In_3)$, respectively, after bonding for 300 s at 200°C, as shown in Fig. 5a. The IMC layer was fully converted to a $\delta(Cu_7In_3)$ layer during HTS testing at 300°C due to the relatively lower melting temperature of $Cu_{11}In_9$ eutectic structures. However, any crack or defect could not be observed in the reaction layer. These results are consistent with the die shear test results during HTS testing shown in Fig. 3.

Chip to substrate samples with TLP bonded joints of Cu/In and Cu/Sn3Ag on ceramic substrates were subjected to 300°C HTS and TC tests (−40 to 125°C). Au/In was not included for the chip to substrates investigation, because the Au/In joint already showed the crack and adhesion degradation after the HTS test from the chip to chip case. A reaction layer 6 μm thick such as the In and Sn3Ag layers was used for the chip to ceramic bonding because of the high roughness of the Cu surface on the ceramic substrate. The maximum peak to valley height in the sampling area (R_t) value of the Cu surface measured by atomic force microscopy was about 3 μm. Figure 6 shows the shear strength of Cu/In and Cu/Sn3Ag joints during 300°C HTS testing. The shear strength values of both Cu/In and Cu/Sn3Ag

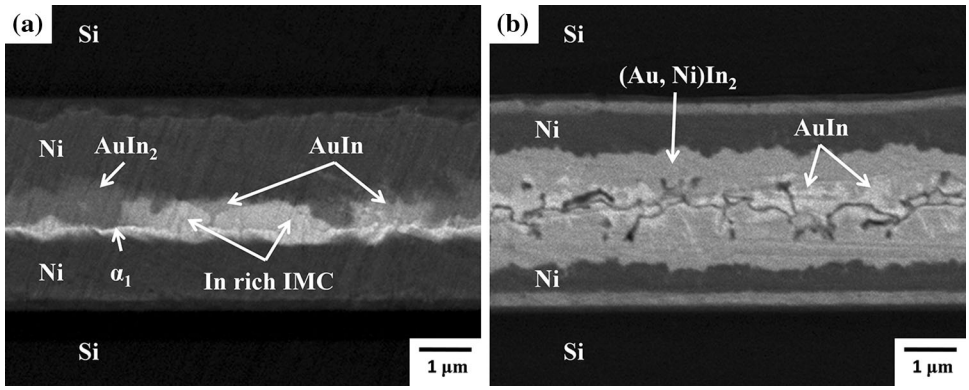

Fig. 4. Cross-sectioned images of the Au/In joint after (a) bonding and (b) 500 h of HTS testing.

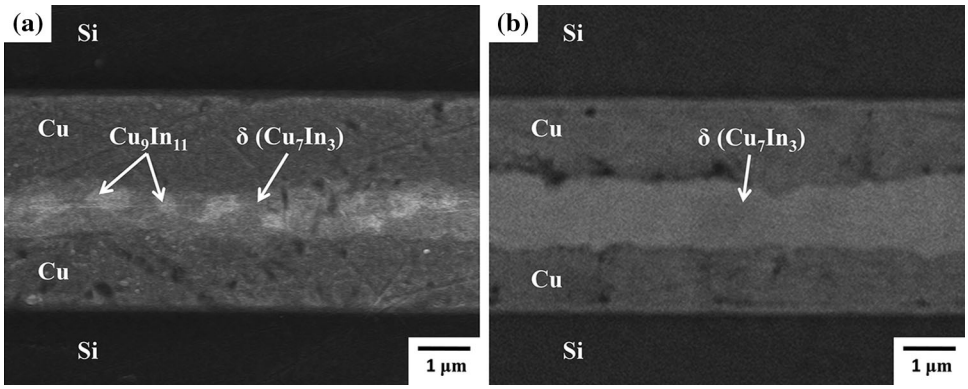

Fig. 5. Cross-sectioned images of the Cu/In joint after (a) bonding and (b) 500 h of HTS testing.

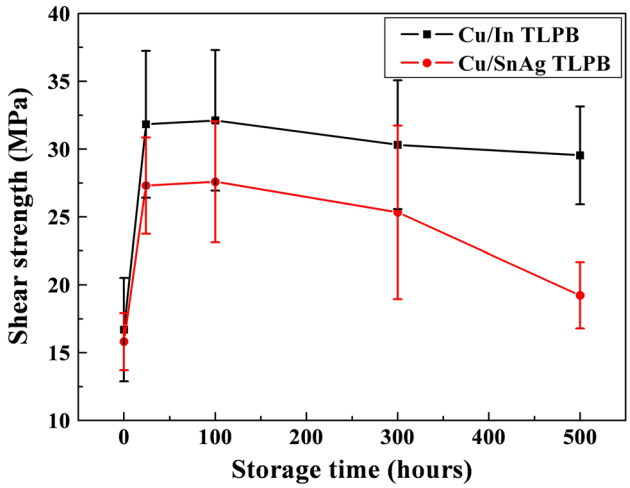

Fig. 6. Variation of the shear strength of Cu/In and Cu/Sn3Ag joints during HTS testing.

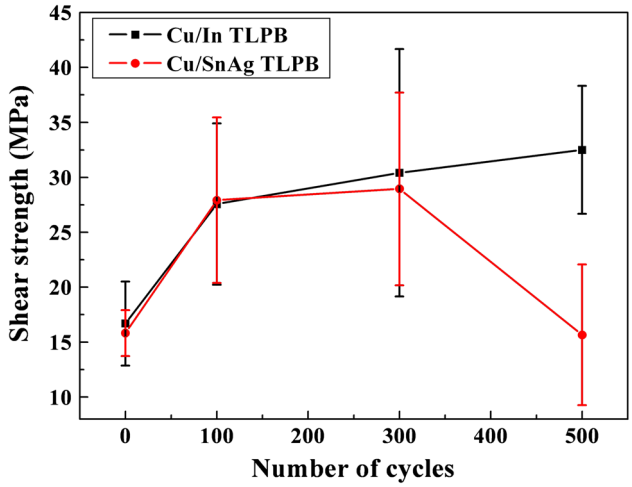

Fig. 7. Variation of the shear strength of Cu/In and Cu/Sn3Ag joints during TC testing.

joints were significantly increased during initial stages of HTS testing, because non-fully formed IMCs right after the bonding process were quickly changed to full IMCs at the bonding interface. Overall shear strength of the 6-μm-thick Cu/In joint showed a higher value than the Cu/Sn3Ag joint due to higher hardness of Cu/In IMC compared to Cu_3Sn or Cu_6Sn_5 IMC in the Cu/Sn3Ag joint. The hardnesses of η phase Cu/In IMC, Cu_3Sn and Cu_6Sn_5 are 9.5 GPa, 6.5 GPa and 3.6 GPa, respectively.[15,16] The average value of Cu/In joint strength was stabilized when the joint was fully transformed to IMCs after 24 h of HTS testing. The shear strength of the Cu/Sn3Ag joint was significantly decreased after 500 h of HTS testing. However, the shear strength was still 3 times higher than the MIL-STD-883G specification.

Figure 7 shows the shear strength of Cu/In and Cu/Sn3Ag joints during TC testing. The increasing rate of the shear strength for the Cu/In joint after 100 cycles of TC testing was slower than that of HTS testing due to the relatively lower peak temperature during the TC test. Nevertheless, the shear strength of the Cu/In joint was slightly increased during the TC test. Figure 8 shows the cross-sectioned images of the Cu/In joint on the ceramic substrate (a) before and (b) after 500 cycles of TC testing. Bonding conditions were same as for thin reaction layer chip to chip bonding. In-rich IMCs were found at the joint due to insufficient bonding and heating time for the 6-μm-thick In layer, as shown in Fig. 8a. The central part comprised the Cu_9In_{11} IMCs formed due to isothermal solidification. The darker phases between Cu_9In_{11} and Cu base metal were supposedly $\delta(Cu_7In_3)$ IMCs. Continuous small voids were found within the IMC. It was suspected that the Cu oxide layer was not fully removed before bonding and caused the tiny voids at the bonding interfaces. However, after 500 cycles of TC testing, relatively large voids and micro-cracks were observed in the middle of TLP layer as shown in Fig. 8b. Cu_9In_{11} IMC could still be observed in the bonding layer after 500 cycles of TC testing. Possible mechanisms of voids and crack

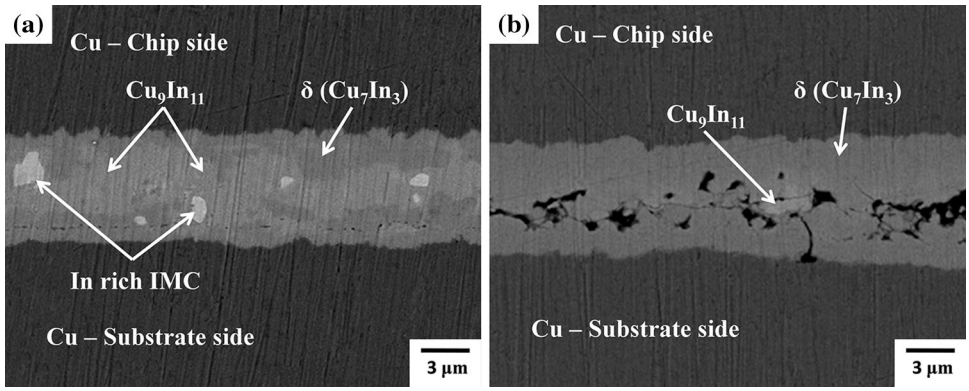

Fig. 8. Cross-sectioned images of the Cu/In joint on ceramic substrate (a) before and (b) after 500 cycles of TC testing.

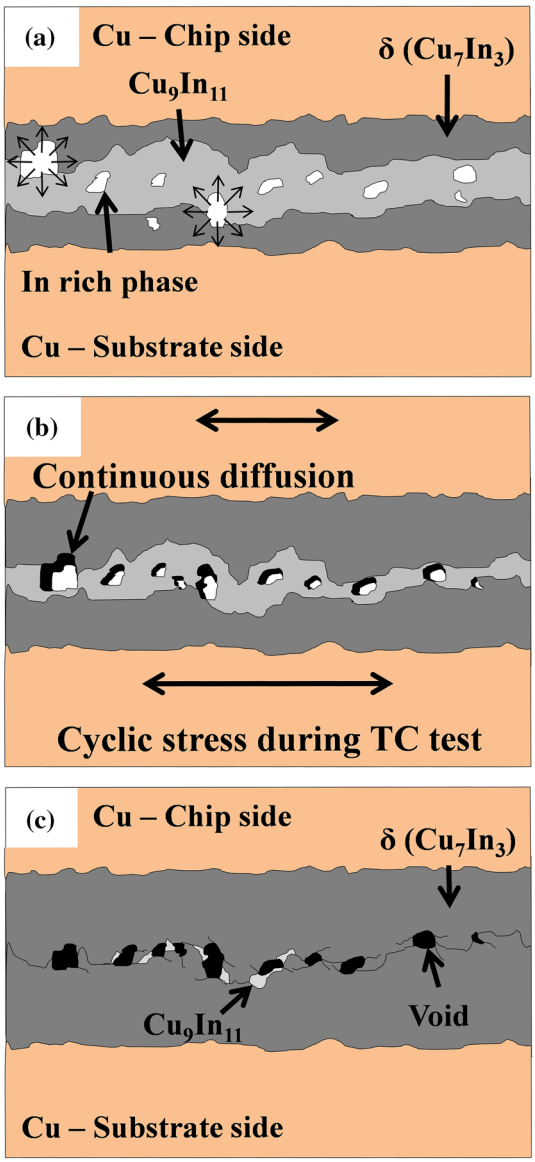

Fig. 9. Illustrations showing the reaction of the In rich phase diffusion to Cu_7In_3 IMC.

formation during TC testing are illustrated in Fig. 9. There is a cyclic stress during the TC tests. Ceramic substrates expand more than Si chips while the test samples are in the high-temperature stage (125°C). Because peak temperature during TC tests is much lower than the melting temperature of Cu_9In_{11} IMC (276.6°C), the diffusion rate of the In-rich phase into relatively stable Cu_9In_{11} or $\delta(Cu_7In_3)$ IMCs is considered to be much faster than the diffusion rate of the stable IMCs into the In-rich phase as shown in Fig. 9a. As the cyclic stress induced to the IMCs during TC testing, the In-rich phases which have a faster diffusion rate were consumed to make Cu_9In_{11} and $\delta(Cu_7In_3)$ and the voids remained in the IMCs, as shown in Fig. 9b.

This process accelerates the growth of the voids and micro-cracks propagate through the bulk IMCs in a web-like structure linking the Cu_9In_{11} IMCs and voids as shown in Fig. 9c. As mentioned, it is supposed that the huge difference in the diffusion rate between IMCs already formed during TLP bonding and the non-reacted In-rich phase during TC conditions could be considered to be the root cause of the severe voids and cracks after TC testing. Voids and cracks can be avoided when the IMC layer is fully transformed to stable phase at the bonding stage or by adding additional thermal aging to remove the In-rich phase. For the chip to chip bonding case shown in Fig. 5a, the In-rich phase was not detected after bonding and also there were no voids after HTS testing as shown in Fig. 5b. Even though the micro-cracks and voids existed in the TLP joint, the shear strength was strong enough to exceed the MIL-STD-883G specification and thus the fracture mode during die shear test was chip cracking instead of joint fracture.

On the other hand, the shear strength of the Cu/Sn3Ag joint significantly decreased after 500 cycles of TC testing, as shown in Fig. 7. The Cu_6Sn_5 IMC layer was obtained by bonding for 300 s at 250°C, as shown in Fig. 10a. Some voids were observed in the middle of the IMC layer after assembly which was

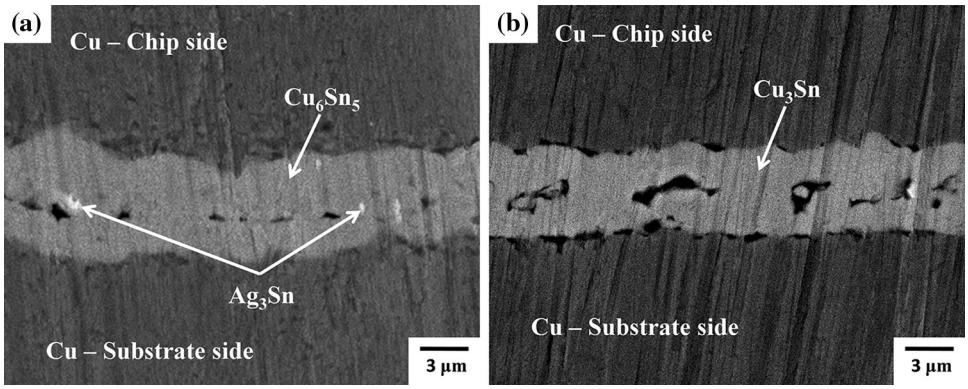

Fig. 10. Cross-sectioned images of the Cu/Sn3Ag joint on ceramic substrate (a) before and (b) after 500 cycles of TC testing.

suspected to be generated by the flux evaporation during the bonding process with a relatively higher temperature than the Cu/In case (200°C). However, those initial voids were increased in the middle of the IMC after TC testing. Also, the large voids were generated at the interface between Cu_3Sn IMC and the Cu-metalized layer for both the chip and substrate sides. The increase of those voids was caused by transformation from Cu_6Sn_5 to Cu_3Sn and repetitive shear stress concentrated at the crest and trough induced by the rough ceramic surfaces during TC testing. The fracture mode after die shear testing was the brittle failure occurring between IMC and the Cu substrate.

CONCLUSION

The reliability of TLP bonded dies of Cu/In, Au/In and Cu/Sn3Ag was successfully characterized. Ar and H_2 plasma pre-treatment was effective in the removal of the native oxide and activation of the bonding surface. The shear strength of the Cu/In joint between chips was higher than the Au/In joint during HTS testing because the 0.5-μm-thick In layer was insufficient for the Au/In joint due to its relatively higher inter-diffusion rate than Cu/In. Cu/In and Cu/Sn3Ag joints on Cu-plated ceramic substrates were subjected to HTS and TC testing. The average Cu/In joint strength stabilized when the joint was fully transformed to IMCs after 24 h of HTS testing. The shear strength of the Cu/Sn3Ag joint decreased slightly after 500 h of HTS testing. Cracks and voids were found in the Cu/In joint after TC testing but did not cause the shear strength to decrease. It is supposed that the huge difference in the diffusion rate between IMCs already formed during TLP bonding and the non-reacted In-rich phase during TC conditiosn could be considered to be the root cause of the severe voids and cracks after TC testing. On the other hand, the shear strength of Cu/Sn3Ag joint decreased significantly after TC testing. Phase transformation at dissimilar metallic bonding joints is critical for long-term reliability.

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